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Fully Differential Op-Amp Is Designed Using The Proposed Compensation Scheme

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Abstract: *This paper concerns the design and implementation of CMOS operational amplifier with current mirror load in 0.18um process to satisfy some specifications such as,: V_{DD} = 1.8V, SR >= 10V/us (C_L = 2pF), phase margin 60^0, f_{-3dB}>= 100kHz (C_L = 2pF), a small signal gain A >=1000 V/V, ICMR is [0.7V, 1.1V] and P_{diss}<=1mW.And shows DC response, AC response, and transient response. CMOS gates are not particularly effective in detecting and reacting to small signal changes, because of the relatively small transconductance of the MOS device. In order to work properly and to achieve high performance, reduced-swing circuits normally require amplifier circuits, whose task it is to restore the signal to its full swing in a minimum amount of time and with a minimum amount of extra energy consumption.*

Keywords: *CMOS operational amplifier, cascade amp, current gain.*

I. Introduction

The operational amplifier, which has become one of the most versatile and important building block in analog circuit design. Operational amplifiers are amplifiers (controlled sources) that have sufficiently high forward gain. But most of the amplifiers do not have a large enough gain such as current amplifier, cascade amplifier. One of the most popular Op-Amp is a two stage op-amp, because it can be used as the starting point for the development of other types of Op-Amp. The Op-Amp (Operational Amplifier) is a high gain, dc coupled amplifier designed to be used with negative feedback to precisely define a closed loop transfer function. The basic requirements for an Op-Amp are sufficiently large gain (the accuracy of the signal processing), Differential inputs, frequency characteristics that permit stable operation when negative feedback is applied. More over with developments in deep sub micrometer CMOS processes, the available dynamic range in Operational Amplifiers (Op-Amps) is reduced due to lower power supply voltages [1]. This loss in dynamic range tightens the noise budget. A larger load capacitor should therefore be used to reduce the circuit noise, and hence increase the Signal-to-Noise Ratio (SNR), which in turn decreases the bandwidth of the amplifier [2]. With ever increasing data rates, many mixed-signal applications, however, require fast settling Op-Amps. There are also some other requirements such as high input impedance, low output impedance, high speed and frequency.

II. Ideal Operational Amplifier

Ideally an Op-Amp has an infinite differential voltage gain, infinite input resistance and zero output resistance. For most application where unbuffered CMOS Op-Amp is used, an open loop gain of 2000 or more is usually sufficient. The symbol of Op-Amp is as shown in figure (1). Where in non ideal case the output voltage V_{out} can be express as:

$$V_{out} = A_v(v_1 - v_2)$$

Where A_v is used for the open loop differential voltage gain, v_1 and v_2 are the input voltages applied to the non inverting and inverting terminals respectively. Moreover this is the kind of Miller Compensation of Two-Stage Op-Amp and also that Miller capacitance compensation is extensively used in two-stage Op-Amps and other applications [2]-[3].Actually the basic function of the Op-Amp is to produce an updated value of the output in response to a switching event at the input in which the sampling capacitor is charged from the source and discharged into the summing node.

III. Design of Operational Amplifier

There are some conditions and requirements for designing the operational amplifier. In this manner we have some boundary conditions such as:

1. Process specification (V_t, K, C_{ox})
2. Supply voltage and range
3. Supply current and range

4. Operating temperature and range

And the requirements for CMOS Op- Amp are; Gain bandwidth, Settling time, Slew rate, Common-mode input range (CMIR), Common-mode rejection ratio (CMRR), Power-supply rejection ratio (PSRR), Output-voltage swing, Output resistance, Offset, Noise, Layout area.

IV. Calculation and Compensation of Op-Amp

Compensation achieves stable operation when negative feedback is applied around the Op-Amp. Compensation plays such a strong role in design. There are many types of compensation such as; Miller compensation (Miller capacitor only, Miller capacitor with a unity-gain buffer to block the forward path through the compensation capacitor, Miller with a null resistor), Self compensating and Feed forward.

Here we use Miller Compensation of the Two-Stage Op-Amp shown in fig (2).

The various capacitors are:

C_C =accomplishes the Miller compensation

C_M =capacitance associated with the first-stage mirror (mirror pole)

C_I =output capacitance to ground of the first-stage

PMOS

From fig. (3) We see that

L=0.24 μ m and W=2.4 μ m, I_{DS}=7.6 μ A and V_{DS}=804mV

I_{DS}=40.4 μ A and V_{DS}=804mV, I_{DS}=6.8 μ A and V_{DS}=1.21V

I_{DS}=38.2 μ A and V_{DS}=1.21V

We find v_t for PMOS by following Equation

$$I_{DS} = \frac{K_p}{2}\left(\frac{W}{L}\right)_p (V_{GS}-V_t)^2(1+\lambda V_{DS})$$

$$40.4\times10^{-6} = \frac{K_p}{2}\left(\frac{2.4}{0.24}\right)(0.8-V_t)^2\left(1+\lambda\times804\times10^{-3}\right) \quad (1)$$

$$7.6\times10^{-6} = \frac{K_p}{2}\left(\frac{2.4}{0.24}\right)(0.6-V_t)^2\left(1+\lambda\times804\times10^{-3}\right) \quad (2)$$

Dividing Eq. (2) by Eq. (1)

$$v_t = 0.448v$$

Also we can find K_p from following equation

$$I_{DS} = \frac{K_p}{2}\left(\frac{W}{L}\right)_p (V_{GS}-V_t)^2(1+\lambda V_{DS})$$

$$K_p = 65.789\,\mu A/V^2$$

Now we find λ for PMOS

$$I_{DS} = \frac{K_p}{2}\left(\frac{W}{L}\right)_p (V_{GS}-V_t)^2(1+\lambda V_{DS})$$

$$\lambda = 0.0016\mu m$$

NMOS

From fig. (4) We see that

L=0.24 μ m and W=2.4 μ m, I_{DS}=274 μ A and V_{DS}=800mV

I_{DS}=118 μ A and V_{DS}=800mV, I_{DS}=284 μ A and V_{DS}=1.20V

I_{DS}=124 μ A and V_{DS}=1.20V

We find v_t for NMOS by following Equation

$$I_{DS} = \frac{K_n}{2}\left(\frac{W}{L}\right)_n (V_{GS}-V_t)^2(1+\lambda V_{DS})$$

$$274\times10^{-6}=\frac{K_n}{2}\left(\frac{2.4}{0.24}\right)(1-V_t)^2 \quad (3)$$

$$118\times10^{-6}=\frac{K_n}{2}\left(\frac{2.4}{0.24}\right)(0.8-V_t)^2 \quad (4)$$

Dividing Eq. (3) by Eq.(4)

$$V_t=0.421v$$

Also we can find K_p for NMOS from following equation

$$I_{DS}=\frac{Kn}{2}\left(\frac{W}{L}\right)_n(V_{GS}-V_t)^2(1+\lambda V_{DS})$$

$$274\times10^{-6}=\frac{K_n}{2}\left(\frac{2.4}{0.24}\right)(0.6-0.421)^2$$

$$K_n=163.46\,\mu A/V^2$$

And λ for NMOS is

$$\lambda=0.0000456\mu m$$

(1) Length of Transistor is o.5μm

(2) As require phase margin

$$g_{m6}\geq10g_{m1}$$

$$C_c\geq0.22C_L$$

$$C_c=0.44pF=0.5pF$$

(3) From the identified SR and Cc, we can determine I_5

$$SR=\frac{I_5}{C_c}$$

$$I_5=I_{D5}=5\mu A$$

(4) The maximum value from the common-voltage can be determined

$$\left(\frac{W}{L}\right)_3=\frac{I_{Ds}}{K_p\left(V_{DD}-V_{cm,\max}+V_{TH1}-|V_{TH3}|\right)^2}\approx0.18$$

$$g_{m3}(g_{m4})=\sqrt{2K_P\left(\frac{W}{L}\right)_3I_{D3}}\approx10.88\times10^{-6}s$$

(5) Now we determine g_{ml}

$$g_{m1}=2\pi GWB\times C_c$$

$$g_{m1}=0.31\times10^{-6}S$$

By transconductance

$$\left(\frac{W}{L}\right)_1=\frac{g_{m1}^2}{2K_nI_{D1}}=\frac{g_{m1}^2}{K_nI_{D5}}\approx1.22\times10^{-4}$$

(6) Determine the size of M_5

$$\left(\frac{W}{L}\right)_5=\frac{2I_{Ds}}{K_n\left(V_{cm,\max}+V_{TH1}-\sqrt{\frac{I_{DS}}{K_n(W/L)_1}}\right)^2}$$

$$\left(\frac{W}{L}\right)_5 = \frac{2\times 5\mu A}{163.46\left(0.7+0.39-\sqrt{\frac{5\mu A}{163.46\times 1.22\times 10^{-4}}}\right)^2} \approx 0.13$$

So far we have completed the design of the differential input stage.

(7) Here we have designed a common source amplifier stage, while identifying g_{m6}

We know that $g_{m6} \geq 10 g_{m1}$ and $I_{D3} = I_{D4}$, $g_{m6} = 100 g_{m1} = 31\times 10^{-6} S$

$V_{DS3} = V_{GS3} = V_{GS4} = V_{DS4} = V_{GS6}$ Therefore $(W/L)_4 /(W/L)_6 = g_{m4} / g_{m6}$

Thus rectifiable M_6

$$\left(\frac{W}{L}\right)_6 = \left(\frac{W}{L}\right)_4 \frac{g_{m6}}{g_{m4}} \approx 12.7$$

At this time M_6 has DC current

(8) Next we find M_7

$$I_{D6} = \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_4} \times \frac{I_{D5}}{2} = \frac{12.7}{0.18} \times 2.5\mu A \approx 176\mu A$$

Then we have $V_{GS5} = V_{GS7}$

$$\frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_5} \times \frac{I_{D6}}{I_{D5}}$$

$$\left(\frac{W}{L}\right)_7 \approx 5$$

So far we have identified all of the dimensions of the tube, and now on the output voltage swing, small signal differential mode voltage increases. And benefits and power consumption of these three indicators are designed to meet the requirements for verification.

(9) Maximum allowable output voltage

$$V_{out,\max} = V_{DD} - \sqrt{\frac{2I_{D6}}{K_p (W/L)_6}}$$

$$V_{out,\max} = 1.8 - \sqrt{\frac{2\times 176}{65.789\times 12.7}} \approx 0.64$$

And the minimum allowable output voltage

$$V_{out,\min} = \sqrt{\frac{2I_{D7}}{K_n (W/L)_7}} \approx 0.65$$

Therefore, the outputs swing to meet the design requirement, ($0.5V \leq V_{out} \leq 2.0V$). If the output voltage swing does not satisfy this design requirement then M_6 and M_7 can be appropriately increased by width to length ratio.

(10) Small signals differential mode voltage gain A_v

$$A_v = \frac{2g_{m2}g_{m6}}{I_{D5}(\lambda_2+\lambda_4) I_{D7}(\lambda_2+\lambda_4)}$$

$$A_v = \frac{2\times 0.31\times 10^{-6}\times 31\times 10^{-6}}{5\mu A\times 176\mu A(0.000045+0.0016)^2} = 8061.41$$

Therefore A_v Indicators meet the design requirements.

(11) The static power consumption

$$P = 2.5\times(I_{D5}+I_{D6}) = 0.452mW$$

So this result meets the design requirements ($P_{diss} \le 1mW$)

Figures

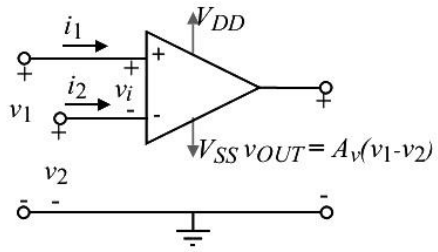

Fig. (1)

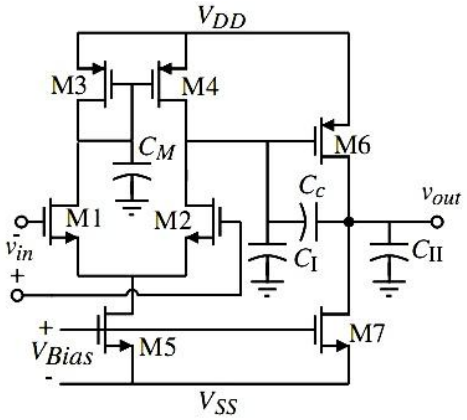

Fig. (2)

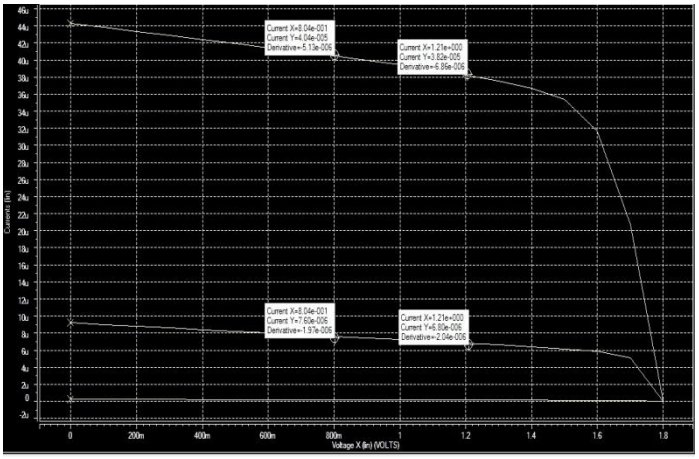

Fig. (3)

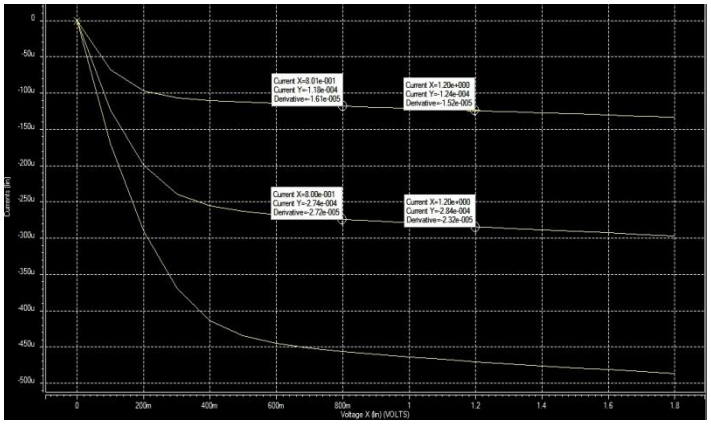

Fig. (4)

V. Conclusion

In this paper, we have attempted to summarize the various architectures and we found out the various numerical values, which have been applied in the design of CMOS operational amplifiers according to given specification. A fully differential Op-Amp is designed in a 0.18 µm standard digital CMOS process using our proposed compensation scheme. These results show a DC response, AC response, and transient response of the operational amplifier.

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