

Analysis, Simulation & Comparison of Various Multilevel Inverters Using Different PWM Strategies

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Abstract: Multilevel inverters are developed as an extension to the conventional inverters. They are widely used for high power applications as they cause very less disturbances and have the possibility to function at lower switching frequencies than ordinary two-level inverters. This paper compares different topologies of inverters. The comparison is done with respect to Total Harmonic Distortion. This paper presents a brief account on the most important topologies like diode-clamped inverter (neutral-point clamped), capacitor-clamped (flying capacitor), and cascaded H-bridge with separate dc sources. It also presents the most relevant control and modulation methods developed for this family of inverters namely sinusoidal pulse width modulation and space-vector modulation. Multilevel inverter promises a lot of advantages over conventional inverter especially for high power applications. Main advantages are that output waveforms were improved since multilevel inverter produces nearly sinusoidal output voltage waveforms, hence the THD will be low. Multilevel converter applications focus on industrial medium-voltage motor drives, utility interface for renewable energy systems, UPS, flexible AC transmission system, and traction drive systems.

Keywords: Multilevel inverter, Topology, Cascaded H Bridge inverter, Diode clamped inverter, flying capacitor inverter, Sinusoidal PWM, Space Vector PWM, THD, MATLAB/SIMULINK.

I. Introduction

Growth in industries has certainly increased the demand for high power applications which ranges to megawatt level. In order to withstand such high voltage levels a single power semiconductor device may not be sufficient. Hence it is essential to use an array of semiconductors which paved the way for the design of multilevel inverters. As indicated above multilevel inverters include an array of Power Semiconductors and capacitor voltage sources, the output of which generates voltages with stepped waveforms. As the number of steps increases there is more possibility to get a smooth and distortion less sinusoidal waveform. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages.

A multilevel inverter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind and fuel cells can be easily interfaced to a multilevel inverter system for high power applications. There are several topologies such as diode clamped multilevel inverter or neutral point clamped inverter, flying capacitor based multilevel inverter, and cascaded multilevel inverter. The main disadvantage in diode clamped multilevel inverter topologies is that it cannot be used for high power applications. Moreover flying capacitor based multilevel inverter also exhibits a disadvantage including more number of capacitors which are bulk in size and are cost effective.

II. Topologies

i. Neutral Point Clamped Inverter or Diode Clamped inverter

The most commonly used multilevel topology is the diode clamped inverter, in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. An m-level diode clamped inverter typically consists of (m-1) capacitors on the dc bus and produces m levels of phase voltages and (2m-1) line voltages. An m-level inverter's leg requires (m-1) capacitors, 2(m-1) switching devices and (m-1)*(m-2) clamping diodes. The important applications of diode clamped inverters are it produces an interface between HVDC and HVAC transmission lines as well as serves as a variable speed drive for high-power medium-voltage (2.4 kV to 13.8 kV) motors. All of the phases share a common dc bus, which minimizes the capacitance requirements of the converter. For this reason, a back-to-back topology is not only possible. The number of clamping diodes required is quadratically related to the number of levels, which can be cumbersome for units with a high number of levels.

ii. Fly Capacitor Inverter

The flying capacitor inverter is a multilevel pulse width modulated (PWM) converter has the property of automatic voltage balancing for passive loads. It thus provides an attractive alternative to the NPC. Furthermore, a single leg Fly Capacitor may be used for both DC/DC and DC/AC conversion; whereas an NPC

converter cannot serve as a DC/DC converter. Phase redundancies are available for balancing the voltage levels of the capacitors. Real and reactive power flow can be controlled. Deep voltage sags and short duration outages can be minimized by using large number of capacitors in the design of the inverter.

iii. Cascaded H Bridge Inverter

The cascaded H-bridge inverter consists of a series of full bridge inverters connected along with a separate dc source (SDCC). The output voltage is the sum of the voltages that is generated by each cell. The number of output voltage levels are $2n+1$, where n is the number of cells. The switching angles can be chosen in such a way that the total harmonic distortion is minimized. One of the advantages of this type of multilevel inverter is that it needs less number of components when compared to the Diode clamped or the flying capacitor, so the price and the weight of the inverter is less than that of the two former types. The switching angles calculation method that is used in this inverter is the same as for the previous multilevel inverters. An n level cascaded H-bridge multilevel inverter needs $2(n-1)$ switching devices where n is the number of the output voltage level.

III. PWM Strategies

The algorithms that generate the switching functions are called Pulse-Width Modulation techniques. It is one of the most flexible ways of generating pulses to a semiconductor device. There are different Pulse Width Modulation techniques used in multilevel inverters apart from the one used in conventional inverters.

A. PWM Technique

Pulse width modulation (PWM) is a technique of generating a train of pulses having constant amplitude with different time delays. This duration varies in direct proportion to the amplitude of analog signal. Power converters perform the control of electric power. In order to acquire high efficiency these converters transfer energy from a source in a switched operation mode.

B. Sine PWM Technique

In sine PWM the width of each pulse is varied in proportion to the amplitude of the sine wave whereas in single-pulse and multiple pulse modulation techniques the widths of all pulses are same. In this technique the gating signals are generated by comparing a sinusoidal reference signal with a triangular carrier wave. The gating signal for the inverter is obtained by taking the repeating sequence (triangular wave) as the control signal and comparing it with the reference wave (sinusoidal wave). In order to detect or eliminate the zero sequence currents we use zero hold circuit which compares it with the help of greater than or equal to blocks.

C. Space Vector PWM Technique

Space vector modulation is a PWM control algorithm for multi-phase AC generation, in which the reference signal is sampled regularly; after each sample, non-zero active switching vectors adjacent to the reference vector and one or more of the zero switching vectors are selected for the appropriate fraction of the sampling period in order to synthesize the reference signal as the average of the used vectors. The topology of a three-leg voltage source inverter is because of the constraint that the input lines must never be shorted and the output current must always be continuous. A voltage source inverter can assume only eight distinct topologies. For a 2 Level inverter six out of these eight topologies produce a nonzero output voltage and are known as non-zero switching states and the remaining two topologies produce zero output voltage and are known as zero switching states. For m level inverter m^3 switching states exist.

IV. Harmonics

Harmonics are the steady-state distortions to voltage and current waveforms due to the non-linear electric loads. The frequent cause of power quality problems in power grid are harmonic frequencies. Wave forms of practical inverter are non-sinusoidal and contain certain harmonics. For low –and medium power application, square wave or quasi – square wave form voltage may be acceptable but for high –power application sinusoidal waveform with low distortion are required. Harmonics content present in the output of a dc to ac inverter can be eliminated either by using a filter circuit or by employing pulse width modulation (PWM) techniques. Use of filter has the disadvantage of large size and cost, whereas use of PWM techniques reduces the filter requirement to a minimum or to zero depending on the type of application.

The summation of all harmonics in a system is known as total harmonic distortion (THD). Total harmonic distortion, or THD, is the summation of all harmonic components of the voltage or current waveform under root compared against the fundamental component of the voltage or current wave:

$$\text{THD} = \frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + \dots + V_n^2)}}{V_1} * 100\%$$

Where, V_n = RMS voltage of nth harmonic
N=1 is the fundamental frequency.

The formula above shows the calculation for THD on a voltage signal. The end result is a percentage comparing the harmonic components to the fundamental component of a signal. Higher the percentage more is the distortion present on the main signal.

V. Two Level Inverter

A device that converts dc power into ac power at a desired output voltage and frequency is called an inverter. A two level inverter consists of 6 switching devices along with 2 dc bus capacitances. These capacitors provide a dc offset voltage with respect to the source voltage. The output voltage waveform consists of only two levels +Vdc/2 and -Vdc/2 hence the name 2 level inverter. The waveform thus obtained is a quasi-square waveform. As the number of levels being low it gives high THD which is not favourable. Hence we go for multilevel inverters (MLI).

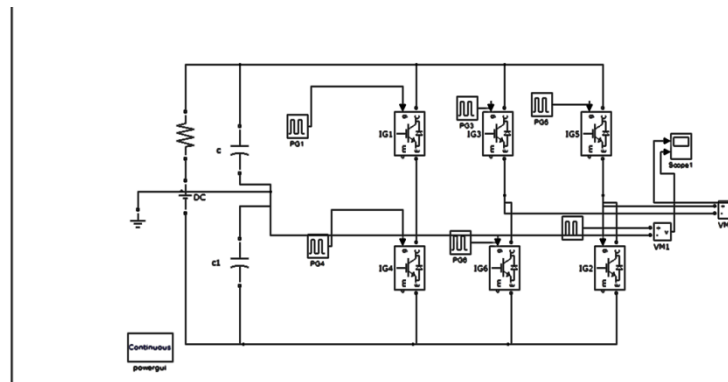


Fig 1: Two level inverter circuit using PWM

VI. Three Level Inverter

The power electronics device which converts DC power to AC power at required output voltage and frequency level is known as an inverter. Two categories into which inverters can be broadly classified are two level inverters and multilevel inverters. One advantage that multilevel inverters have compared to two level inverters is minimum harmonic distortion. A multilevel inverter can be utilized for multipurpose applications, such as an active power filter, a static VAR compensator and machine drive for sinusoidal and trapezoidal current applications. Some drawbacks to the multilevel inverters are the need for isolated power supplies for each one of the stages, the fact that they are a lot harder to build, they are more expensive, and they are more difficult to control in software. This chapter focuses on the analysis of a three-level inverter. Full analysis for the three level inverters is given. Desirable voltage and frequency have been achieved; however, harmonics distortion should be investigated during three-level inverter operation. When AC loads are fed through inverters, an output voltage of required magnitude and frequency has to be achieved. A variable output voltage can be obtained by varying the input DC voltage and maintaining the gain of the inverter constant. On the other hand, if the DC input voltage is fixed and it is not controllable, a variable output voltage can be obtained by varying the gain of the inverter, which is normally accomplished by pulse-width-modulation (PWM) control within the inverter. The inverters which produce an output voltage or a current with medium or low rate power are known as two level inverters. In high-power and high-voltage applications these two level inverters have some limitations in operating at high frequency mainly due to switching losses and constraints of device rating. This is where three level inverters are advantageous. Increasing the number of voltage levels in the inverter without requiring higher rating on individual devices which can increase power rating. The pulse width modulation (PWM) strategies are the most effective to control multilevel inverters. Even though space vector modulation (SVPWM) is complicated, it is the preferred method to reduce power losses by decreasing the power electronics devices switching frequency, which can be limited by pulse width modulation.

a) PWM Techniques Circuits.

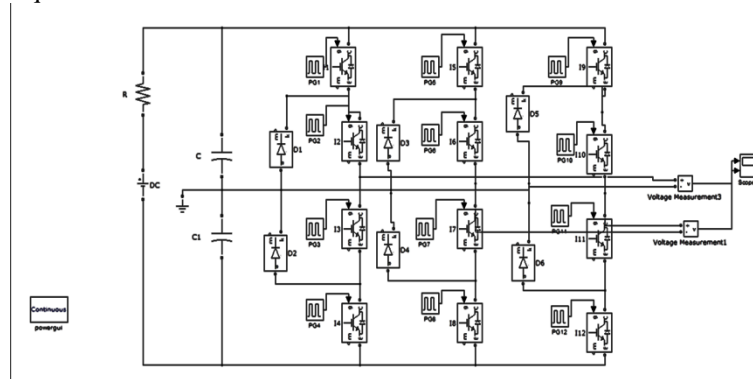


Fig 2: Neutral point Clamped inverter Circuit

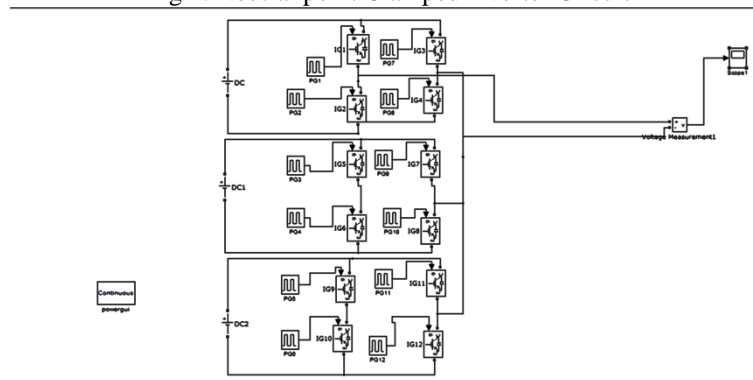


Fig 3: Cascaded H Bridge inverter Circuit.

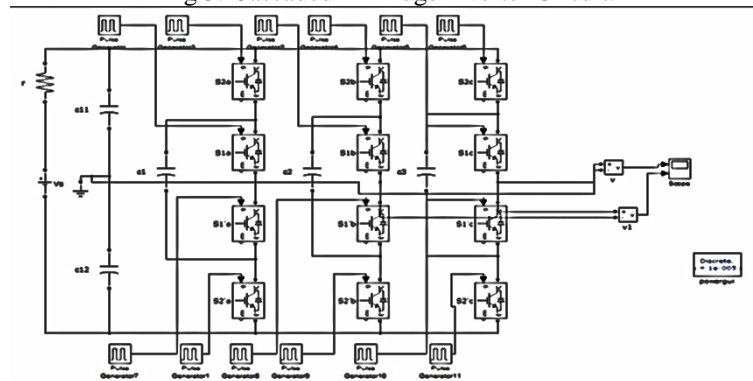


Fig 4: Fly Capacitor inverter Circuit.

b) Sine PWM Technique circuits

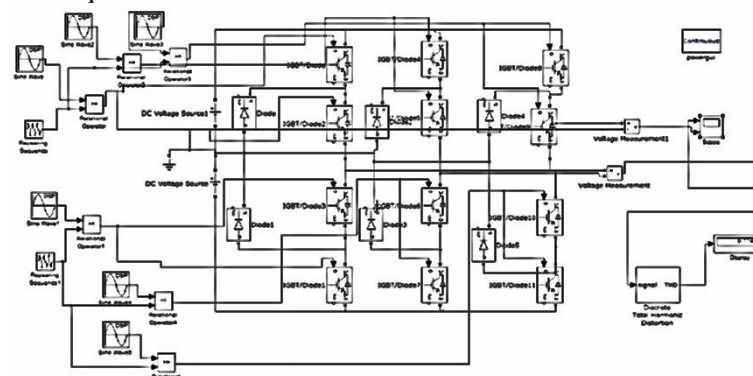


Fig 5: Neutral point Clamped inverter Circuit.

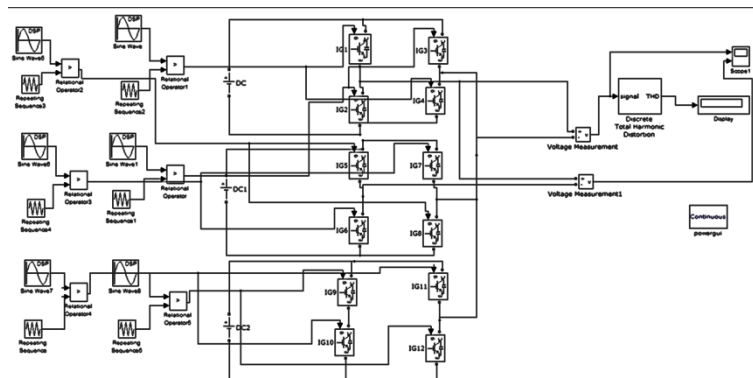


Fig 6: Cascaded H Bridge inverter Circuit.

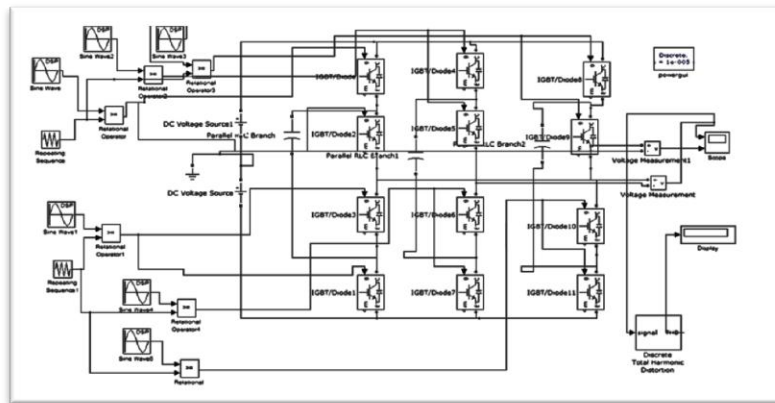


Fig 7: Fly Capacitor inverter Circuit

c) Space Vector PWM Technique circuit

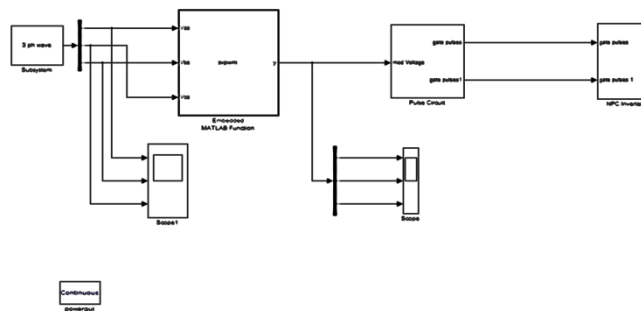


Fig 8: Neutral point clamped inverter.

VII. Five Level Inverter

Five level inverter is designed as an extension for the three level inverters. The name itself indicates that it consists of 5 levels in the line to phase output voltage waveform. The principle behind it is same as that of the 3 level inverters except for the number of switching devices, capacitors and the clamping diodes used. As there is an increase in the level of output voltage the THD gets considerably reduces and thereby efficiency increases.

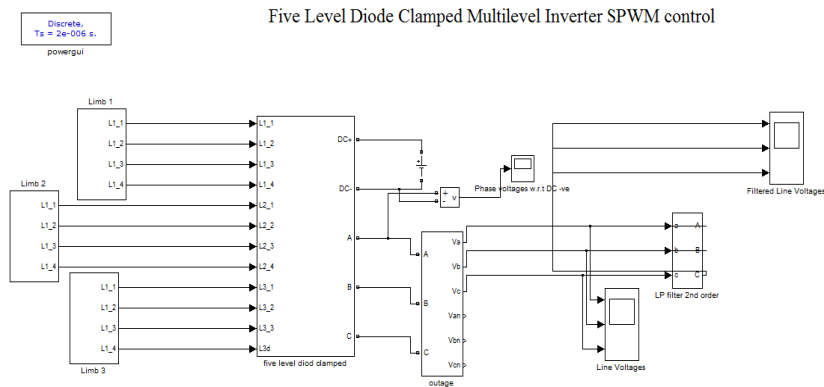


Fig.9. Neutral Point clamped inverter using SPWM

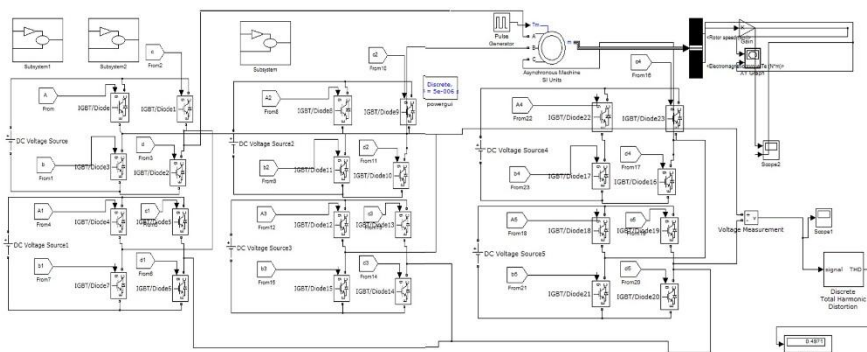


Fig.10. Cascaded H-Bridge inverter using SPWM

VIII. Simulation Results

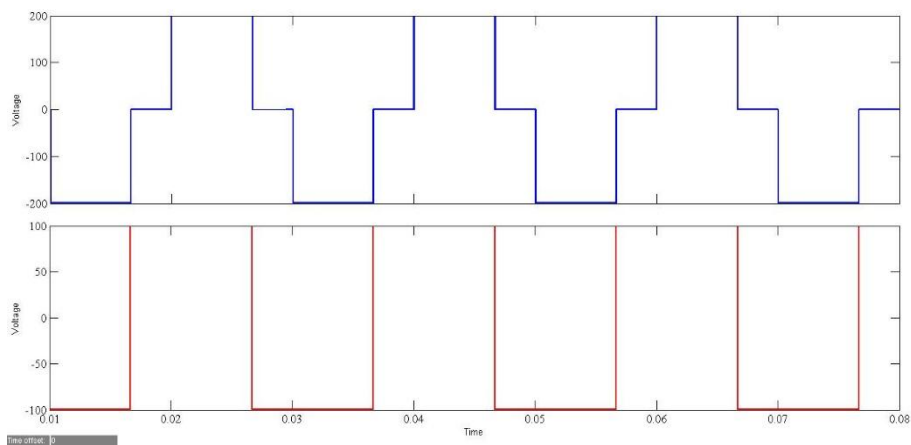


Fig 11: Output of 2 Level Inverter using PWM Technique.

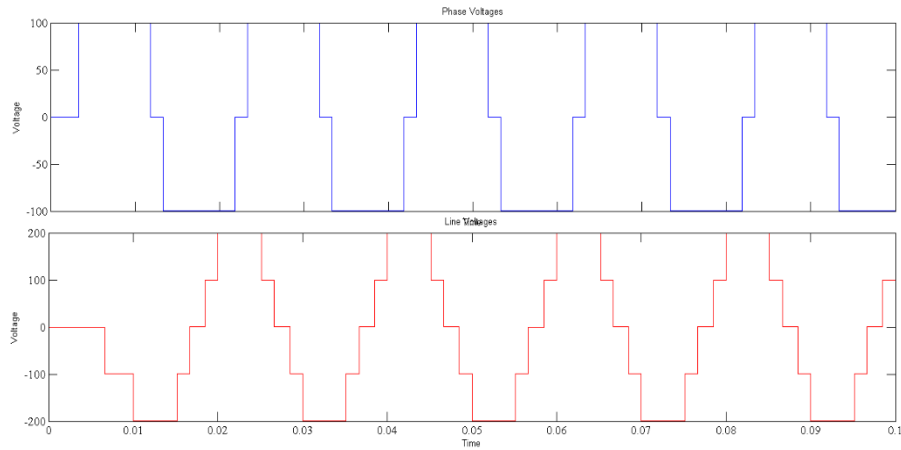


Fig 12: Output of 3 Level Inverter using PWM Technique.

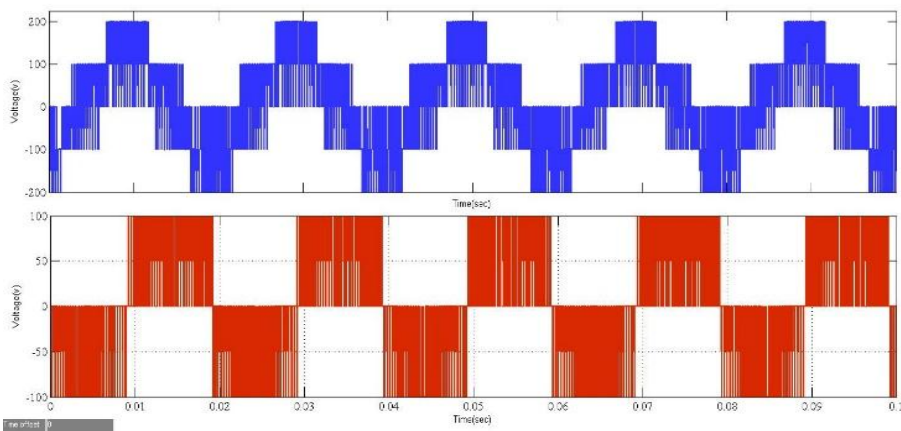


Fig 13: Output of 3 Level Inverter using SPWM Technique.

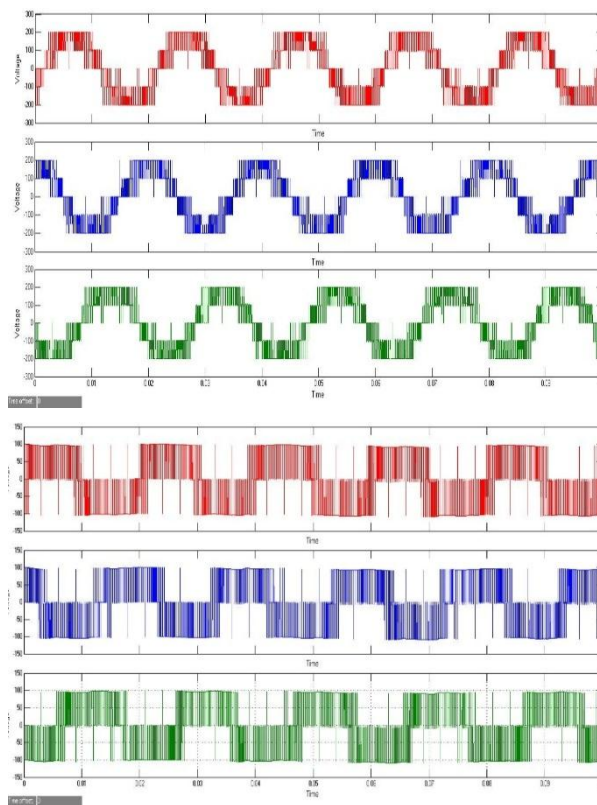


Fig 14: Output of 3 Level Inverter using SVPWM Technique.

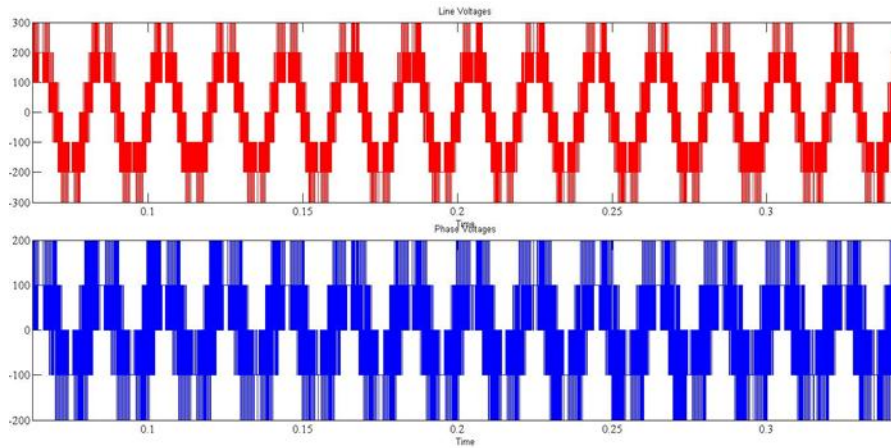


Fig 15: Output of 5 level cascaded H Bridge inverter.

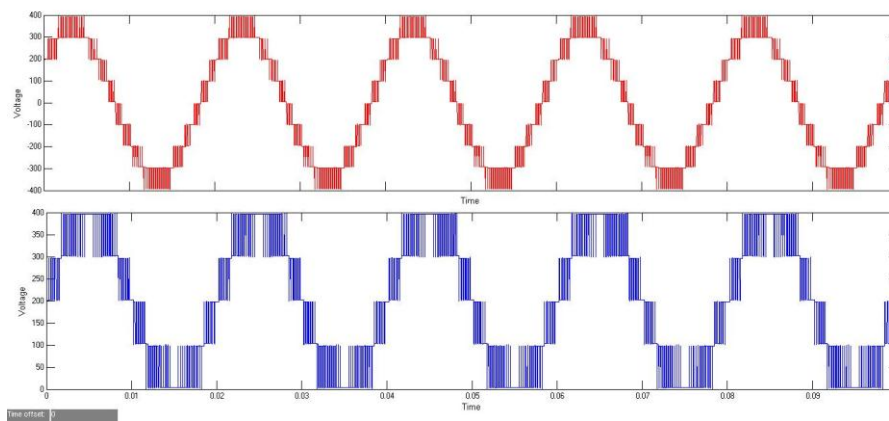
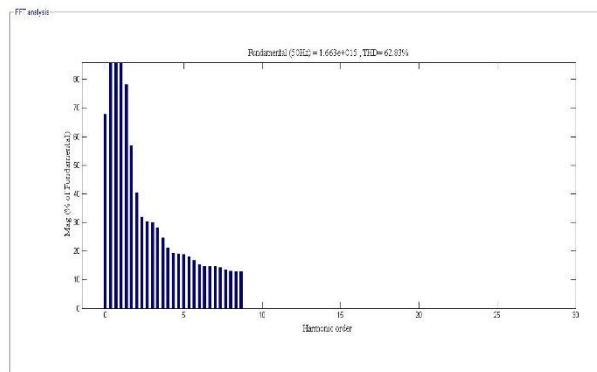
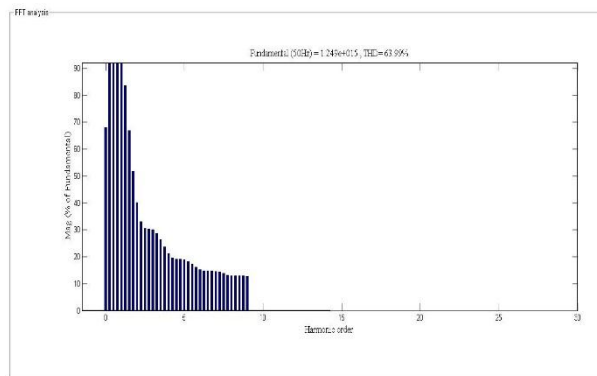


Fig.16. Output of 5 Level NPC inverter

THD of Different Multilevel Inverters



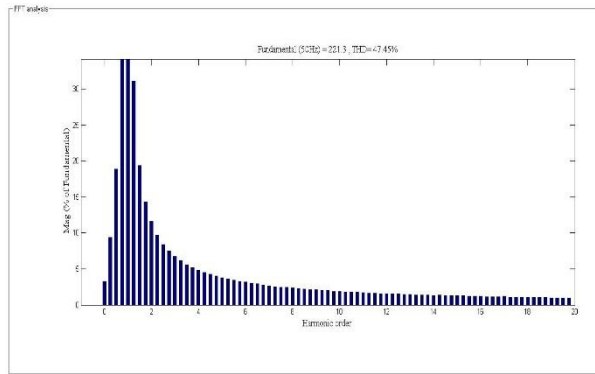


Fig 17: Total Harmonic Distortion of Two Level Inverter using PWM, SPWM, SVPWM

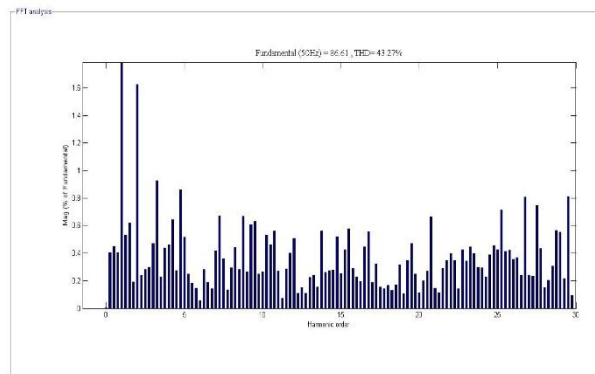
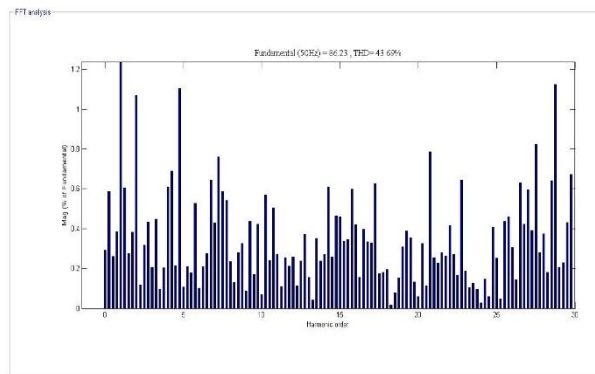
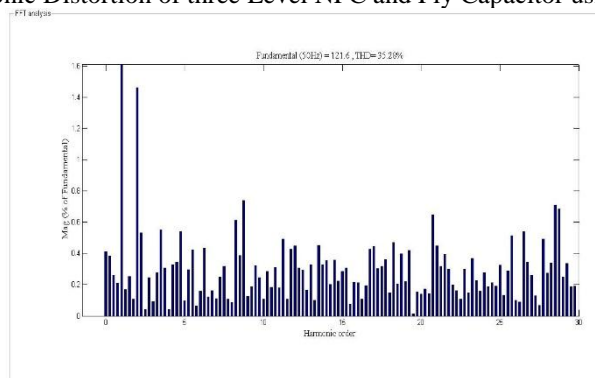


Fig 18: Total Harmonic Distortion of three Level NPC and Fly Capacitor using PWM Technique.



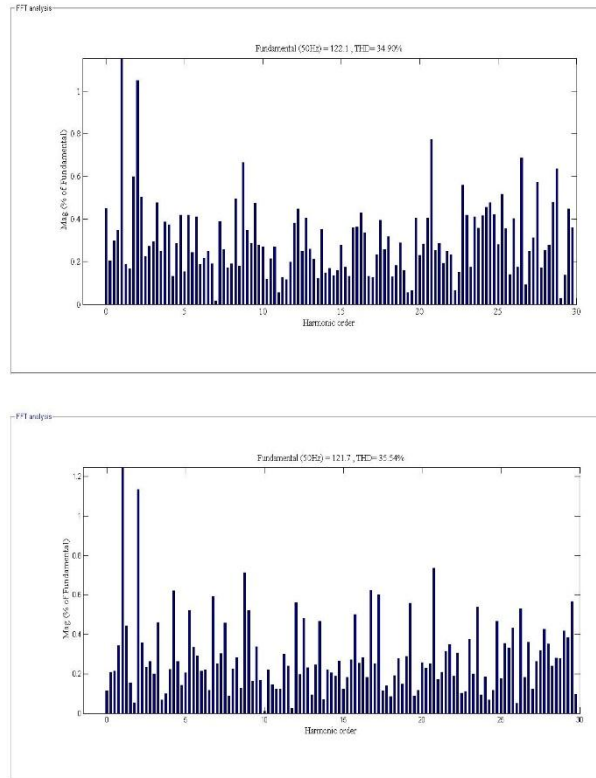
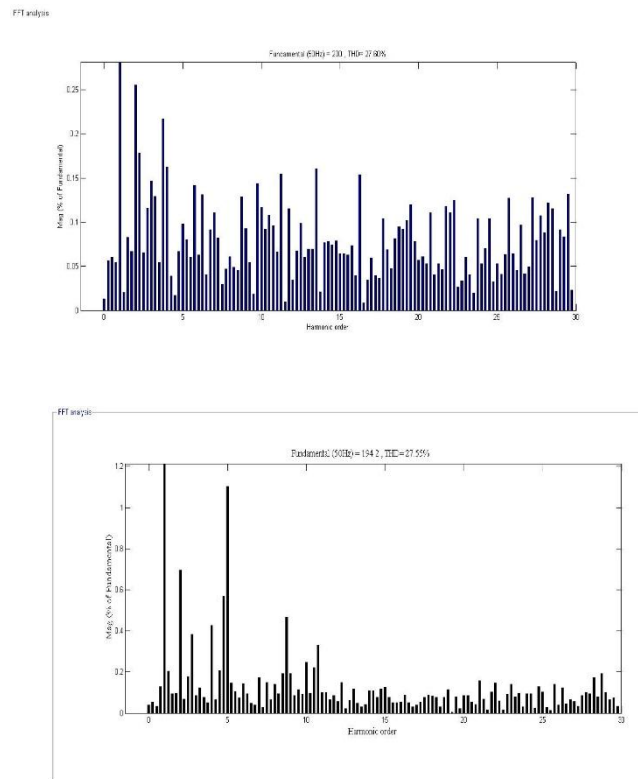


Fig 19: Total Harmonic Distortion of 3 level NPC, Fly Capacitor & Cascaded H-Bridge using SPWM Technique.



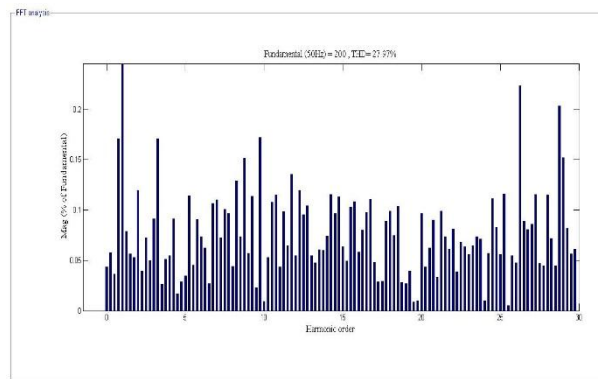


Fig 20: Total Harmonic Distortion of 3 level NPC, Fly Capacitor & Cascaded H-Bridge using SVPWM Technique.

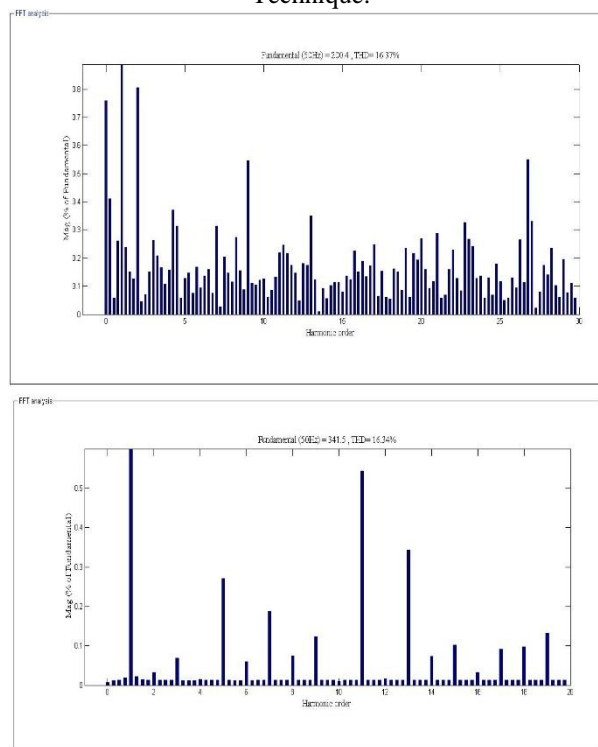


Fig.21.Total Harmonic Distortion of 5 Level Cascaded H-Bridge,NPC Using SPWM Technique

THD TABLES

2 Level	PWM	SPWM	SVPWM
	74.55%	62.83%	47.45%

3 Level	Cascaded H Bridge	NPC	FLY Capacitor
PWM	46.59%	43.69%	43.27%
SPWM	35.54%	35.28%	34.90%
SVPWM	27.97%	27.60%	27.55%

*5 Level *	Cascaded H Bridge	NPC
SPWM	16.37%	16.34%

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IX. Conclusion

The analysis and simulation of all the inverter topologies corresponding to different levels have been made by using three different PWM strategies discussed above. The observations regarding the THD's shows that cascaded H-bridge using SVPWM is the best technique irrespective of cost and size. When compared to the number of levels a 5 level inverter is best suited when compared to the 3 level inverters. Keeping in view the size and cost constraints, a cascaded H-bridge with more levels using SVPWM would serve the best. Moreover it is concluded that with the increase in the number of levels the THD decreases.

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