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Simplified Analogue Realization of the Digital Direct Synthesis (DDS) Technique for Signal Generation

Patrick O. Olabisi[1], Prof B. J. Olufeagba[2]
[1]*Bells University of Technology, Ota, Nigeria.*
[2]*University of Ilorin, Ilorin, Nigeria.*

Abstract: *The design of signal generators has evolved through various analog techniques and in the recent years has seen the adoption of digital design methods owing to tremendous advantages that digital methods offer over analog. This work studied Direct Digital Synthesis (DDS) technique and the implementation was done using simplified yet innovative approach to realize the memory data storage of signal points on look-up tables in a PROM and also the DAC.*
Keywords: *Digital Direct Synthesis (DDS), Functions, Look-up Table, Multiplexer, DAC.*

I. Introduction:

Digital technique has become popular in the twenty-first century so much that it is positively affecting all facets of our lives, considering its enormous advantages. In signal generation, particularly function generators, digital techniques are taking over the stage in the generation of various signal waveform patterns ranging from the normal waveforms of square, sinusoidal, triangular and sawtooth waveforms to specialize waveforms like the modulation waveforms (AM, FM, ASK, FSK, etc) and other waveform functions like the ramp, unramped, sweeping, arbitrary, TTL pulse, CMOS pulse waveforms, and so on.

Digital function generators offer such advantages over their analogue counterparts as higher frequency stability and accuracy, ability to generate much wider spectrum of standard and designer-specified programmable waveforms, higher spectral purity, low phase noise and excellent frequency agility accompanying the use of digital filters that can be realized through software incorporated into the micro-controller and programmable memory chips.

The digital function generators fundamentally use digital to analogue converter (DAC) to generate wave shapes from values stored in a memory, such that any waveform can be synthesized from the digital values stored in such memory. Digital synthesis of waveforms is applied in various electronic, computer and telecommunication devices and other related signals equipment. For example, digital synthesis of sine wave is employed in so many systems ranging from telephone signaling and switching systems, modems, electrical and electronic instrumentations to measuring equipment.

A variety of digital signal processing techniques have been used to generate various signals digitally, the most versatile of which is the digital signal generating techniques is the Direct Digital Synthesis (DDS) technique.

II. The Direct Digital Synthesis (DDS) Technique

This technique also known as the direct digital frequency synthesis (DDFS) came on board in 1971[(1)]. It simply converts digital numbers stored in a memory into analogue or real signals through conversions by a Digital-to-Analogue Converter (DAC). The DDS technique processes data blocks read from a look-up table in a Programmable Read Only Memory (PROM) to generate a form of frequency-tunable and phase-tunable output signal with reference to a fixed - frequency precision clock source. This technique is used in various signal generators, signal mixers and modulators, local oscillators in transmitters and receiver, sound synthesizers, and so on. It is a technology used by some advanced high-end function generators for waveform generation[(2)].

Some of the major merits of the DDS signal generating technique are summarized as follows[(3,4)]:

1. The tuning resolution can be brought so small as to satisfy any design requirement;
2. The DDS can be used to obtain a variety of high precision waveforms in milli-hertz range;
3. Controlling the frequency and the phase of the output waveform can be done in one sample period. So can be phase modulated;
4. Implementing the DDS relies on integer arithmetic and so can be carried out using any type of micro-controller;
5. Due to the stability of the DDS technique, the need for automatic gain control is ruled out;
6. It has phase continuity making it useful for tunable waveform generators.

The basic DDS shown in figure 1 consists of a numerically controlled oscillator (NCO) coupled with a phase modulator (or accumulator), a block that converts the phase information to amplitude values, a digital-to-analogue converter (DAC) and a low-pass filter [(5)]. It could be noted that the DDS as signal generator is been packaged and now available as single integrated circuit chips generating up to hundreds of megahertz frequencies, example is the full-fledge DDS Analog Devices AD9835 chip used by Electronic Alternatezone to build a 10MHz function generator[(3,6)].

Poole Ian[(7)] indicates that the operation of the DDS can be envisaged more easily by looking at the way the phase angle progresses over the course of one circle of the waveform as shown in figure 2. The progression of the phase around the circle corresponds to progression in the output waveform.

A complete signal cycle (2π rad) is divided into 2^n data points on the phase wheel with each data point rounded off to the nearest number. For n-bits of binary digits, the length of bits of the phase accumulator, all the number representing the signal is stored in the memory look-up table. A large number of points are required for each cycle of the waveform in order to achieve high spectral purity of the output signal. The output frequency, f_o, of a DDS device is determined form the basic equation of the DDS through a phase increment, Δ_{ACC} of the phase accumulator within a sample period T_s. To make a complete cycle, the time period required is given by:

$$T_o = \frac{2^n T_s}{\Delta_{ACC}} = \frac{1}{f_o} \qquad (1)$$

Practically speaking, f_s is the internal reference clock frequency. The tuning step of the accumulator, which determines the smallest tuning of the output frequency if obtained from the product of difference in the phase increment and the output frequency or as a ratio of the sampling frequency and the total number of phase points on the phase wheel, thus[(3)]:

$$\Delta f_{o(min)} = f_o(\Delta_{ACC} + 1) - f_o(\Delta_{ACC})$$

$$= \frac{f_s}{2^n}(\Delta_{ACC} + 1 - \Delta_{ACC})$$

$$= \frac{f_s}{2^n} \qquad (2)$$

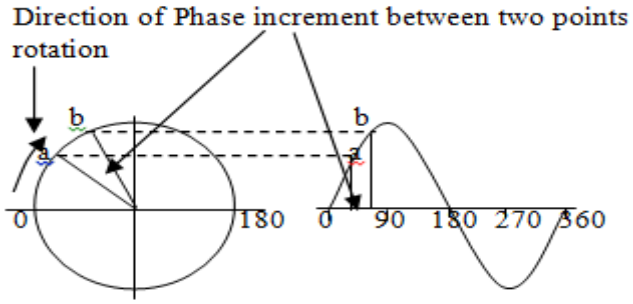

Figure 2: Phase Progression Around a Circle in a DDS.

The frequency tuning word length, n, is given by[(3)]:

$$n = \left[\log_2\left(\frac{f_s}{\Delta f_{omin}}\right) + 0.5\right] \qquad (3)$$

where Δf_{omin} is the minimum frequency that the DDS can generate.

Table 1: Table of Number of bits and the corresponding Phase Increment.

n	**n - bits**	**No. of points**	**Phase increment value**
8	8	256	360/256 = 1.40625
12	12	4096	360/4096 = 0.0878906
16	16	65535	360/65535 = 0.0054932
20	20	1048576	360/1048576 = 0.000343322
24	24	16777216	360/16777216 = 0.000021457
32	32	4294967296	360/4294967296 = 0.000000083
Etc			

III. The Direct Digital Synthesis (DDS) Signal Generator

The DDS signal generator offers substantial performance improvements, at reduced costs, over conventional analog signal generators. It has improved over the years with greater, wider frequency ranges, calibrated output levels, more variety of waveforms, modulation modes, computer interfacing and combination of sweeping or arbitrary functions [8].

Data patterns for different signal waveforms can be stored in the EPROM, which can then be converted by the DAC to generate the required analog signal. For example, if the first half of the table for a signal pattern were filled with zeroes and the second half with values of 100%, then the data represent a square wave. Otherwise, for the sinusoidal waves, the data levels follow what is known as step-wise waveform. Shown in figure is a typical block diagram of the DDS signal generator.

IV. Implementation

The DDS signal generator was implemented for a sinusoid following phase cycle progression shown in figure 2. The phase wheel was divided choosing n = 4 and the following calculation were carried out:
The number of points on the wheel = $2^n = 16$.

The phase increment of the phase accumulator is obtained as follows:

$\Delta_{ACC} = 2\pi/16 = 0.125\pi$ (rad.) or $360/16 = 22.5$ (deg.) (4)

The amplitude could be obtained by calculation or from an accurate plot of the phase wheel in figure 2. Shown on table 3 is the calculated version of the amplitude. For a sine wave, the figures on the second column are the ones actually saved in a look-up table in an EPROM.

Equal Voltage Steps Approach:

During experimentation, the unequal voltage step changes described above was realized. But the realization was clumsy, requiring resistors of various non-standard values to actualize the voltage steps. Subsequently, an approach of partitioning the whole value range into equal voltage steps was adopted so that same value resistors were used in the potential divider network. This also allowed the use of R-R and R-2R ladder networks in the potential divider network, and the equal step values are as shown in column 4 of table 2.

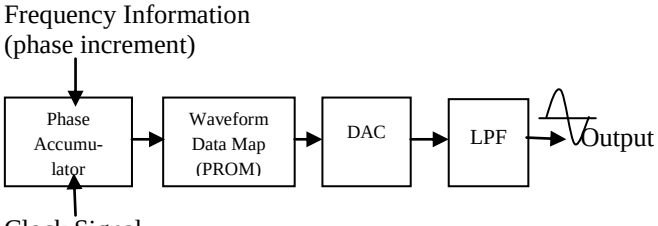

Figure 3: Basic DDS Sine Wave Generator.

Table 2: Phase Increment and Voltage Amplitude per Step.

Cumulative Phase Increment, $\sum_{i=1}^{16} \Delta_{ACC}$	Sine of Phase Increment, $\sin(\Delta_{ACC})$	Stepped Amplitude for Peak-to-Peak of 5volts [2.5 x $\sin(\Delta_{ACC})$ + 2.5] volts	Stepped Amplitude for Equal Difference, [(5/8) = 0.625 volt] Between Steps
0	0	2.5	2.5
22.5	0.3827	3.4568	3.125
45	0.7071	4.2678	3.750
67.5	0.9239	4.8098	4.375
90	1	5.0	5.000
112.5	0.9239	4.8098	4.375
135	0.7071	4.2678	3.750
157.5	0.3827	3.4568	3.125
180	0	2.5	2.5
202.5	-0.3827	1.5433	1.875
225	-0.7071	0.7322	1.250
247.5	-0.9239	0.1903	0.625
270	-1	0.0	0.0
292.5	-0.9239	0.1903	0.625
315	-0.7071	0.7322	1.250
337.5	-0.3827	1.5433	1.875
360	0	2.5	2.5

For the circuitry to realize this technique, use was made of a Texas Instrument sixteen input channels analog multiplexer (CD4067BE)[9,10] to select voltage levels in steps between 0 and 5 volts for a complete cycle using the figures in table 2. Switching through the sixteen input channels was enabled with the operation of a 4–bit Counter (74LS93) [11]., which in itself was clocked with an oscillator. The circuit connection is as shown in figure 3. With a peak-to-peak voltage of 5 volts, the sub-division into the 16 states or levels done with potential divider network as shown in figure 4.

The amplitudes on the rise and on the fall side of the period are the same, e.g. 4.8098 volts just before and just after the 5.0 volts. This enabled the reduction of the number of resistors in the potential divider bank from 16 to 8 resistors. A voltage level was connected to two appropriate channels for selection by the multiplexer. In another version of the implementation, in order to be able to make use of a R-R or R-2R ladder network in-place of 8 resistors in the potential-divider network, the amplitude difference between every two steps was made the same as shown on column four of table 2.

V. Output Waveform:

The output step-wise waveform from which sine wave can be synthesized is shown in figure 6 as captured on the oscilloscope.

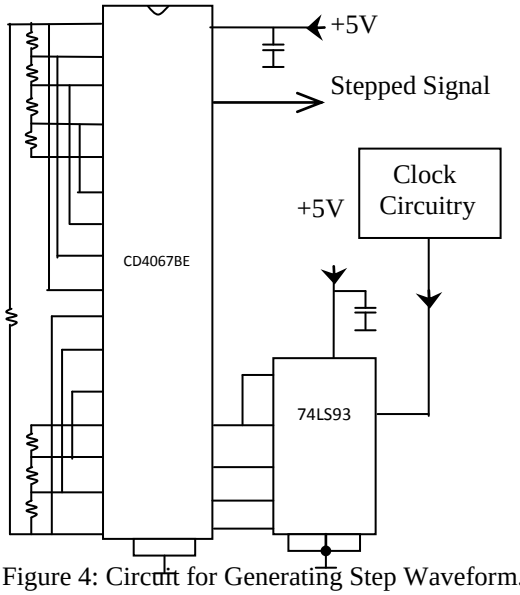

Figure 4: Circuit for Generating Step Waveform.

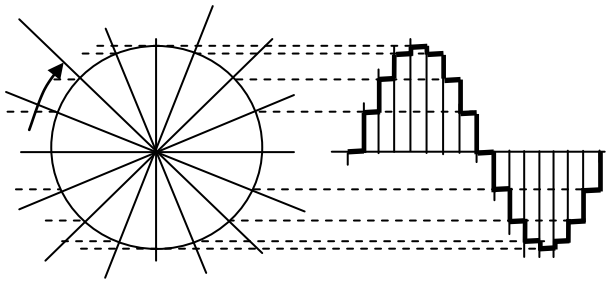

Figure 5: Stepped Amplitudes for Sine Wave Synthesis

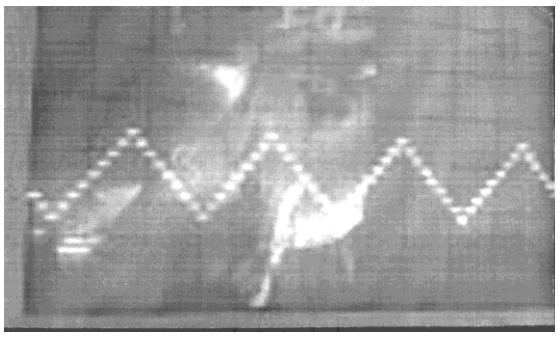

Figure 6: Equal Amplitude Stepped Output Waveform

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