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Improved Pulse –Width Modulation Strategies for Voltage Source Inverter

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Abstract: *The power electronics are gaining more popularity because of their user friendly behavior. Here the recently proposed improved PWM strategies are compared and the performances in the field of harmonic reduction are traced out. The strategies one prior to other helps in reducing the harmonics and gives the topology a major breakthrough in the field of voltage source inverters. The diode assisted buck-boost voltage source inverter with the recently proposed improved strategies enhances the voltage boost capability with a low boost duty ratio. The efficient use of the intermediate DC-link voltage by the two improved strategies achieves high gain and alleviates the stresses occurring across the switches in the circuit. The work exposes the performance of the respective strategies with help of the harmonic spectra and graphs are drawn to analyze the dependence of the THD with the variation of the load inductance and the duty ratios.*

Keywords: *PWM Strategies, DC-Link Voltage, THD, Voltage Source Inverter, Conduction Losses.*

I. Introduction

Recent trends to reduce greenhouse gas (GHG) emission made the new generation capacity can no longer be met by traditional power generation methods of burning primary fuel sources such as coal, oil, natural gas, etc., but the traditional sources are predicted to last only about 100 to 200 years in the world. In addition, nuclear power plants experienced safety problems like decomposition of nuclear waste due to radioactive rays .These facts made renewable energy have come of age. Distributed generation (DG) technologies provide a potential solution of increasing generation capacity for renewable energy systems. DG systems are usually small modular devices with increased security and reliability, and are close to electricity users with improved power quality due to short transmission lines. Such systems need dc-ac converters or inverters as an interface between their single-phase loads and sources, and often have a wide range of input voltage variations due to the uncertainties of energy sources, which imposes stringent requirements for inverter.

Interest in buck-boost inverters has grown notably with the development of sustainable energy systems in recent years. Renewable energy from the wind, sun, water, wave, tidal, etc., is inexhaustible but irregular and fluctuates dramatically with the weather and season. Thus the buck boosts inverter with improved strategies function as a power system conditioner. The diode-assisted buck–boost VSI further extends the voltage transfer ratio and avoids the extreme duty ratio of switching device in the front boost circuit for the wide range buck and boost power conversion .The topology shown in Fig 1integrates an X-shaped diode-assisted capacitor network between the boost inductor and the inverter bridge [1]-[4]. Since the diodes in the network are naturally conducting to perform parallel capacitive charging and are reverse-biased in the next interval to realize series capacitive discharging, the relatively high voltage in the dc-link of the inverter bridge. Here two distinct modulation schemes are compared with the first gaining a better symmetrical waveform quality and the second gaining a lower commutation count without stressing the active and passive.

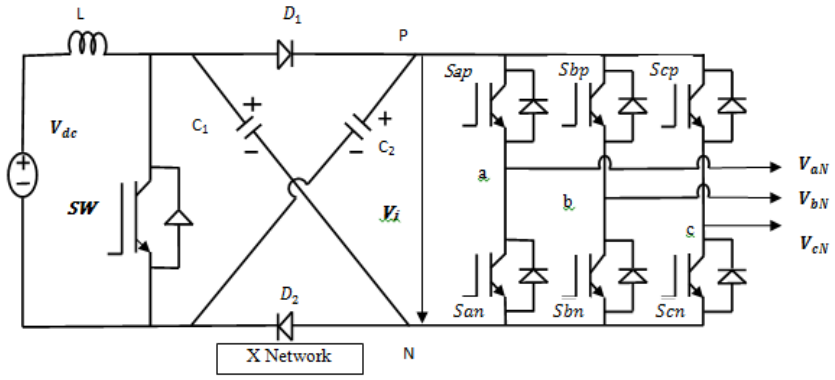

Fig.1.Diode-assisted buck–boost VSI with diode-capacitor network

The diode-assisted capacitor network introduces an instantaneous intermediate dc-link voltage change of the inverter bridge in one switching time period. However, the PWM strategies [1] presented just utilize active vectors for ac output in the duration when the two capacitors are connected in series. When the switching device S1 is turned OFF, the two capacitors is connected in parallel through two forward-biased diodes and the intermediate dc-link voltage $V_i$is the same as the capacitor voltage. During this interval, the three-phase VSI operates in null state and output ac voltage is zero. In view of the variable intermediate dc-link voltage of the inverter bridge in one switching time period, sufficient utilization of intermediate dc- link voltage can improve the voltage- transfer ratio and reduce the voltage rating of the capacitors. This paper mainly examines the possibilities of the inverter in employing it as an efficient drive for the future motor applications. It analyzes the THD values for the modulation strategies named IPWM1 and IPWM2 separately.

II. Working Principle With Equivalent Circuit

Diode assisted buck-boost inverter uses a voltage boost circuitry to boost its dc input voltage by controlling the conductive duty ratio of switch SW. Mathematically, by performing state-space averaging, it can easily be shown that the capacitor voltage V_C and peak ac output voltage $\hat{v}$ of the inverter can explicitly be expressed as,

$$V_c = \frac{1}{(1-k)} V_{dc} \hat{v} = M \frac{1}{2(1-k)} V_{dc} \qquad (1)$$

Where k refers to the conductive duty ratio of SW, M represents the modulation index and 1/ (1−k) is defined as the voltage boost factor. The values of k and M are tuned accordingly to step down or up the inverter AC output voltage with respect to the applied input voltage, which also affects the voltage stresses appearing across switches SW, SX, and SX' (X =A, B, or C), expressed as V_c. The inverter can theoretically attain an infinite gain; practical parasitic imperfections generally limit its maximum gain to a finite value. In addition to this limitation of maximum gain, its associated large k is expected to stress the switches considerably, since they are now forced to turn OFF and then ON within short time duration. To produce a higher gain, while avoiding the use of a large k, the diode-assisted inverter shown in Fig.1where a diode-capacitor network replaces the single dc capacitor placed between SW and the three-phase VSI Bridge. By turning ON SW, the diodes become reverse –biased and the inductive current i_L flows solely from the dc source to boost the magnetic energy stored in inductor L according to the equivalent circuit shown in Fig.2. Besides inductive charging, capacitors $C_1$and C_2 are found to be in parallel.

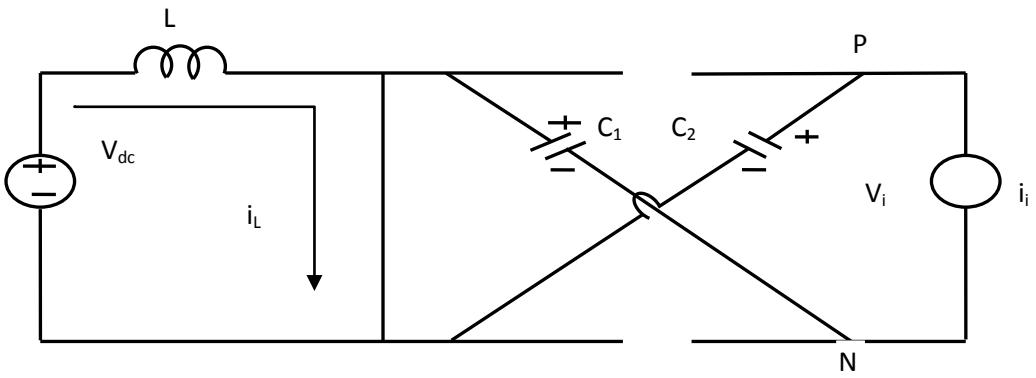

Fig. 2. Equivalent circuits diode-assisted inverter when SW is turned ON

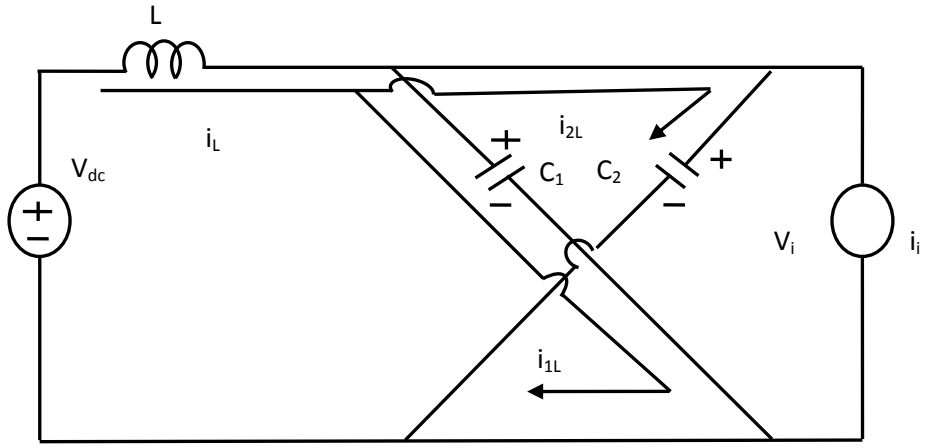

Fig. 3. Equivalent circuits diode-assisted inverter when SW is turned OFF

Having a larger DC-link voltage now also means the switches SX and SX' (X= A, B, and C) in the rear-end three-phase bridge have to block a higher voltage, expressed as $2V_C$.

$$v_i = v_{c1} + v_{c2} = 2v_c; (C_{1=}C_2 = C) \quad (2)$$

On the other hand, with SW turned OFF, the inductor current i_L flows through the diode–capacitor network according to the equivalent circuit shown in Fig. 3, where diodes $D_1$and D_2 are now forward-biased to connect C_1 and C_2 in series.

$$v_i = v_{c1} = v_{c2} = v_c; (C_{1=}C_2 = C) \quad (3)$$

Therefore, quite intuitively, for producing a higher voltage gain, the inverter active states (six in total) must be placed only within the SW=ON interval. In contrast, inverter null states (two in total) are not restricted, meaning that they can occupy either the SW=ON or SW=OFF interval without transferring the discretely varying dc-link voltage pattern to the ac load, since null states give rise to zero line voltages (ZLVs) regardless of the dc-link voltage variation. For deriving the inverter voltage transfer gain expression, steady-state constraints applied to the inductor L are analyzed with the inductive current i_L observed to rise with a slope of V_{dc}/L during the SW=ON interval and fall with a slope of $-(V_C-V_{dc})/L$ during the SW=OFF interval. Equating the incremental rise and fall of i_L during the two intervals in a switching period T, voltage V_C across each capacitor can be derived as

$$\frac{V_{dc}}{L} kT = \frac{V_C - V_{dc}}{L}(1-k)T \quad (4)$$

Comparing (4) and (2), the ac output voltage of the diode assisted buck-boost inverter is observed to experience a voltage boost, assuming that all control parameters are set equally. Thus the inverter is therefore suitable for use in those buck–boost applications where a bias towards higher voltage boost is needed.

III. Comparison Of The Strategies

3.1. Improved PWM strategy (IPWM1)

In this PWM strategy, the switching frequency of each power devices is *fs* (*fs*=1/*Ts)*.Obviously, the small vectors are not included in the interval of S1 = OFF. The voltage stress across the SW is *Vsf and* is the same as the capacitor voltage V_c. *Vsi* is the voltage stress across the switching devices in the inverter stage which is twice the capacitor voltage ($2V_c$).The arrangement of voltage vectors in the first sextant for IPWM1 is shown in Fig.4. The interval of S1=ON is inserted symmetrically in the center between the OFF intervals in the switching interval $2T_s$. Since S1 turns ON and OFF once per two switching time periods, there is one advantage that the

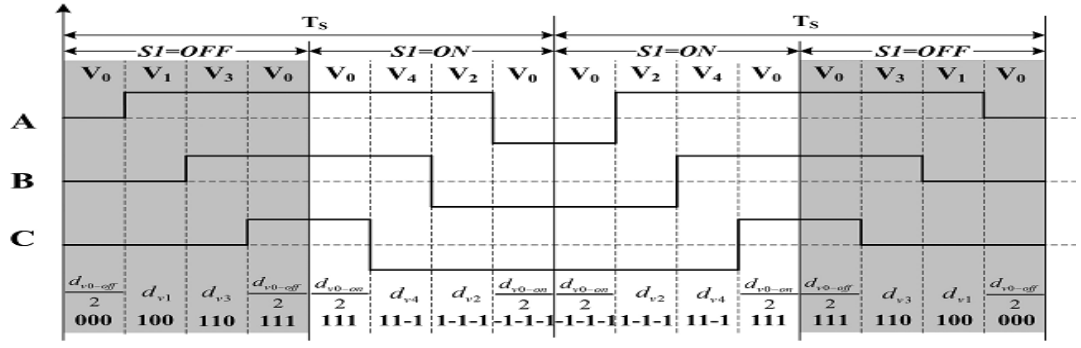

Fig.4. Sequences of voltage vectors in the first sextant for IPWM1

switching loss of power devices in the front boost circuit can be reduced by half and S1 is also commanded in null states of the inverter stage during which the equivalent output ac voltage is zero. With IPWM1, the switching frequency of power devices in the front boost circuit and inverter bridge is fs/2 and fs, respectively. This control method is referred as the first improved PWM strategy (IPWM1) in this study.

3.1.1 Realization of IPWM1

The output reference vector V_r can be synthesized by using vectorsV1, V2, V3, and V4 for IPWM1 in the first sextant.

$$\left.\begin{aligned} d_{v1} &= \mathrm{k_s}.\ \sin(\frac{\pi}{3}-\theta).\mathrm{k_{off}}.\mathrm{T_s} \\ d_{v1} &= \mathrm{k_s}.\sin(\theta).\mathrm{k_{off}}.\mathrm{T_s} \\ d_{v2} &= \mathrm{k_s}.\ \sin(\frac{\pi}{3}-\theta).\mathrm{k_{on}}.\mathrm{T_s} \\ d_{v4} &= \mathrm{k_s}.\sin(\theta).\mathrm{k_{on}}.\mathrm{T_s} \\ d_{v0-off} &= (1-\mathrm{k_s}.\ \sin(\frac{\pi}{3}+\theta)).\mathrm{k_{off}}.\mathrm{T_s} \\ d_{v0-on} &= (1-\mathrm{k_s}.\ \sin(\frac{\pi}{3}+\theta)).\mathrm{k_{on}}.\mathrm{T_s} \end{aligned}\right\} \quad (5)$$

$$k_s = \frac{M_{iout}}{M_{imax}} \quad (6)$$

By solving the Equation (5) gives the IPWM1 strategy, in which k_{on} gives the duty ratio at SW=ON, k_{off} gives the duty ratio at SW=OFF and T_s gives the switching time period.M_{iout} is the amplitude of the output reference vector Vr, M_{emax} is the obtainable maximum amplitude of the voltage vector with existing PWM strategy by using large voltage vectors, M_{imax} is the obtainable maximum amplitude of the voltage vector with two kinds of improvedPWMStrategies

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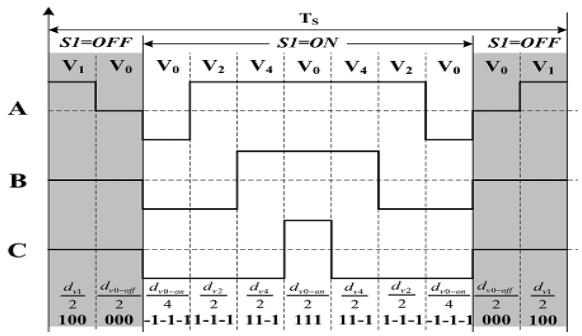


Fig.5. Sequences of voltage vectors in the first sextant for IPWM2. IPWM2 in zone A

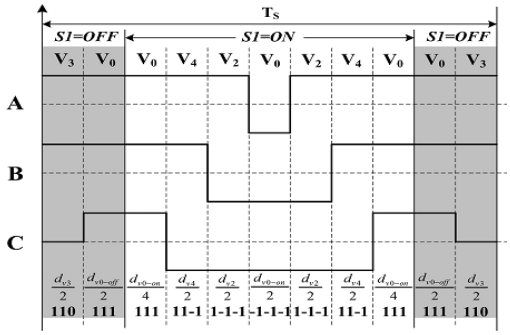


Fig.6.Sequences of voltage vectors in the first sextant for IPWM2. IPWM2 in zone

3.2. Improved PWM strategy (IPWM2)

In order to minimize the half-switching-frequency harmonics distortion, the second improved PWM strategy referred as IPWM2 is presented which ensures symmetrical placement of switching states in one switching time period. In the second improved strategy (IPWM2) the first sextant is divided into two zones A and B. The feature of this modulation strategy is that S1 turns ON and OFF once with S1=ON interval symmetrically inserted at the center of one switching time period T_s. The small vector V1 introduces an additional switching state. Therefore, IPWM2 introduces one more switching action in one phase leg of the inverter bridge in the interval of S1=OFF. With IPWM2, the equivalent switching frequency of power devices in the inverter bridge is (1+1/6) f_s.

3.2.1 Realization of IPWM2

To synthesize the reference vector (Vr) in zone A, active switching vectors (V1, V2, andV4) are used and all the vectors are symmetrically distributed during one switching time period as shown in Fig.5. Similarly, to synthesize the reference vector V_r in zone B, active switching vectors (V_2, V_3, and V_4) are used as shown in Fig. 6. With the same design approach, the switching states in other sextants can be obtained.

$$\left.\begin{aligned} d_{v1} &= \mathrm{k_s}\,.\,\mathrm{k_{off}}\,.\,\mathrm{T_s} \\ d_{v0-off} &= (1-\mathrm{k_s})\,.\,\mathrm{k_{off}}\,.\,\mathrm{T_s} \\ d_{v2} &= \left(\frac{1+\mathrm{k_{on}}}{2}\ \sin(\frac{\pi}{3}-\theta) - \frac{1}{2}\mathrm{k_{off}}\right)\,.\,\mathrm{k_s}.\,\mathrm{T_s} \\ d_{v4} &= \frac{1+\mathrm{k_{on}}}{2}.\sin(\theta).\,\mathrm{k_s}.\,\mathrm{T_s} \\ d_{v0-on} &= \left(\mathrm{k_{on}} - \frac{1+\mathrm{k_{on}}}{2}\ \sin(\frac{\pi}{3}+\theta).\,\mathrm{k_s} + \frac{1}{2}\mathrm{k_s}.\,\mathrm{k_{off}}\right)\,.\,\mathrm{T_s} \end{aligned}\right\} \quad (7)$$

Solution of the above Equations gives the IPWM2 strategy.

IV. Simulation Results forImproved Strategies

The Diode assisted buck-boost inverter structure is simulated using MATLAB/SIMULINK to verify the improved PWM strategies. The specifications of the components and devices used in the circuit are given in the TABLE1.The circuit is simulated for various duty cycles are tabulated in TABLE 2.Comparison of two strategies have been done by varying the duty cycle (TABLE 2) and the load value (TABLE 3). THD values are less for IPWM2 as compared to the IPWM1 which clarifies that the performance of the IPWM2 will be prior to the IPWM1.

Table 1.Specifications of the setup

SWITCHING DEVICE	SW	IGBT (IGW40T120)
	Sap,San,Sbp,Sbn, Scp,Scn	IGBT (IGW25N120) and DIODE (IDP18E120)
INDUCTOR	L	4mH
DIODE-CAPACITOR NETWORK	D1 and D2	DIODE
	C1 AND C2	500µF
FILTER CIRCUIT	L_f	400µH
	C_f	35µF
RL LOAD	R	40Ω
	L	2mH
SWITCHING TIME PERIOD	T_s	100 µs
SOFTWARE	MATLAB/SIMULINK 8.0	

Table 2. Corresponding THD value for various duty cycles

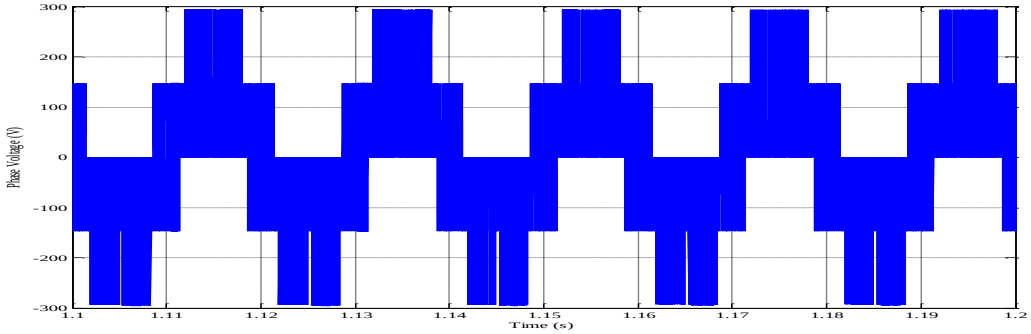
Duty cycle	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1
IPWM1 THD in %	17.04	16.73	17.41	18.75	20.12	21.14	23.00	29.93	37.80	37.80
IPWM2 THD in %	14.73	14.48	14.97	16.24	17.73	18.73	20.79	27.93	35.76	35.76

Table 3. THD for various loads

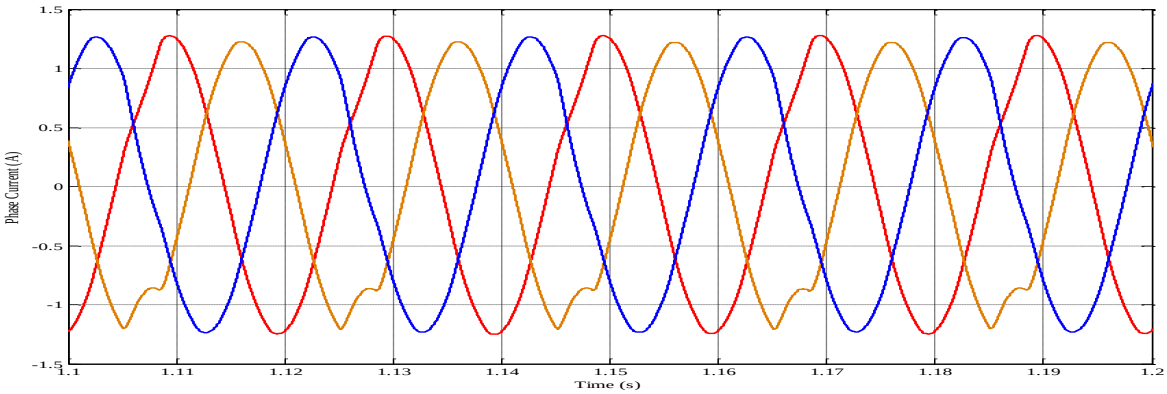
L in mH	2	4	6	8	10
IPWM1 THD in %	21.14	21.17	21.20	21.24	21.27
IPWM2 THD in %	18.73	18.74	18.75	18.77	18.79

The above tables explain the performance of the two strategies that has been mentioned in the paper. In the Table1, the experimental setup has been given. In the Table 2, the THD % has been taken to the performance between IPWM1 and IPWM2.In the Table 3, the inductance value of the load is varied to get the corresponding THD value for the inductance value.

4.1. Simulation results for the improved strategy 1(IPWM1)



(a)



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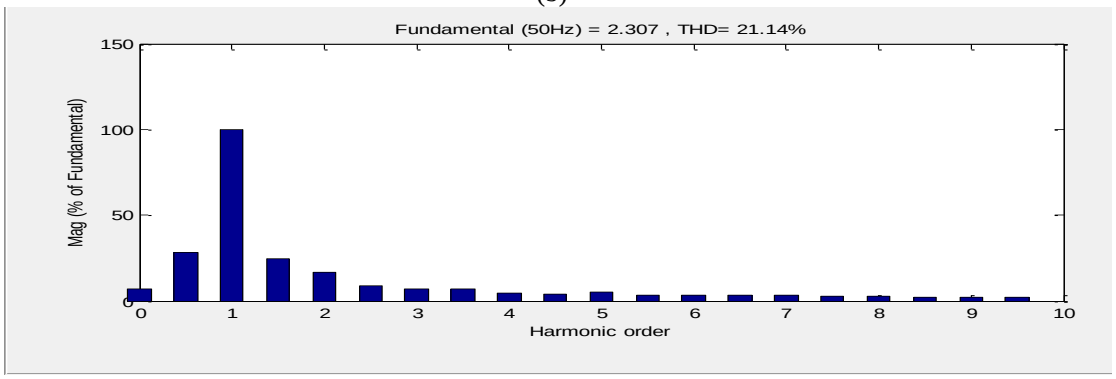
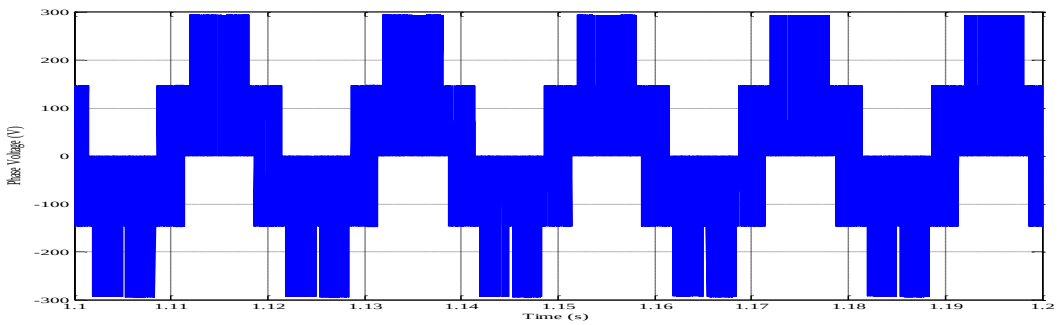
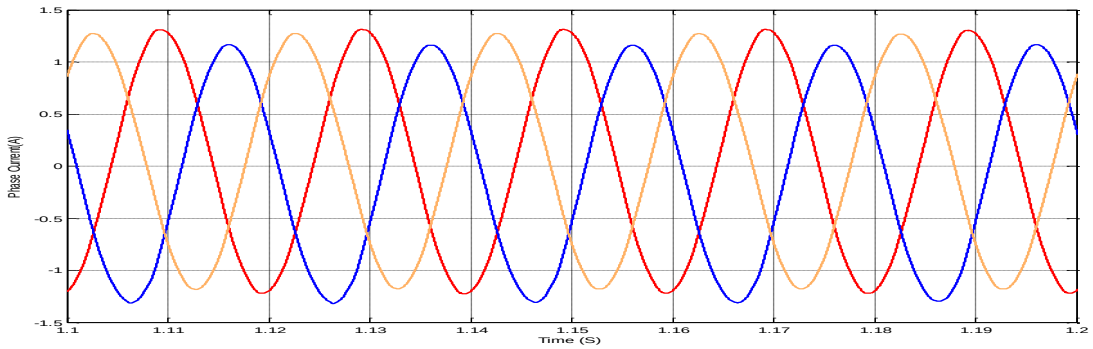


(c)

Fig.7. Simulation waveforms of IPWM1 with (*k*on = 0.5, and Vdc = 100 V). (a)Output phase voltage. (b)Output line current. (c) Harmonic spectrum

4.2. Simulation results for the improved strategy 2(IPWM2)





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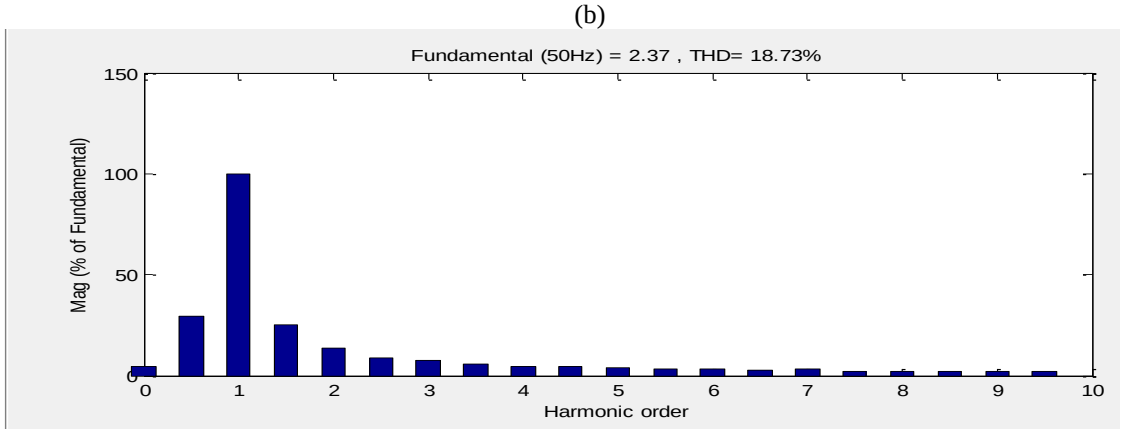

(c)

Fig.8.Simulation waveforms of IPWM2 with (*k*on = 0.5, and Vdc = 100 V). (a)Output phase voltage. (b)Output line current. (c) Harmonic spectrum.

4.3. Simulation diagram for the Diode Assisted Buck-Boost Inverter Using IPWM Strategies.

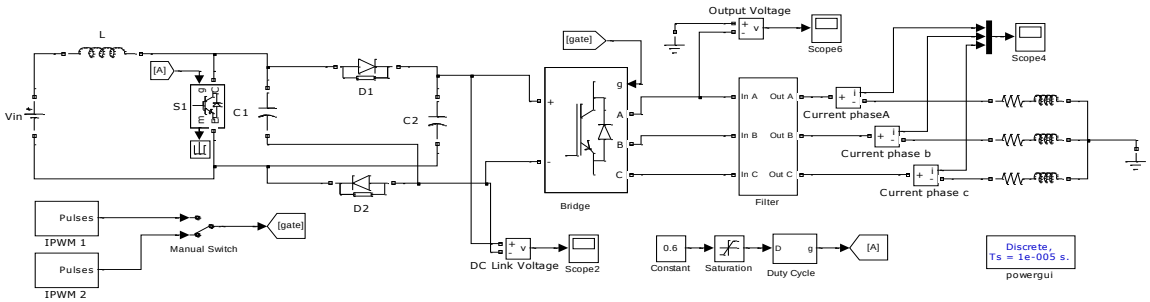

Fig.9.Simulation circuit for the diode assisted buck-boost VSI.

4.4. Graph showing the THD spectrum of IPWM 1&2 v/s Duty Ratio

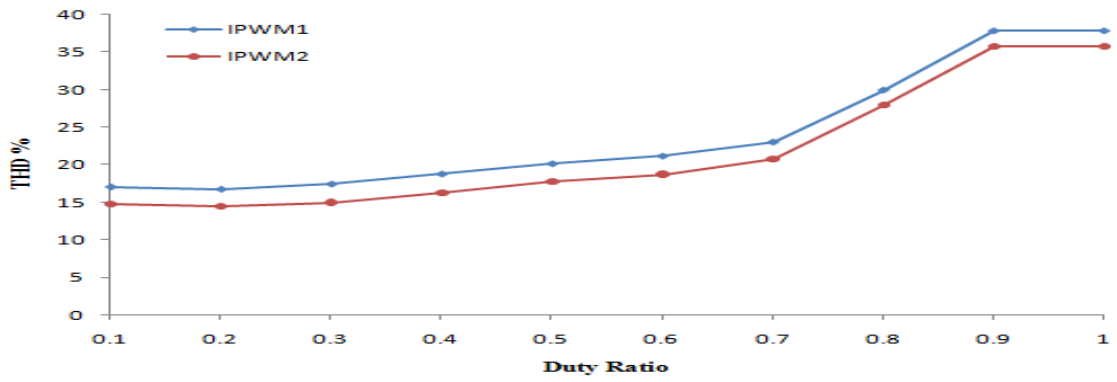

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Fig.10.THD versus Duty Ratio for the improved strategies

4.5. Graph showing the THD spectrum of IPWM 1&2 v/s Load inductance

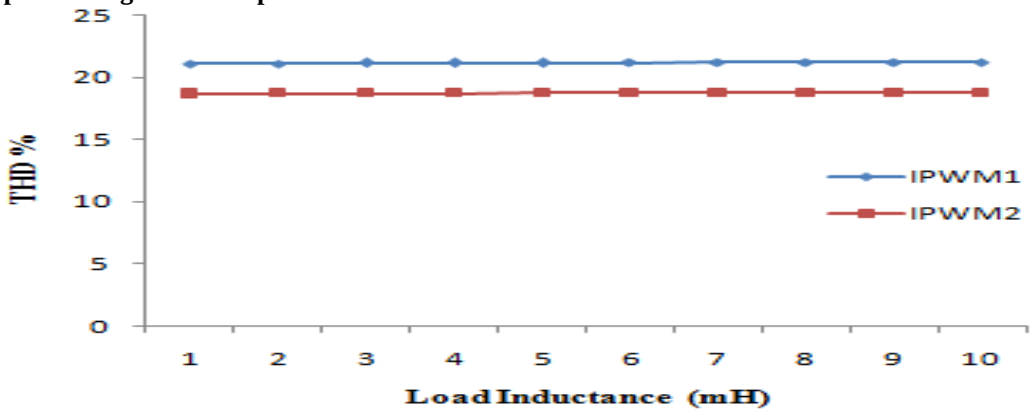

Fig.11.THD versus Load Inductance values for the improved strategies

Table 4. Corresponding THD value for various duty cycles for the motor load

Dutycycle		0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1
IPWM1 THD in %	With RL load	17.04	16.73	17.41	18.75	20.12	21.14	23.00	29.93	37.80	37.80
	With MOTOR load	18.52	19.52	20.21	20.60	18.73	15.93	18.16	23.45	27.11	27.11
IPWM2 THD in %	With RL load	14.73	14.48	14.97	16.24	17.73	18.73	20.79	27.93	35.76	35.76
	With MOTOR load	13.75	15.23	16.33	16.70	14.61	10.83	12.69	19.31	25.02	25.02

4.6. Graph showing the THD spectrum of IPWM 1&2 v/s Duty Ratio

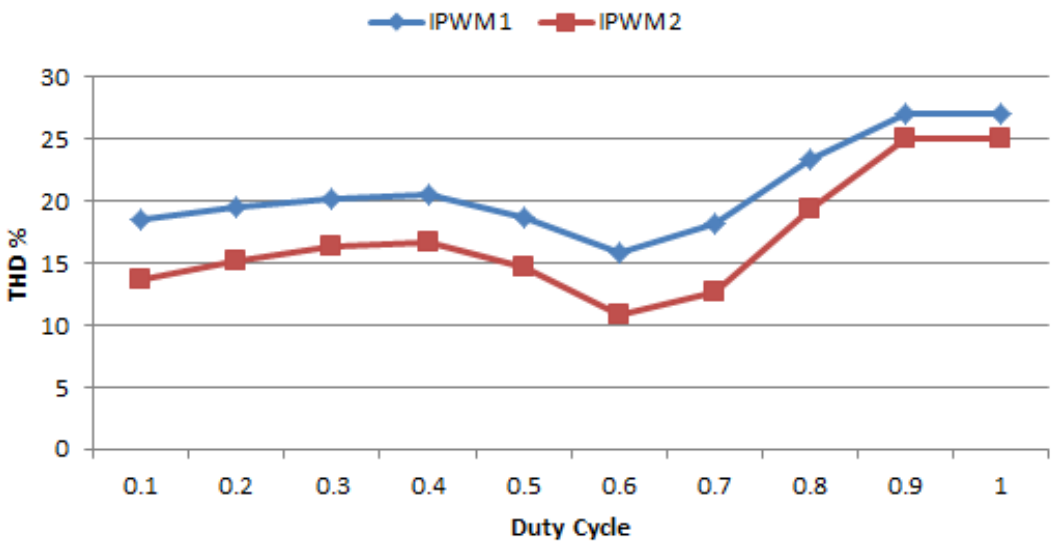

Fig.12.THD versus duty ratio values for the improved strategies with motor load

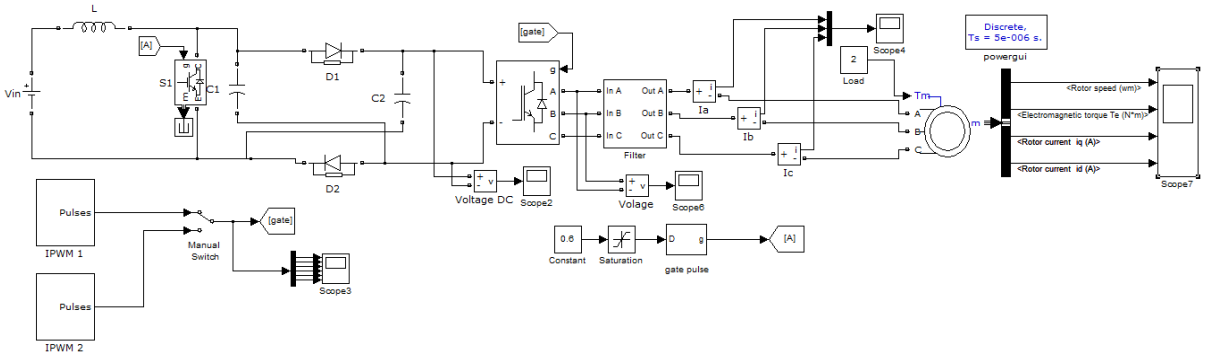

Fig.13.Simulation circuit for the diode assisted buck-boost VSI with motor load.

Fig.13 shows the simulation diagram of the respective VSI which uses the motor load. Performance analysis has been done and THD values collected from the FFT analysis are tabulated(Table 4).It is evident that the motor load gives less value of THD at the duty ratio 0.6.

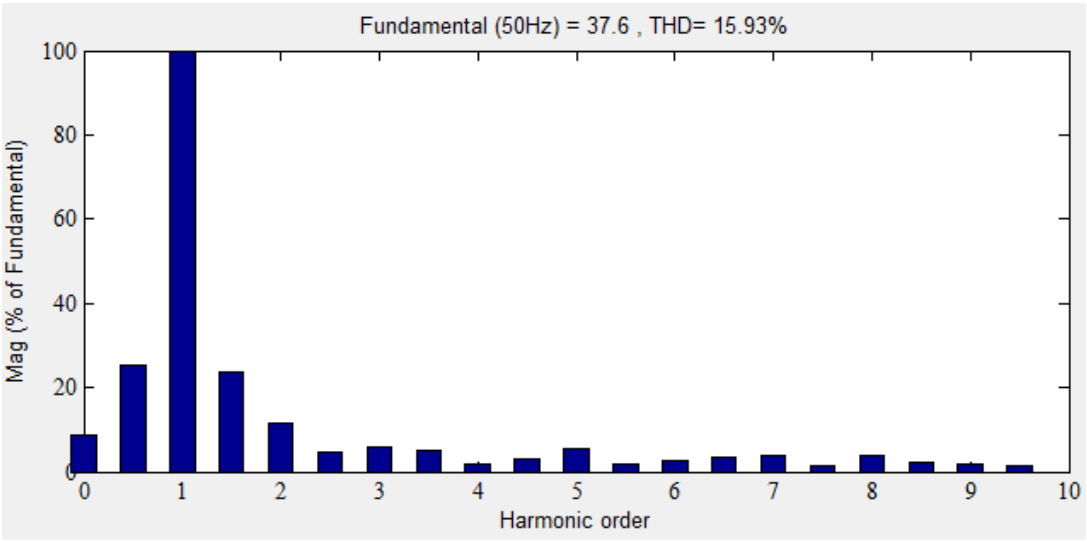

Fig.14.Harmonic spectrum of IPWM1 with *k*on = 0.6, and Vdc = 100 V

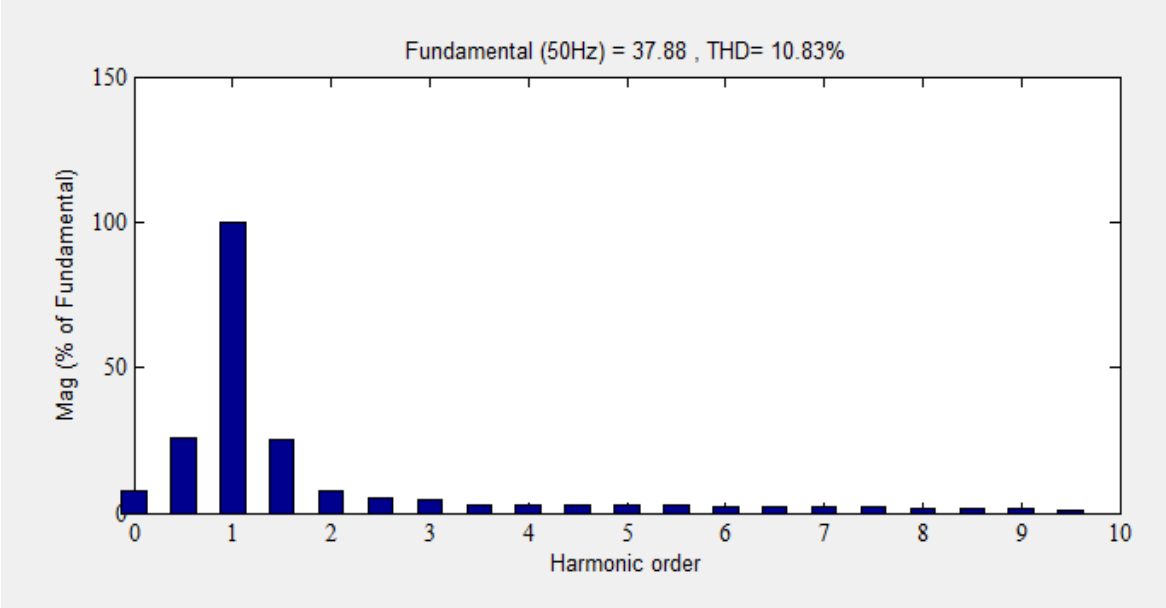

Fig.15. Harmonic spectrum of IPWM2 with *k*on = 0.6, and Vdc = 100 V

V. Conclusion

Initially, the paper analyses the working of the diode assisted buck-boost voltage source inverter using the two improved strategies IPWM1 and IPWM2, its realization and the generation. The improved strategies reduce the conduction losses of the switch. This paper mainly compares the performances of IPWM1 and IPWM2 and various analysis has been done in the field of harmonics. From the spectrum itself it is clear that the improved strategies can perform well that the old existing ones. Simulation results and the harmonic spectrum are given for both motor and RL loads to distinguish the two strategies. Usage of this inverter in the field of the motor drives is also investigated theoretically using the motor as load in the place of RL load. With the results we can conclude that the improved strategies are advantageous and it gives high gain with low boost duty ratio for both RL and Motor load. The strategies are applicable for the control of the AC drives used in the industrial applications like elevator industry.

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