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Optimization of Power Consumption in VLSI Circuit

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Abstract: *Increasing speed and complexity of design gives a significant increase in power consumption in VLSI chips. Speed, power consumption and space are major issues in VLSI circuit. To meet these challenges there are certain design techniques which are used to reduce power. Optimization of power can be done by considering various components such as transistor sizing, voltage scaling, variable V_{DD}, multiple threshold voltages, voltage islands, power gating, long channel transistor, stacking & parking states and logic styles etc. Power consumption in VLSI circuit is data dependent. In this paper different design methods are tested to optimize the power. It is found that algorithm based design reduces gate switching activity that results reduction of power in multiplier circuit.*

Keyword: *Transistor sizing, voltage scaling, variable V_{DD}, multiple threshold voltages, voltage islands, long channel transistor, stacking & parking states, logic styles, Genetic algorithm, Booth multiplication*

I. Introduction

Reduction in power dissipation is an important design issue in VLSI circuits. The design parameters have major effect on the overall performance of the system. On the basis of component used and their function different optimization techniques can be used. For example in case of multiplier power consumption depends upon data. This is because switching contributes to more power consumption. This can be optimized by using various gate combinations. Gate switching can be reduced by using algoritms. For example of in case of multiplier design method Booth algorithm as well as modified Booth algorithm can be used for efficient multiplication. In this paper various approaches are used for power consumption eg. transistor sizing, voltage scaling, variable V_{DD}, multiple threshold voltages, voltage islands, long channel transistor, stacking& parking states, logic styles, Genetic algorithm, Booth multiplication etc.

This paper is divided into five sections. First section is of introduction. Second section is about preliminary studies. Third section includes different design methods and their testing. Fourth section is of comparison with discussion. Finally, fifth section is conclusion of the work reported here.

II. Preliminaries

2.1 Power Dissipation

In case of VLSI circuits power dissipation is of two types' i.e. static power dissipation and dynamic power dissipation. This is shown as under:-

1. Static Power Dissipation
2. Dynamic Power Dissipiation

Static power dissipation is due to three major factors as leakage current, sub threshold current of transistors and tunnelling effect of current. So optimization can be achieved by concentrating all these design issues. As we know that MOS transistor has two P-N junctions: one is between source and drain and other is between drain and source. When source substrate junction or drain substrate junction is reversed biased. The leakage current flows through reverse biased P-N junctions. Generally this leakage current is very small in magnitude so we ignore this current.

Leakage current is temperature dependent. This is because leakage current is caused by thermally generated carriers. With increase in temperature, leakage current increases. According to a survey it is found that it becomes double for every 10^0C rise in temperature. From this it is clear that temperature of a circuit must be controlled at any cost.

1.1 Sub threshold current of transistors

At VGS = V_T surface is said to be inverted. In this condition there is strong inversion and conduction takes place afterwards. But practically $V_{GS} < V_T$. MOS transistor is under sub threshold or weak inversion conduction. This current is equally small in magnitude and rises exponentially. This current flows from drain to source. It is observed at V_{GS}=0.

If V_T is nearly zero volt. Then threshold leakage current will be more. From this it is clear that if threshold voltage is less leakage current will be more. Hence $(PD)_{static}$ will also be more. The threshold voltage has to keep high.

As $(P_D)_{static} = P(t) = i_{DD}(t)\, V_{DD}$

Here $i_{DD}(t)$ is the leakage current or static current and V_{DD} is supply voltage. From this it is clear that if leakage current increases, then static power increases. Hence threshold voltage represents a trade off between performance and static power dissipiation.

2.2 Tunnelling Current Effect

As gate oxide material is SiO_2 and SiO_2 is very good dielectric. The leakage current through this good dielectric is very low. But if the thickness of dielectric is very less. Then electrons can tunnel through this dielectric. If the thickness of dielectric decreases tunnelling effect increases.

2.3 Dynamic Power Dissipiation

Dynamic power dissipiation occurs in charging and discharging of capacitive loads. Let C_L is the capacitive load. If this capacitive load is switched between ground and V_{DD} and switching frequency is taken as $(f)_{switching}$ then charging of load taken takes place for T $(f)_{switching}$ time and discharging also takes place for same time, T being the time interval.

During charging current flows from V_{DD} to C_L and during discharging current flows from C_L to V_{DD}. Total charge transferred from positive supply rail (V_{DD}) to negative supply rail (ground) during charging and discharging cycle will be:-

$Q = C_L\, V_{DD}$

So $(P_D)_{Dynamic} = \frac{1}{T}\int_0^T i_{DD}(t)\, V_{DD}\, dt = \frac{VDD}{T}\int_0^T i_{DD}(t)\, dt$

$= \frac{1}{T} V_{DD}[\, T(f)_{switching}\, C_L\, V_{DD}]$

$= C_L V_{DD}^{\,2} (f)_{switching}$

$(P_D)_{Total} = (PD)_{switching} + (P_D)_{dynamic}$

Usually $(PD)_{Total}$ can be ignored but high sub threshold current if exist, then it cannot be ignored. But $(P_D)_{dynamic}$ is far greater than $(PD)_{static}$ hence it cannot be ignored.

At this short span of time, rail to rail current flows and causes power dissipiation which can not be avoided.

Table 1

Sources to bear power dissipiation
Air cooled system
Heat sinks
Liquid cooling

Dynamic power dissipiation affects the battery when the device is in active mode but static power battery life even when the device is in sleep mode.

Power Dissipation Estimation

In all logic circuits power consumption is related to information transfer and each circuit have inherent requirement of information transfer. Let R is transfer rate requirement for a given architecture. The lower bound of this rate may be determined which can be used for power dissipiation estimation. The different architecture can perform same function but may have different information transfer rate and channel capacity. The channel capacity can be given as under:-

$$C = \int_0^W \log_2[1 + SNR(f)]\, df$$

Here SNR stands for signal to noise ratio. For any transfer, capacity should be greater than or equal to R. The overall power in digital circuit is a function of signal power, temperature and semiconducting property etc. However power dissipiation is mainly due to ground bounce. The lower bound of power dissipiation can be calculated using information transfer capacity of channel. Let R be the required information transfer rate, W is the channel bandwidth & C is the channel capacity. Lower bound of power dissipiation can be given as:-

$$P_{D1,min,sen} = C_L \left(2^{\frac{R}{W}} - 1\right) \& \sigma_N^2 W$$

III. Design methods for optimisation

3.1 Power Optimization as Data dependent

Complexity of data contributes to switching activity in the circuit. With the use of efficient algorithm design component of circuit can be reduced. By the application of simulation to standard design and comparing

it with optimization better design component can be found. Gate switching for all initial states and all inputs can be simulated to analyse power consumption. Data dependency is helpful in gate design complexity. Ordering of gate inputs affect both power and delay. Prasad [1] has described methods to optimize the power and/or delay of logic gates based on transistor reordering. So, considerable improvements in power and delay can be obtained by proper ordering of transistors. For instance, late arriving signals can be placed closer to the output to minimize gate propagation delay. Another approach to reduce power is to consider the size of gate, which has significant impact on circuit delay and power dissipation. By increasing the size of transistors in a given gate, delay of the gate can be decreased but in contrast, power dissipated in the gate and fabrication space increases. Therefore, an optimum balance can be achieved by sizing of transistors appropriately. A method is to compute the slack at each gate in the circuit, where the slack of a gate corresponds to how much the gate can be slowed down without affecting the critical delay of the circuit. Alternatively, in different sub – circuits, where slack is greater than zero are utilized and the size of the transistors is reduced until the slack becomes zero, or the transistors attain a minimum size.

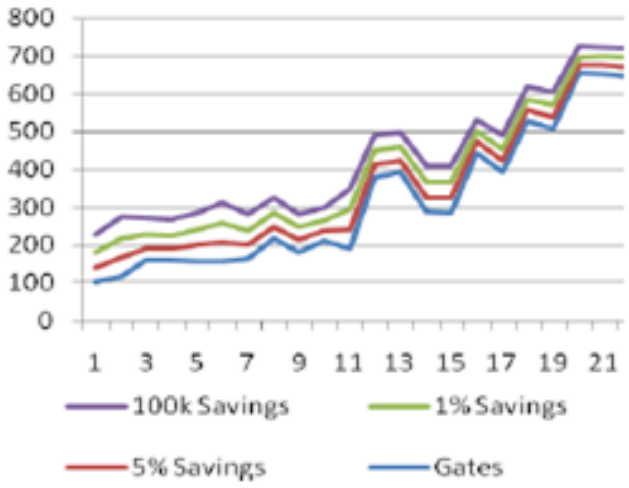
Combinational Gate Level Design

In gate level design of circuit, different combination of logical gates may different combination of logical gates may produce same circuit output but different value of power consumption. Path balancing, factorization and don't care optimization may be utilized to optimize power consumption. Path balancing can be achieved by avoiding delay at each input gate. Genetic Algorithm can be used to determine different combination of gates and power consumption can be formulated by devising *Fitness Function*. Coello [3] has proposed design of combinational logic circuit based on Genetic Algorithm.

By defining chromosome development schemes of various combinations of logic circuit can be developed using cross over and mutation. This approach is more efficient than human designer as various constraint of design circuit can be devised subject to fitness function. Genetic Algorithm can reduce number of gates, which consequently reduce power consumption; as the work of Coello [2], shows on 2-bit adder and 2-bit multiplier with a particular 'cardinality' that 56% reduction in number of gates for the circuit can be achieved.

IV. Comparison and discussion

Number of Gates versus power saving in CMOS – based on ISCAS-89 benchmark circuits. [8]



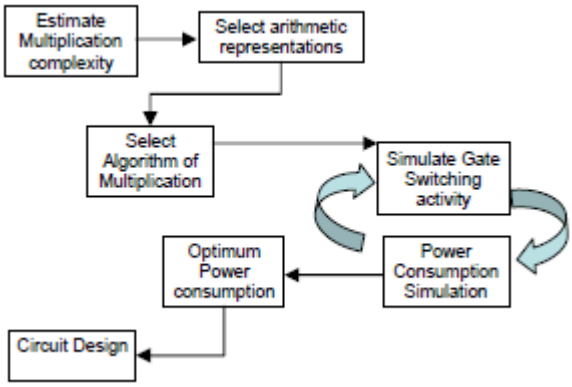
***(Graph-1) Gate V's Power based on the work of Jonathan P. Halter and Farid N. Najm* [8]**

Table 2. Power reduction versus Speed Loss

Power Reduction in supply voltage	Speed Loss	Constraints/ Specifications
leakage power reductions up to 54%	Not reported	"Logic design to reduce the leakage power of CMOS circuits that use clock gating to reduce the dynamic power dissipation tested on ISCAS-89 benchmark circuits" [8]
0.13 V or 800 times	19 times	"0.5-fim gate length and static logic" [9]
"1.1 V supply and consumes less than 5 mW-which is more than three orders of magnitude lower power compared to equivalent commercial solutions." [10]	Not reported	—

For instance, a modular approach as shown below in ***Fig. 1*** is proposed to adopt appropriate optimization technique considering different possibilities in multiplier design.

Figure1. Modular approach for multiplier design



V. Conclusion

It is found that data complexity and various combination of gate level digital circuit has considerable impact in power dissipiation. Besides, this physical design can be optimized by using Genetic algorithm by analysing the placement option. This is subjected to optimum space allocation. Similarly selection of Booth algorithm may reduce power consumption of data complexity. It is found that in multiplier circuit Modified Booth Algorithm reduces power consumption as compared to other methods of multiplication.

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