

## **Design and Development of Efficient Digital Filter Structures using Xilinx System Generator**

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**Abstract:** In this paper we propose the design and development of digital filters for audio application using Xilinx System Generator. Digital Filters are important elements in Digital Signal Processing (DSP). In this case, we can decimate the high frequency signal (128 KHz) upto respective low frequency signal (3.4 KHz). Also we introduced some designs of digital filters using MATLAB Simulink model and Xilinx System Generator and compare their respective results in case of computation and storage requirement. The proposed technique is centered on the FIR filtering technique for decimation of audio signal.

**Keywords:** Digital Signal Processing, Digital filters, FIR filter, Matlab Simulink and Xilinx System Generator.

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### **I. Introduction**

In many practical application of digital signal processing, there is a problem of changing the sampling rate of a signal, either increasing it or decreasing it by some amount. For example, in telecommunication system that transmits and receives the different types of signals (e.g. fax, speech, video, etc), there is a requirement to process the various signals at the different rates with corresponding bandwidth of the signals. The process of converting a signal from a given rate to a different rate is called as “sampling rate conversion” and the systems that employ multiple sampling rates in the processing of digital signals are called as “multirate digital signal processing system” [9].

In signal processing, down sampling (or "sub sampling") is the process of reducing the sampling rate of a signal [5]. This is usually done to reduce the data rate or the size of the data. The down sampling factor (commonly denoted by  $M$ ) is usually an integer or a rational fraction greater than unity. This factor multiplies the sampling time or, equivalently, divides the sampling rate [6]. Since down sampling reduces the sampling rate, it is usually a good idea to make sure the Nyquist–Shannon sampling theorem criterion is maintained relative to the new lower sample rate, to avoid aliasing in the resulting digital signal. To ensure that the sampling theorem is satisfied, or approximately so, a low-pass filter is used as an anti-aliasing filter to reduce the bandwidth of the signal *before* the signal is down sampled; the overall process (low-pass filter, then down sample) is sometimes called decimation .

Digital filters are easily designed, tested and implemented on a general purpose computer or workstation than the analog filters. The IIR filters are not well supported by softwares and Intellectuals property cores as compared to the FIR filters [20].

In this paper, we discuss the implementation of FIR filters using MATLAB Simulink model and Xilinx System Generator blocks.

### **II. Fir Filter**

Finite Impulse Response (FIR) filter is a type of a signal processing filter whose impulse response (or response to any finite length input) is of *finite* duration, because it settles to zero in finite time [14]. This is in contrast to infinite impulse response (IIR) filters, which have internal feedback and may continue to respond indefinitely (usually decaying). The impulse response of an Nth-order discrete-time FIR filter lasts for  $N+ 1$  sample, and then dies to zero [20]. In this design a MAC (Multiplier Accumulator) based FIR filter has been used.

There are many reasons why FIR filters are very attractive for digital filter design [20]. Some of them are:

- Simple robust way of obtaining digital filters
- Inherently stable when implemented non recursively
- Free of limit cycles when implemented non recursively
- Easy to attain linear phase
- Simple extensions to multirate and adaptive filters

- Relatively straight-forward to obtain designs to match custom magnitude responses
- Some vendors and specialized hardware only support FIR
- Low sensitivity to quantization effects compared to many IIR filters

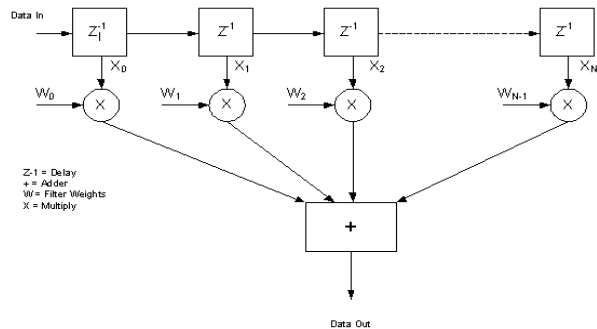


Fig.1: Basic FIR Filter Structures

### III. Fir Lowpass Filters

Because the impulse response required to implement the ideal lowpass filter is infinitely long, it is impossible to design an ideal FIR lowpass filter [17]. Finite length approximations to the ideal impulse response lead to the presence of ripples in both the passband ( $w < wc$ ) and the stopband ( $w > wc$ ) of the filter, as well as to a nonzero transition width between the passband and stopband of the filter (see Figure 3) where,  $w_c =$  cutoff frequency [20].

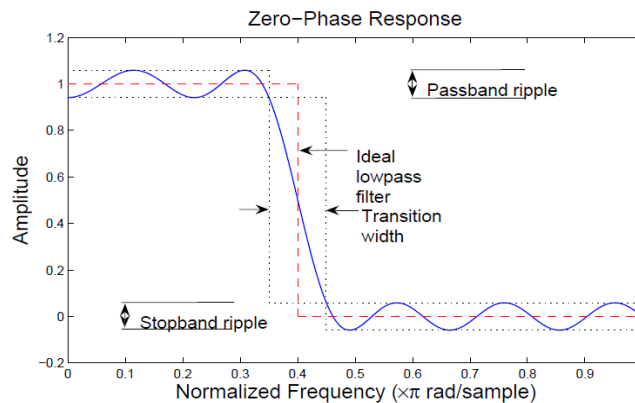


Fig.2: Illustration of the typical deviations from the ideal lowpass filter when approximating with an FIR filter,  $w_c = 0.4\pi$ .

### IV. Matlab Simulink

Simulink is a software package for modeling, simulating, and analyzing dynamical systems including in the MATLAB environment. It supports linear and nonlinear systems, modeled in continuous time, sampled time, or a hybrid of the two. Systems can also be multirate, i.e., have different parts that are sampled or updated at different rates. Model analysis tools include linearization and trimming tools, which can be accessed from the MATLAB command line, plus the many tools in MATLAB and its application toolboxes. And because MATLAB and Simulink are integrated, we can simulate, analyze, and revise our models in either environment at any point [19] and [20].

### V. Xilinx System Generator

Xilinx produces many software tools to simplify the design task for hardware programmers. One such program is DSP System Generator. It interfaces with Matlab Simulink and provides efficient implementations of digitally realizable Simulink blocks and commonly used digital programming blocks. Another important feature of System Generator is the Gateway In/out blocks. These provide the interface between the double precision of Simulink with the floating point architecture of FPGA [2].

## VI. Block Modelling Of Fir Filter

### a. Single Stage FIR Filter:



Fig.3: Block diagram of Single stage Decimation Filter

In this single stage FIR Filter model, input high frequency signal is 128 KHz and we have to decimate it up to 3.4 KHz. Thus we use decimation factor is 32 i.e. ( $M = 32$ ). The sampling rate of input signal is 256 KHz.

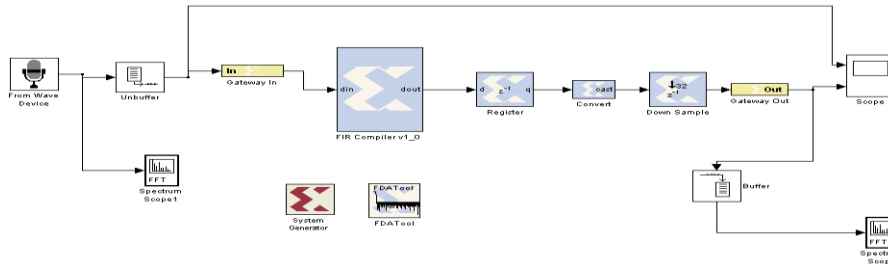


Fig.4: Simulink model of Single Stage FIR Filter

Filter Specifications	Values
Sampling Frequency	256 KHz
Decimation factor	32
Passband Frequency	3.4 KHz
Stopband Frequency	4 KHz
Transition width	0.00234
Passband Attenuation	0.1 dB
Stopband Attenuation	40 dB
Order of Filter (N)	900

Table 1: Filter Specification of Single Stage FIR Filter

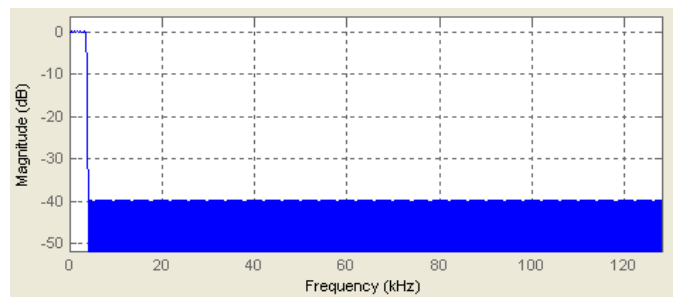


Fig.5: Frequency response of Single Stage FIR Filter

### b. Two Stage FIR Filter

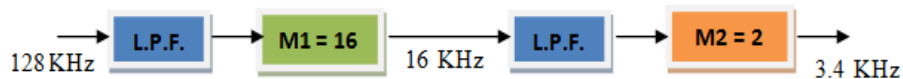


Fig.6: Block diagram of two stage Decimation Filter

In this two stage FIR Filter model, input high frequency signal is 128 KHz and we have to decimate it up to 3.4 KHz. Thus we use two decimation factors are 16 and 2 i.e. ( $M1 = 16$  and  $M2 = 2$ ). Thus the total decimation factor is 32. The sampling rate of input signal at first stage is 256 KHz and sampling rate of second stage is 32 KHz.

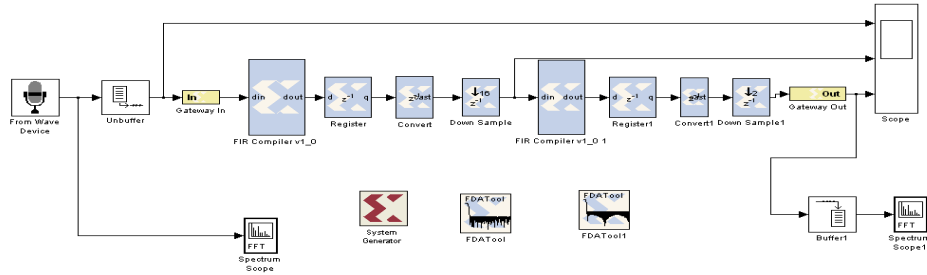


Fig.7: Simulink model of Two Stage FIR Filter

Filter Specifications	Values
Sampling Frequency	256 KHz
Decimation factor	16
Passband Frequency	3.4 KHz
Stopband Frequency	12 KHz
Transition width	0.03359
Passband Attenuation	0.05 dB
Stopband Attenuation	40 dB
Order of Filter (N)	83

Table 2: Filter Specification of Two Stage FIR Filter (First Stage)

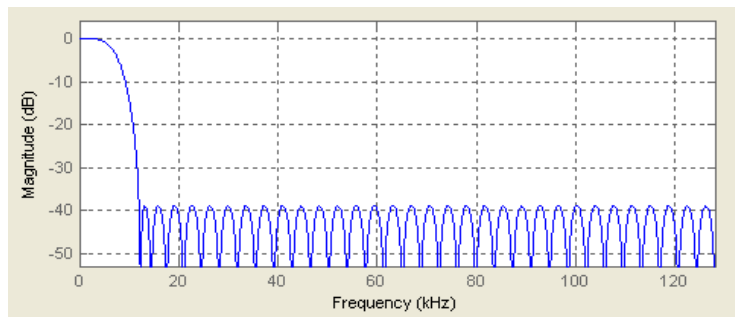


Fig.8: Frequency Response of First Stage of Two Stage FIR Filter

Filter Specifications	Values
Sampling Frequency	256 KHz
Decimation factor	2
Passband Frequency	3.4 KHz
Stopband Frequency	8 KHz
Transition width	0.01796
Passband Attenuation	0.05 dB
Stopband Attenuation	40 dB
Order of Filter (N)	155

Table 3: Filter Specification of Two Stage FIR Filter (Second Stage)

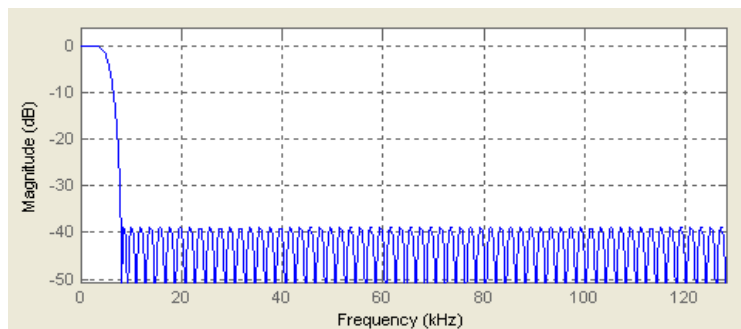


Fig.9: Frequency response of second stage of Two Stage FIR Filter

c. Three Stage FIR Filter

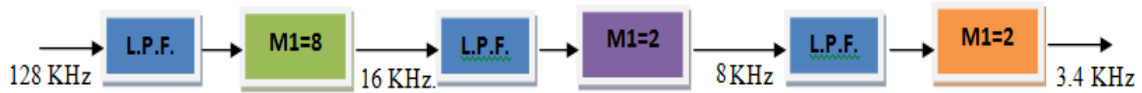


Fig.10: Block diagram of Three Stage Decimation Filter

In this three stage FIR Filter model, input high frequency signal is 128 KHz and we have to decimate it up to 3.4 KHz. Thus we use three decimation factors are 8, 2 and 2 i.e. (M1 = 8, M2 = 2 and M3 = 2). Thus the total decimation factor is 32. The sampling rate of input signal at first stage is 256 KHz and sampling rate of second stage is 32 KHz and sampling rate of third stage is 16 KHz.

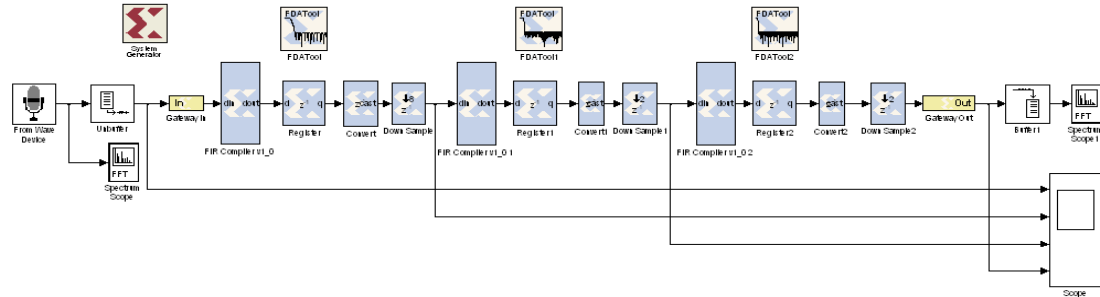


Fig.11: Simulink model of Three Stage FIR Filter

Filter Specifications	Values
Sampling Frequency	256 KHz
Decimation factor	8
Passband Frequency	3.4 KHz
Stopband Frequency	28 KHz
Transition width	0.0960
Passband Attenuation	0.033 dB
Stopband Attenuation	40 dB
Order of Filter (N)	25

Table 4: Filter Specification of Three Stage FIR Filter (First Stage)

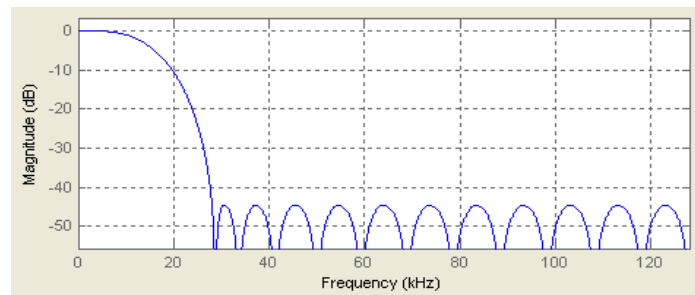


Fig.12: Frequency response of First stage of Three Stage FIR Filter

Filter Specifications	Values
Sampling Frequency	256 KHz
Decimation factor	2
Passband Frequency	3.4 KHz
Stopband Frequency	12 KHz
Transition width	0.03359
Passband Attenuation	0.033 dB
Stopband Attenuation	40 dB
Order of Filter (N)	69

Table 5: Filter Specification of Three Stage FIR Filter (Second Stage)

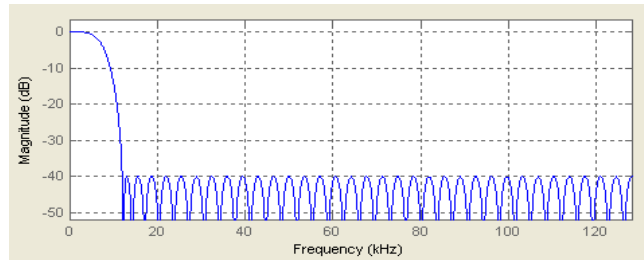


Fig.13: Frequency response of Second stage of Three Stage FIR Filter

Filter Specifications	Values
Sampling Frequency	256 KHz
Decimation factor	2
Passband Frequency	3.4 KHz
Stopband Frequency	8 KHz
Transition width	0.0179
Passband Attenuation	0.033 dB
Stopband Attenuation	40 dB
Order of Filter (N)	136

Table 6: Filter Specification of Three Stage FIR Filter (Third Stage)

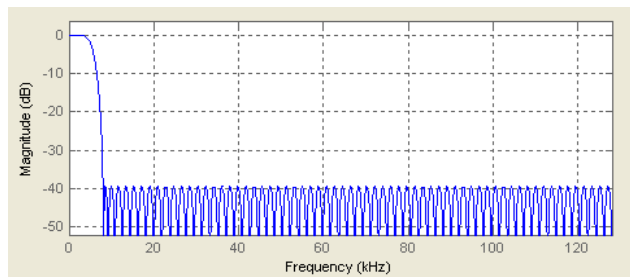


Fig.14: Frequency response of Third stage of Three Stage FIR Filter

**d. Four Stage FIR Filter**

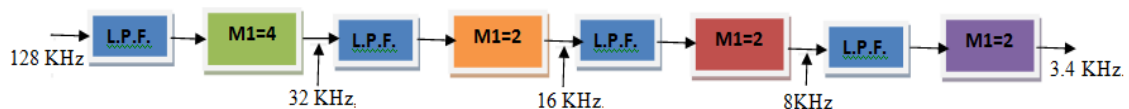


Fig.15: Block diagram of Four Stage Decimation Filter

In this four stage FIR Filter model, input high frequency signal is 128 KHz and we have to decimate it up to 3.4 KHz. Thus we use four decimation factors are 4, 2, 2 and 2 i.e. (M1 = 4, M2 = 2, M3 = 2 and M4 = 2). Thus the total decimation factor is 32. The sampling rate of input signal at first stage is 256 KHz and sampling rate of second stage is 64 KHz, sampling rate of third stage is 32 KHz, sampling rate of fourth stage is 16 KHz.

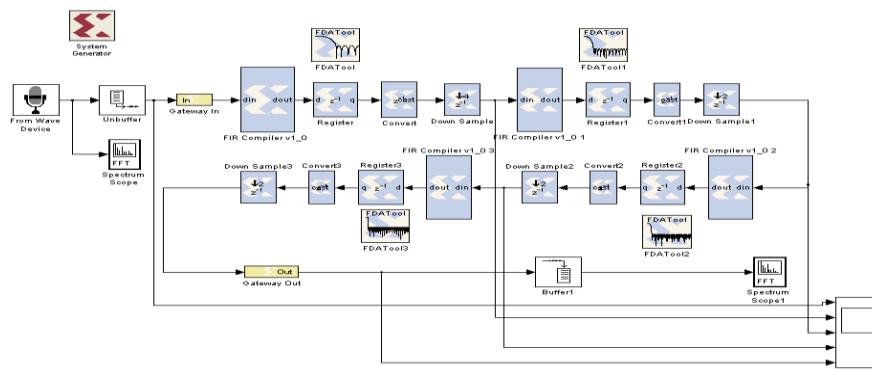


Fig.16: Simulink Model of Four Stage FIR Filter

Filter Specifications	Values
Sampling Frequency	256 KHz
Decimation factor	4
Passband Frequency	3.4 KHz
Stopband Frequency	60 KHz
Transition width	0.2210
Passband Attenuation	0.024 dB
Stopband Attenuation	40 dB
Order of Filter (N)	10

Table 7: Filter Specification of Four Stage FIR Filter (First Stage)

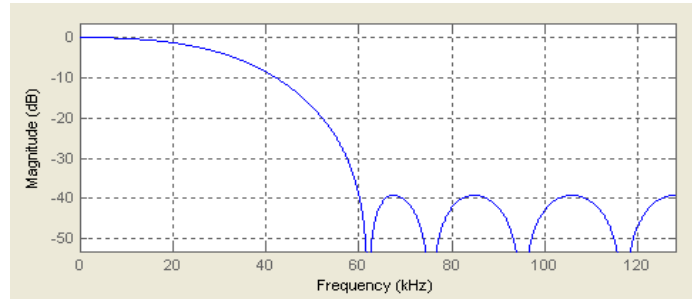


Fig.15: Frequency response of First stage of Four Stage FIR Filter

Filter Specifications	Values
Sampling Frequency	256 KHz
Decimation factor	2
Passband Frequency	3.4 KHz
Stopband Frequency	28 KHz
Transition width	0.0960
Passband Attenuation	0.024 dB
Stopband Attenuation	40 dB
Order of Filter (N)	26

Table 8: Filter Specification of Four Stage FIR Filter (Second Stage)

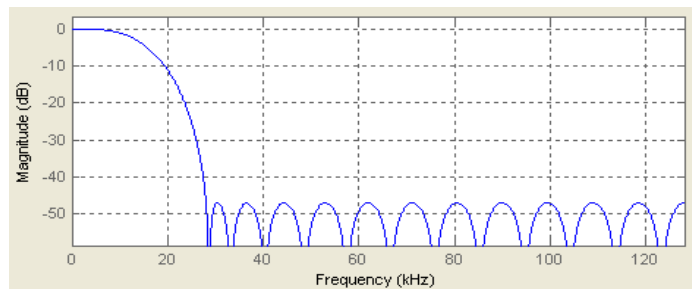


Fig.16: Frequency response of Second stage of Four Stage FIR Filter

Filter Specifications	Values
Sampling Frequency	256 KHz
Decimation factor	2
Passband Frequency	3.4 KHz
Stopband Frequency	12 KHz
Transition width	0.0335
Passband Attenuation	0.024 dB
Stopband Attenuation	40 dB
Order of Filter (N)	75

Table 9: Filter Specification of Four Stage FIR Filter (Third Stage)

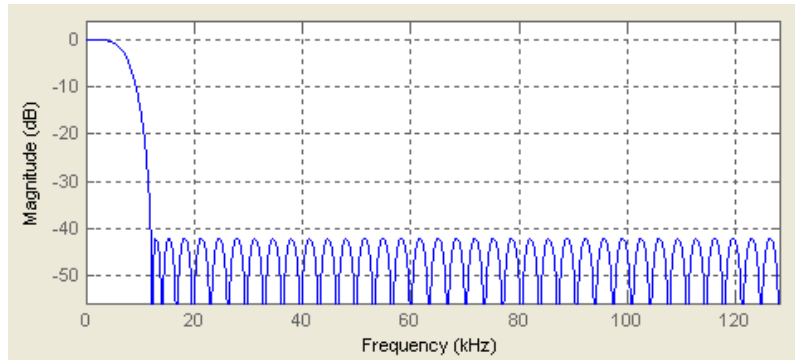


Fig.17: Frequency response of Third stage of Four Stage FIR Filter

Filter Specifications	Values
Sampling Frequency	256 KHz
Decimation factor	2
Passband Frequency	3.4 KHz
Stopband Frequency	8 KHz
Transition width	0.0179
Passband Attenuation	0.024 dB
Stopband Attenuation	40 dB
Order of Filter (N)	140

Table 10: Filter Specification of Four Stage FIR Filter (Forth Stage)

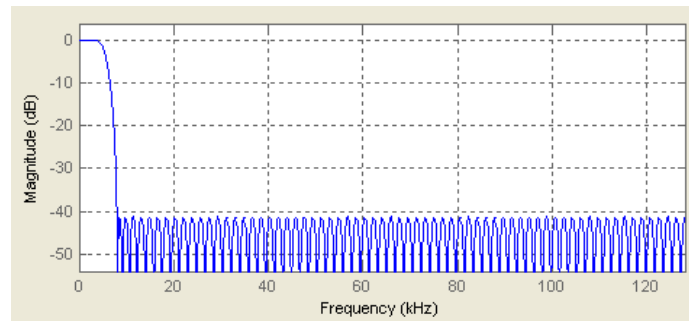


Fig.18: Frequency response of Fourth stage of Four Stage FIR Filter

### VII. Conclusion

No. of Stages	N1	N2	N3	N4	M1	M2	M3	M4	MPS	TSR
1	900	-	-	-	32	-	-	-	28800	900
2	83	155	-	-	16	2	-	-	1638	238
3	25	69	136	-	8	2	2	-	610	230
4	10	26	75	140	4	2	2	2	522	251

It is clear that, in general, multirate designs yield very significance reductions in both computation and storage requirements compared with single-stage designs. The reductions are due to the wide transitions of filters at the early stages, leading to small values of N (filter coefficients).

In comparison of efficiencies of the multistage designs, it is found that the reduction in computation of Multiplication per Second (MPS) and Total Storage Requirement (TSR) are greatest in going from one stage to four stages. Overall, Three stages FIR filter is appeared the most efficient implementation.



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