A New Full Bridge DC/DC Converter Topology with ZVZCS Features

Anupama K Vijayan, Sreesh Sreedharan, Prima Philip

Abstract: *DC/DC converters are having important applications in many offline power supplies. They are widely used in different types of electronic devices such as battery charger, electric vehicles, and in portable devices like cellular phones, laptops, computers etc. In battery charger applications, after the battery is fully charged, the load is zero and the converter should be safely operate from no-load to full load conditions. The fundamental problem regarding the conventional full bridge DC/DC converter topology is the voltage spikes across output diodes due to transformer leakage inductance and also, the conventional topology is not able to ensure ZVS operation for wide range of load variations. This paper presents a novel full bridge DC/DC converter topology having zero voltage zero current switching (ZVZCS) features. The proposed converter clamps the voltage across the output diodes by using a symmetric passive auxiliary circuit and offers ZVS at all load conditions. The simulation result of the proposed converter is carried out in MATLAB 7.8.0(R2009a) and the waveforms are analyzed.*

Index Terms: *DC/DC converter, full-bridge converter, Zero Current Switching (ZCS), ZeroVoltage Switching (ZVS), ZeroVoltage ZeroCurrent Switching (ZVZCS).*

I. Introduction

Nowadays, interest in the use of electric vehicles has been motivated by the carbon emission savings they could achieve [1] and their advantage over the conventional internal combustion engine is the main reason for the upcoming developments in the field of electric vehicles. Electric vehicles derive some or all of the power from large, rechargeable batteries. This paper introduces a new type of DC to DC fullbridge converter topology with ZVZCS features [2].The DC to DC converter proposed in this paper can be used for charging the high voltage battery of the electric vehicle.Generally,full bridge DC/DC converter topology is the most popular topology used in the power range of a few kilowatts (1-5 KW) [3] and MOSFET's are used to implement the full bridge converters. For the reliable and efficient operation, MOSFET's should be switched under zero voltage.Loss of ZVS will increase the converter switching losses and EMI due to high di/dt of the snubber discharge current. Loss of ZVS also causes a noisy control circuit, which will result in a shoot through state of the converter switches. Operation of converter switches at zero voltage switching decreases the switching losses and provides a noise free environment for the control circuit.

Fig. 2 represents the general block diagram for the electric vehicle power conditioning system [12]. In this system, there are two battery units: a high voltagebattery, and a 12-V battery. The power conversion system consists ofan ac/dc converter which is a rectifier, a dc/dcConverter which is the proposed full bridge ZVZCS dc/dc converter and a dc/ac inverter.
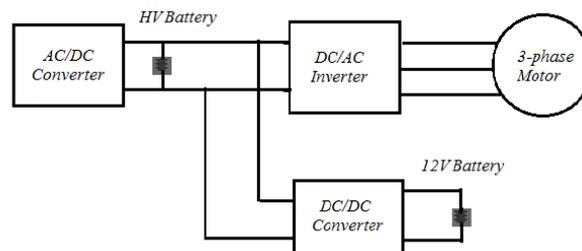

Fig.2. Block Diagram Of EV Power Conditioning System

The proposed ZVZCS full bridge converter charges the high voltage battery which feeds the three phase inverter and the electric motor. The high-voltage battery is also charging the12-V battery through a dc/dc converter.
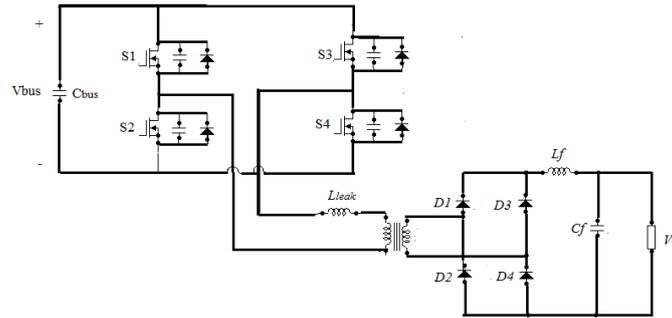
1)

Fig.1. Conventional full-bridge converter`

The main problem identified in the conventional full bridge dc to dc converter shown in fig.1 is the large voltage spikes across the output diodes,these voltage spikes are caused by the leakage inductance of the transformer. The voltage spikes across the output diodes get intensified as switching frequency of the converter increases since the leakage inductance acts as a current source. Thus the output diodes will have to withstand these large voltage spikes. For example, for a 400V output DC supply a 1200V voltage appears across the output diodes. Thus, the component rating increases and the topology is not practical for the high voltage high frequency applications.

In the battery charging applications, after the battery is completely charged, the load is zero and the converter must be safely operated under this condition. Zero voltage condition is very important in battery charging applications and the condition should be satisfied from no load to full load condition. In the conventional full bridge converters, ZVS is achieved by using the energy used in the leakage inductance to discharge the output capacitance of the MOSFET's. Thus, the range of ZVS in conventional system will highly depends on the load and transformer leakage inductance. Thus, the conventional full bridge DC to DC converter topology is not able to ensure ZVS operation over a wide range of load variations [4].

There are some existing methodologies to eliminate the voltage spikes across the output diodes. In [5], an R-C-D snubber and in [6],an active clamp circuit has been added to the converter to clamp the voltage across the output diodes. Energy recovery clamp circuits (ERCCs) has been proposed to avoid the adverse effect of voltage spikes in the diodes [7]-[9].The ERCC techniques are able to reduce the voltage stress of the output diodes, but in case of ERCC's the amount of the voltage stress will depend on the duty ratio and input voltage of the converter in most of the ERCCs techniques. Some references tried to decrease the leakage inductance as much as possible through the transformer winding structures [10]. These topologies effectively decrease the peak of the voltage spikes across the output diodes. The problem is, reducing the leakage inductance decreases the ZVS operating range of the full-bridge converter, which results in a very narrow range of ZVS operation. In [11], a new modified current-fed full-bridge DC to DC converter topology is introduced in order to reduce the voltage stress arising in the conventional current-fed full-bridge converter.

The main objective of this project is to design a novel DC to DC converter with ZVZCS features having superior efficiency at all load conditions. The proposed converter should clamp the voltage spikes across the output diodes. The proposed converter operates as a current driven rectifier and provides zero current switching (ZCS) for the output rectifier which eliminates the voltage spikes problem. The proposed topology offers zero voltage switching under all load conditions.

This paper is organized as follows: Section II describes the proposed topology. Section III analyzes the different operating modes of the proposed converter. Design considerations are given in section VI. Section V shows the simulation results and Section VI, provides the conclusion.
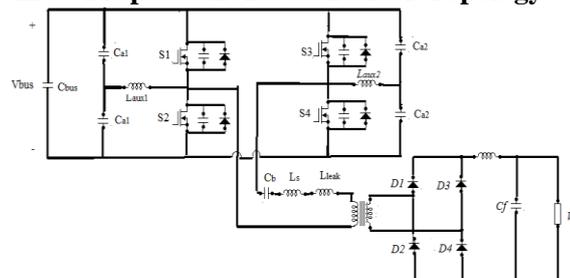
II. Proposed Zvzcs Converter Topology

Fig 2.Proposed ZVZCS full-bridge converter

Fig. 2 shows the proposed ZVZCS full bridge converter. The main problem identified in the conventional full bridge dc to dc converter is the large voltage spikes across the output diodes, these voltage spikes are caused by the leakage inductance of the transformer. These voltage spikes are get intensified as switching frequency of the converter increases since the leakage inductance acts as a current source. Thus the output diodes will have to withstand these large voltage spikes. . For example, for a 400V output DC supply a 1200V voltage appears across the output diodes. Thus, the component rating increases and the topology is not practical for the high voltage high frequency applications.

This phenomenon can be mitigated by using snubber circuits or clamp circuits. The snubber circuit can effectively reduce the voltage spikes across the output diodes. Although it can reduce the peak value of the voltage spikes,the amount of losses in the snubber resistor is the main disadvantage, which considerably decreases the efficiency of the converter especially at higher power. That means, the R-C-D snubber circuits are usually lossyand cannot be used for high frequency applications. In addition, the voltage spikes are highly intensified as load is increased which makes the snubber circuit a very poor solution for high frequency applications. A clamp circuit also can effectively clamp the voltage spikes of the output diodes, but the active clamp circuits will increases the complexity of the converter and causes small losses in the clamp circuit.

The proposed converter rectifies the voltage stress problems related to the conventional full-bridge DC/DC converter. The proposed ZVZCS full bridge DC to DC converter topology provides zero current switching (ZCS) for the output rectifiers, and zero voltage switching (ZVS) for the full bridge inverter. Output diode rectifiers are turned on when the current is zero in the transformer leakage inductance. In the proposed ZVZCS converter, an auxiliary circuit is used to produce the reactive. Current for the full bridge switches and this ensures the ZVS. This auxiliary circuit will be working independent of the system operating conditions and is able to guarantee ZVS at all operating conditions and the use of this auxiliary circuit is to provide reactive current for the full-bridge semiconductor switches, which guarantees zero voltage switching for the semiconductor switches. The different mode of operations of the proposed ZVZCS full bridge converter is explained below [1].

III.   Modes Of Operation
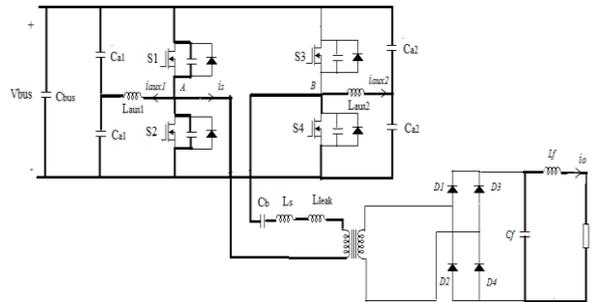
MODE *1: ($t_0 \leq t \leq t_1$):*

Fig 3(a)

S_2 is turned OFF at t_0. The output capacitor of S_1 is discharging and that of S_2 is charging up using the reactive current provided by the auxiliary circuit. In this interval, the secondary-side diodes are reversed biased and are OFF. In this mode,the rising voltage V_{AB}conducts a very small current through the DC blocking capacitor C_b, series inductance L_S, leakage inductance L_{leak}, and magnetizing inductance L_M. Fig. (a) Shows the active components during this mode of operation [1].
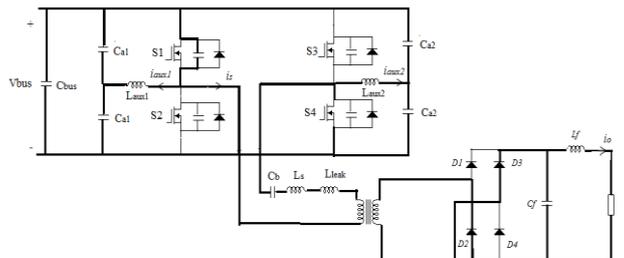
MODE 2: *($t_1 \leq t \leq t_2$):*

Fig 3(b)

The output diodes get forward biased in this mode as V_{AB} reaches output voltage plus the voltage drops of the diode.Fig.3 (b) shows the active components during this mode. As shown in this figure, the output capacitor of

the MOSFET, S_1 is still discharging to finally reach zero and that of S_2 is charging up to V_{dc}. The second mode ends once the voltage across this capacitor becomes zero. The active component during this mode is shown in fig (b) [1].

MODE 3: *($t_2 \leq t \leq t_3$) :*
In this mode starts the MOSFET of the output capacitors have been charged and discharged completely. Now the gate voltage is applied to S_3 and is turned ON. Fig.3 (c) shows the active components during this mode
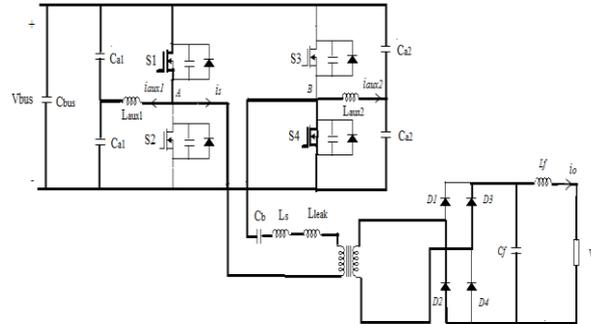

Fig 3 (c)

In this mode, the output diodes clamp the secondary voltage to the output voltage and there is a constant voltage across the combination of the series inductance and the leakage inductance. The series current ramps up to its peak value [1].
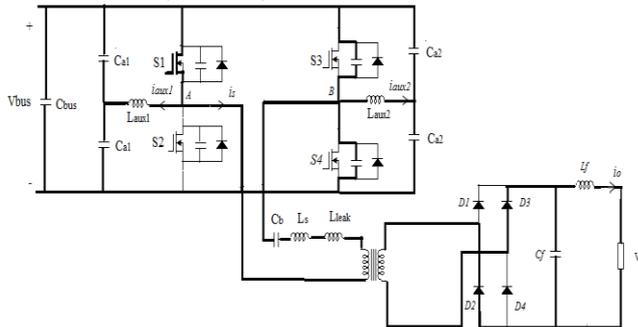
MODE 4 :*($t_3 \leq t \leq t_4$) :*

Fig 3 (d)

Fig.3 (d) Shows the active circuit during this mode. In this interval the output capacitor of S_3 is discharging from and that of S_4 is charging up to V_{dc}. This mode ends when the S_3 output capacitor got completely discharged and S_4 output capacitor got charged to V_{dc}. At the end of the mode 4, $V_{AB}(t_4) = 0$ [1].

MODE *5: ($t_4 \leq t \leq t_5$):*
Fig.3 (e) Illustrate the active components during this mode of operation. Once this voltage V_{AB} will become zero this mode commences. During this mode, the output voltage of the inverter is zero and the output diodes will clamp the secondary voltage to the output voltage. Therefore, a net negative voltage is incident across the series inductor, which is the reflected output voltage at the transformer primary side. This will lead to the current i_s to ramp down [1].
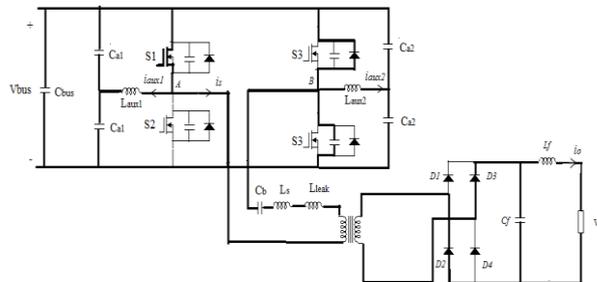

Fig. 3(e)

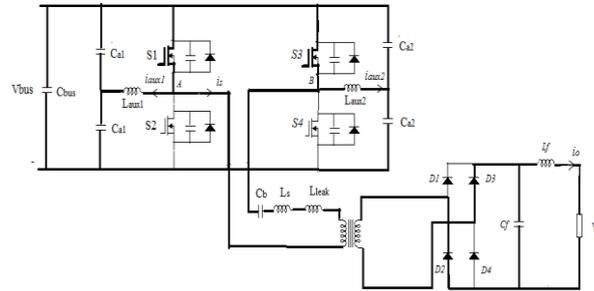MODE 6: $(t_5 \leq t \leq t_6)$

Fig 3 (f)

Mode 6 starts when the gate pulse is applied to S_3. The active components in this mode are illustrated in Fig.3 (f). Therefore, the series inductor current is still ramping down and reaches zero at the end of this mode. Switch S_1 turns off under near zero current switching at the end of this mode. At the end of this mode, the current through the series inductor reaches zero and the output diodes D_2 and D_3 naturally turn off with zero current [1].
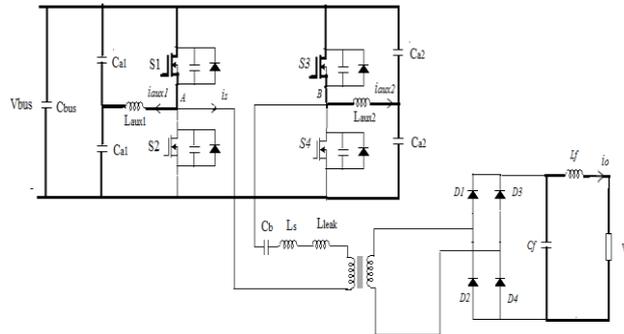
MODE 7: $(t_6 \leq t \leq t_7)$:

Fig 3 (g)

Fig.3 (g) illustrates the active components during this mode of operation. This mode starts when the current through output diodes reaches zero and the diodes naturally turn off with zero current. In this mode, the output capacitor C_f feeds the output load with its stored energy while on the transformer primary side there is no current. In one switching cycle, the proposed circuit has 14 modes during steady-state operation. The remaining 7 modes have the symmetrical structure as the previous 7 modes.

IV. Design Cosiderations
DESIGN OF AUXILIARY INDUCTORS

Auxiliary inductors are designed based on the amount of reactive power required to guarantee ZVS for the MOSFETs. This reactive current must be enough to completely charge and discharge the MOSFET output capacitors. In battery charging applications, after battery is fully charged, load is zero. Thus, ZVS must be guaranteed for zero load in order to make sure ZVS operation for all operating conditions. At absolutely no-load, the primary current is zero and therefore, the current through auxiliary circuit of the leading leg should only charge and discharge the output capacitors of the MOSFETs. The auxiliary circuit current remains constant during the dead-time between the switching transitions, and the auxiliary inductor acts as a constant current source, which discharges the capacitor across S_1 and charges the capacitor across S_2.

$$I_{PA} = \frac{V_{dc}}{8 L_{AUX1} f_s}$$

To design the inductor for the auxiliary circuits, first the amount of energy required to charge and discharge the output capacitors of the MOSFETs must be calculated. The amount of dead-time required to allow complete charging and discharging is also derived. The amount of energy stored in the auxiliary inductor is given by,

$$E_{AUX} = \frac{1}{2} . L_{AUX1} . I^2_{PA}$$

The amount of energy required to charge and discharge the output capacitors of the MOSFETs is given by the equation,

$$E_{Cso} = C_{SO}.V^2{}_{dc}$$

The value of the auxiliary inductance is designed using the following equation,

$$L_{AUX1} = \frac{1}{128C_{SO}.f_s{}^2}$$

In order to ensure ZVS operation, the dead-time t_d should be adjusted such as to allow the output capacitors of the MOSFETs to fully charge and discharge. The dead time to have ZVS operation is given by the equation,

$$t_d = \frac{2C_{SO}.V_{dc}}{I_{PA}}$$

VI. Simulation Results

There are number of simulation software available and here the simulink part of the MATLAB is employed. Simulation of conventional and proposed full bridge DC/DC converter topology is performed using matlab. The output waveforms of conventional full bridge converter and proposed ZVZCS full bridge converter are given. All input dc sources are equal.MATLAB 7.8.0(R2009a) is used for simulation part of the work
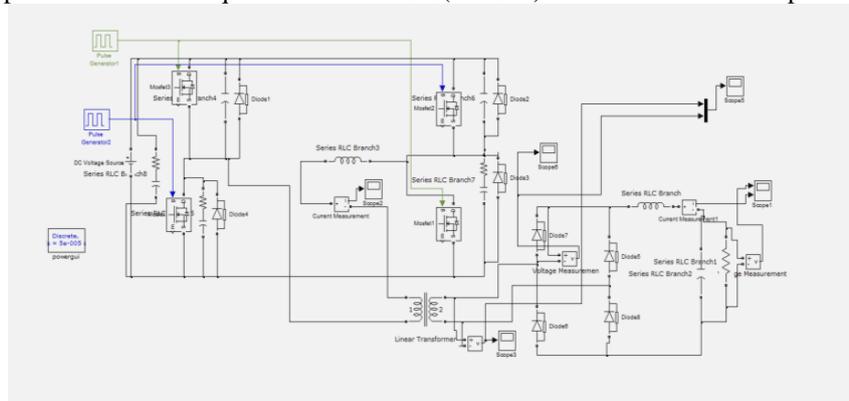

Fig.4.Simulation diagram of Conventional full bridge converter

Fig.4 shows the MATLAB simulation circuit for the conventional DC/DC converter, the waveforms are obtained as shown in below. The DC input of the converter is given as 190V.
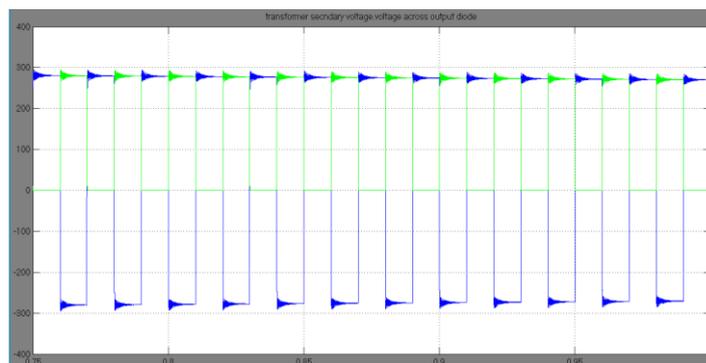

Fig. 5.Transformer secondary voltage, voltage across diode of Conventional full bridge converter
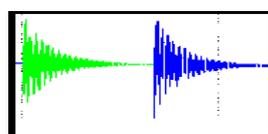

Fig. 5(a) Zoomed figure of fig.5

The transformer secondary voltage and the voltage across the output diode of the conventional full bridge transformer is distorted and we get a 300 V DC output voltage. Thesevoltage spikes are get intensified as switching frequency of the converter increases since the leakage inductance acts as a current source. Thus the output diodes will have to withstand these large voltage spikes. Thus the converter cannot be used in high voltage high frequency applications.
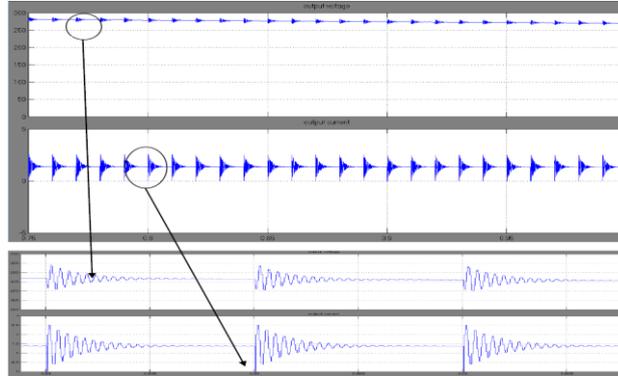

Fig. 6. Output voltage and output current

Fig.6 illustrates the output voltage and output current for the conventional full bridge DC to DC converter. From the simulated waveform, it is found that the output voltage and current are distorted. These are the fundamental problems identified in the conventional DC to DC converter.

The simulation of the proposed ZVZCS full bridge converter is illustrated in fig.7. The input given is 190 V and the switching frequency is set to be 10KHZ. The design specifications of the proposed converter is given in the table I.

Table I. DESIGN SPECIFICATIONS OF PROPOSED CONVERTER

SYMBOL	PARAMETER	VALUE
Laux1,2	Auxiliary inductor	67μH
Leq	Series inductor	11.8μH
Cf	Filter capacitor	1μH
Lf	Filter inductor	80μH
Ca1	Auxiliary capacitor	2.2μH

The main advantage of this convertor is the absence of voltage spike across the power electronic switches. The switching loss in this converter is minimum and the rating of power electronic switches is reduced considerably.

The zero voltage switching for switch S1 is shown in fig.8. From the analysis of the figure, gating pulses are given for switch S1, whenever the voltage across the switch becomes zero. That means Zero voltage condition is achieved for the proposed converter and is satisfied under all load conditions. The zero voltage switching has advantages like reduced switching losses and EMI and also it provides a noise-free environment for the control circuit.
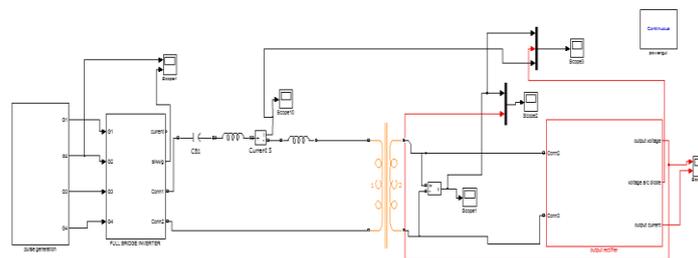

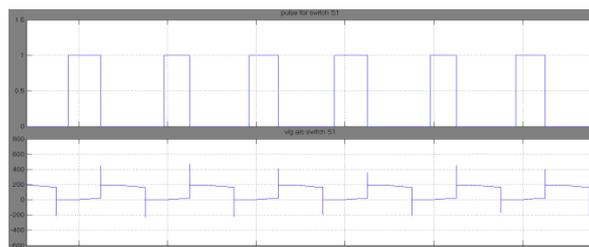Fig. 7.Simulation diagram of Proposed ZVZCS full bridge converter

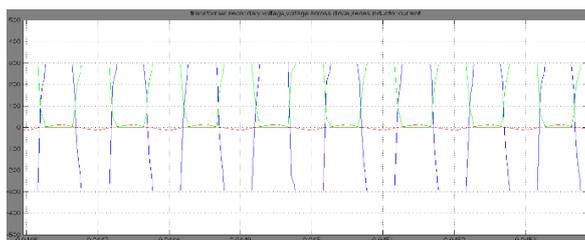Fig.8. Zero voltage switching for switch S1

Fig. 9. Transformer secondary voltage, voltage across diode and series inductor current

The fig.8 illustrates the transformer secondary voltage, voltage across output diode and the current through the series inductor. There are no voltage spikes in the transformer secondary voltage and voltage across output diodes as shown in conventional full bridge converter (fig.4).
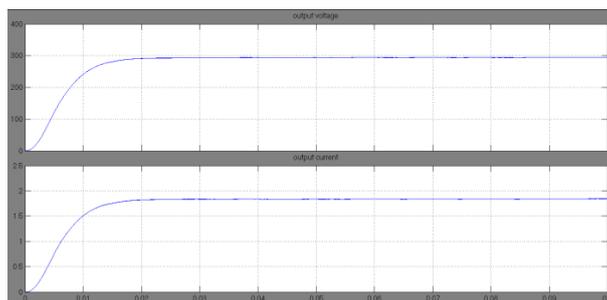

Fig.10. Output voltage and output current

Fig.9 gives the Output voltage and output current for the proposed ZVZCS full bridge DC to DC converter. From the comparison of the output's of the conventional full bridge topology given in fig.6 and fig.9, it is found that the voltage spikes are eliminated.From the analysis of this waveform, it is found that all the limitations in the conventional full bridge DC to DC converter is eliminated in the proposed ZVZCS full bridge converter.

VII.   Conclusion

A novel full bridge topology is introduced that is used for high voltage battery charging applications that are having ZVZCS property. The proposed converter eliminates the limitations in the conventional full bridge DC to DC converter. The proposed converter effectively rectifies the voltage stress problems related to the full-bridge DC/DC converter that is caused by the leakage inductance of the transformer. The proposed topology provides zero current switching (ZCS) for the output rectifiers, and zero voltage switching (ZVS) for the full bridge inverter. Zero current switching for the output rectifier eliminates the voltage spikes across the output diodes. In the proposed converter, an auxiliary circuit consisting of an inductor and split capacitor is used to produce the reactive current for the full-bridge switches. The auxiliary circuit is working independent of the system operating conditions and is able to guarantee ZVS at all operating conditions and this auxiliary circuit provides reactive current for the full-bridge semiconductor switches, which guarantees zero voltage switching for the semiconductor switches.

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Anupama K Vijayan obtained her Bachelor degree in Electrical And Electronics from Ilahia College Of Engineering & Technology, Muvattupuzha, Kerala , India. She is currently pursuing M.Tech in Power Electronics from Toc H Institute of Science and Technology (TIST), Kerala, India. Her area of interest is Power Quality.

SreeshSreedharan received his B. Tech degree from Government Engineering College, Idukki, Kerala, India. Currently he is doing M.Tech in power Electronics and Control from GEC ,Idukki, Kerala, India.. His area of interest is resonant converters.

Prima Philip is currently working as an Assistant Professor at Toc H Institute of Science and Technology, Arakkunnam. Her area of interests are Power Electronics and Control Systems.