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Exploring CMOS logic families in sub-threshold region for ultra low power applications

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Abstract : *Numerous efforts in balancing the trade-off between power, area and performance have been done in the medium performance, medium power region of the design spectrum. However, not much study has been done at the two extreme ends of the design spectrum, namely the ultra-low power with acceptable performance at one end and high performance with power within limit at the other. One solution to achieve the ultra-low power requirement is to operate the digital logic gates in sub-threshold region. In this paper, we investigate different logic families in sub-threshold region for ultra-low-power applications. For the first time, the performance characteristics of inverter and also the basic gates for different logic families operating in the sub-threshold region have been compared using 90nm technology cadence circuit simulations. The results of the simulations show that the sub-threshold logics have some advantages compared to their strong inversion counterparts. Enhancing the performance of these circuits will leads to enhancement of overall system performance.*

Keywords: *circuit simulation, Digital logic gates, Medium performance, Sub-threshold region, Ultra low power design*

I. INTRODUCTION

In digital VLSI system design space, considerable attention has been given to the design of high performance microprocessors. However, in recent years, the demand for power sensitive designs has grown significantly. This tremendous demand has mainly been due to the fast growth of battery-operated portable applications such as personal digital assistants, cellular phones, medical applications, wireless receivers, and other portable communication devices. [1] Energy recovery or adiabatic techniques promises to reduce power in computation by orders of magnitude. But it involves use of high-quality inductors which makes integration difficult. More recently, design of digital sub-threshold logic was investigated with transistors operated in the sub-threshold region (supply voltage (*V*dd) less than the threshold voltage (*V*th)) of the transistor) in such a technique the sub-threshold leakage current of the device is used for necessary computation. This result in high transconductance gain of the devices (thereby providing near ideal voltage transfer characteristics of the logic gates) and reduced gate input capacitance. Its impact on system design is an exponential reduction of power at the cost of reduced performance. [] Digital computation using sub-threshold leakage current has gained a wide interest in recent years to achieve ultralow-power consumptions in portable computing devices. Both logic and memory circuits have been extensively studied with design consideration at various levels of abstraction. It has been shown that using sub-threshold operation; significant power savings can be achieved in applications requiring low to medium (ten to hundreds of megahertz) frequency of operation. Hearing aid devices are clearly one of the most suitable application areas for sub-threshold logic since ultra-low-power consumption takes first priority, while the clock rate is merely in the kHz range. Digital sub-threshold logic has successfully achieved ultra-low-power consumption in areas where performance is of secondary importance. By simply reducing the supply voltage below (threshold voltage), we can operate circuits using only the minute leakage current. [3] Although, the delay rapidly increases, ultra-low power can be achieved without major alteration of the circuit.

The rest of this paper is organized as follows. In Section II, We review the key metrics involved in the sub-threshold region and the concept behind it. In Section III, we reviewed about differ CMOS logic families optimal for sub-threshold circuit design. In section IV we presented the design schematics and the performance characteristics of the basic gates for different logic families operating in the sub-threshold region which are obtained from cadence circuit simulations. In Section V, we present the 90nm technology cadence circuit simulation results of designed circuits in Section IV. Finally we conclude in Section VI.

II. SUB-THRESHOLD REGION

The operation of a MOSFET can be separated into three different modes, depending on the voltages at the terminals. In the following discussion, a simplified algebraic model is used. Modern MOSFET characteristics are more complex than the algebraic model presented here. For an enhancement-mode, n-channel

MOSFET, the three operational modes are Sub-threshold or Weak-inversion mode, non-saturation mode, Saturation mode. When $V_{GS} < V_{th}$, where V_{gs} gate-to-source is bias and V_{th} is the threshold voltage of the device. According to the basic threshold model, the transistor is turned off, and there is no conduction between drain and source. A more accurate model considers the effect of thermal energy on the Boltzmann distribution of electron energies which allow some of the more energetic electrons at the source to enter the channel and flow to the drain. This results in a sub-threshold current that is an exponential function of gate–source voltage. While the current between drain and source should ideally be zero when the transistor is being used as a turned-off switch, there is a weak-inversion current, sometimes called sub-threshold leakage. In weak inversion the current varies exponentially with VGS as given approximately in (1):

$$ID \approx IDO\, e^{\frac{Vgs-Vt}{nVT}} \quad (1)$$

Where IDO= current at VGS=VTH, the thermal voltage VT=KT/Q and the slope factor *n* is stated in (2):

$$n = 1 + C_D/C_{OX} \quad (2)$$

With C_D = capacitance of the depletion layer and C_{OX} = capacitance of the oxide layer. In a long-channel device, there is no drain voltage dependence of the current once VDS>>VTH, but as channel length is reduced drain-induced barrier lowering introduces drain voltage dependence that depends in a complex way upon the device geometry (for example, the channel doping, the junction doping and so on). Frequently, threshold voltage V_{th} for this mode is defined as the gate voltage at which a selected value of current I_{D0} occurs. [4] Some micro-power analog circuits are designed to take advantage of sub-threshold conduction. By working in the weak-inversion region; the MOSFETs in these circuits deliver the highest possible transconductance-to-current ratio almost that of a bipolar transistor as in (3):

$$gm / I_D = 1/(nV_T) \quad (3)$$

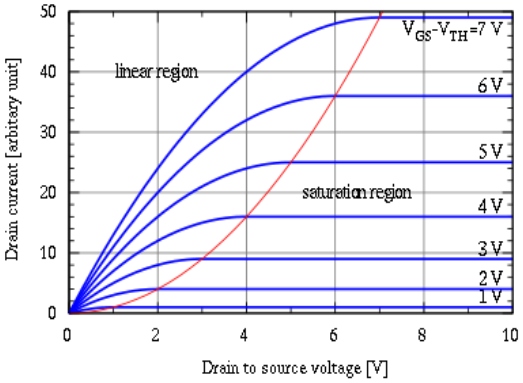


Fig 1. Sub-threshold I-V characteristics curve

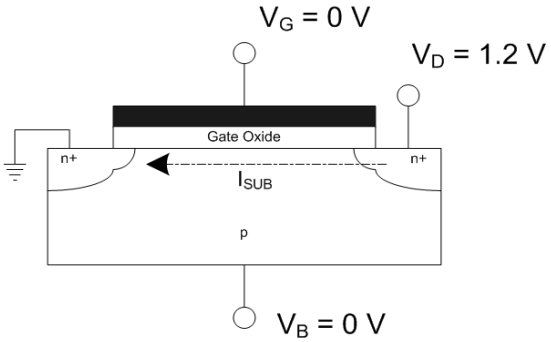


fig 2. Subthreshold conduction in MOSFET

The sub-threshold I–V curve shown in fig 1 depends exponentially upon threshold voltage, introducing a strong dependence on any manufacturing variation that affects threshold voltage; for example: variations in oxide thickness, junction depth, or body doping that change the degree of drain-induced barrier lowering. The resulting sensitivity to fabrication variations complicates optimization for leakage and performance. [5] Sub-threshold conduction or sub-threshold leakage or sub-threshold drain current in the MOSFET as shown in fig 2 is the current that flows between the source and drain of a MOSFET when the transistor is in sub-threshold region, or weak-inversion region, that is, for gate-to-source voltages below the threshold voltage. The sub-threshold region is often referred to as the weak inversion region**.**

III. CMOS LOGIC FAMILIES OPTIMAL FOR SUB-THRESHOLD CIRCUIT DESIGN

The low *V*dd results in a reduced *I*ON/*I*OFF ratio that can reduce robustness. Static CMOS gates continue to function in subthreshold, but because of enhanced problem of short-channel effects due to variations at nano scale, logic families other than CMOS may offer greater resiliency to certain variation sources such as voltage or process. Therefore, design of robust subthreshold logic circuits exploring logic families other than static CMOS is another open area for exploration. The following logic families have been identified as suitable for designing more robust and energy efficient subthreshold circuits.

3.1 SUBTHRESHOLD CMOS LOGIC

Sub-threshold CMOS logic operates with the power supply Vdd less than the transistors' threshold voltage VT. This is done to ensure that all the transistors are indeed operating in the sub-threshold region. In subthreshold region, for Vds>3kT/q, Ids becomes independent of Vds for all practical purposes. In analog design, this favorable characteristic has been extensively exploited as it provides an excellent current source that spans for almost the entire rail-to-rail voltage range The 3kT/q drop (about 78mV at T=300K) is practically

negligible compared to the Vt drop in the normal strong inversion region. In the normal strong inversion region, it is well-known that the optimum NMOS to PMOS ratio which will give a minimum delay is due to the ratio of NMOS and PMOS transconductance parameters. [6] In subthreshold region, however, the optimum ratio has a much wider range, due to the exponential ratio between the NMOS and PMOS currents. Static CMOS is the most common logic style used in sub-threshold due to its robustness. However, different metrics applied to static CMOS will vary broadly as process balance changes.

The inverter design shown in fig.3 operates only when vgs>VT i.e. the voltage from gate to source which is applied at the input terminal is greater than the threshold voltage of the device. The threshold voltage is the minimum voltage that is applied for the device to operate. The above cmos device also works when vgs<Vt i.e. for smaller voltage changes and there exists a exponential relationship and the small voltages that are produced are useful for ultra low level applications and this region is called the subthreshold region. Subthreshold CMOS logic operates with the power supply Vdd less than the transistors' threshold voltage VT. This is done to ensure that all the transistors are indeed operating in the subthreshold region. The NAND and NOR gates is designed in the subthreshold cmos logic is as shown in fig4 and fig.5 respectively. The disadvantage of sub cmos logic design is that it is more sensitive to process variations due to exponential dependency of weak inversion current on vgs and VT. It is sensitive to power supply variations It has good noise margin and excellent robustness.

3.2 SUBTHRESHOLD PSUEDO-NMOS LOGIC

The subthreshold Pseudo-NMOS inverter is shown in fig 6. To achieve some improvement in operating speed, we analyze subthreshold Psuedo-NMOS logic. To ensure that Pseudo-NMOS logic functions correctly, careful sizing of PMOS to NMOS ratio is a must. In subthreshold region, however, Pseudo-NMOS logic is much more robust than its strong-inversion counterpart. This is mainly because of the favorable device subthreshold characteristics, namely: excellent voltage-controlled constant current source characteristics and exponential relationship. The gate will continue to function correctly as long as the current for PMOS is within the bands of current for NMOS. With a few decades of varying current, the sizing ratio of PMOS to NMOS becomes less critical as wider range of the ratio value is now acceptable for the logic gate to function correctly. The NAND and NOR gates is designed in the subthreshold pseudo NMOS logic are shown in the fig.7 and fig 8 respectively.

3.3. SUB-DTMOS LOGIC

Sub-DTMOS logic provides an alternative way to achieve the stability with direct substrate biasing without using any additional control circuitry. Sub-DTMOS logic uses transistors whose gates are tied to their substrates as the substrate voltage in sub-DTMOS logic changes with the gate input voltage, the threshold voltage is dynamically changed. In the off-state, i.e., VIN = 0 (VIN =Vdd) for NMOS (PMOS), the characteristics of DTMOS transistor is exactly the same as regular MOS transistor. Both have the same properties, such as the same off-current, subthreshold slope, and threshold voltage. In the on-state, however, the substrate-source voltage is forward- biased and thus reduces the threshold voltage of DTMOS transistor. The reduced threshold voltage is due to the reduction of body charge. The reduction of body charge leads to another advantage, namely higher carrier mobility because the reduced body charge causes a lower effective normal field. The reduced threshold voltage, lower normal effective electric field, and higher mobility results in higher on-current drive in DTMOS than that of a regular MOS transistor. Furthermore, the subthreshold slope of DTMOS improves and approaches the ideal 60 mV/decade which makes it more efficient in subthreshold logic circuits to obtain higher gain. Another significant advantage of the sub-DTMOS logic is that it does not require any additional limiter transistors, which further reduces the design complexity. In contrast, in the normal strong inversion region, the limiter transistors are necessary to limit the forward-biased to be less than 0.6 V. This is to prevent forward-biasing the parasitic PN junction diode while allowing a much higher power supply to be used in the circuit [8].

There are two different topologies in subthreshold DTMOS logic. The first one is Standard DTMOS logic uses transistors whose gates are tied to their substrates. However in standard DTMOS topology the body-drain capacitor forms a Miller capacitance that may eliminate any gain from added current drive. The second style of DTMOS uses minimum-sized auxiliary devices to augment the current drive by manipulating the body bias. In this style any excess current caused by forward biasing is used to charge/discharge the output. The gates of auxiliary devices are tied to main transistor's drain instead of gate. The higher on-current of sub-DT-CMOS logics causes them to have higher power consumption, but they can switch much faster than regular sub-CMOS logic. We propose using a new style of DT-MOS transistors in sub-threshold logics. The proposed inverter circuit designed using cadence tool is shown in fig 9. As it can be seen in this inverter, drains are tied to substrates. Where the n-transistor body is low, causing a weak transistor trying to pull down the output against a strong p transistor. Using this style of DT-MOS in sub-threshold logics, favorable conditions can be obtained to maximize gain and minimize leakage currents in the transistors. The standard DT-CMOS only while the

transistor is driving the output and proposed DT-CMOS at all other times can minimize leakage. The NAND and NOR gates is designed in the SubDTMOS logic are shown in the fig.10 and fig 11 respectively.

3.4 Sub-Domino Logic

Domino logic is a CMOS-based evolution of the dynamic logic techniques based on either PMOS or NMOS transistors. It allows a rail-to-rail logic swing. It was developed to speed up circuits. These logic circuits, however, can be operated only at lower frequencies due to lower supply voltage. To increase the frequency of operation, Sub domino logic has been proposed. Sub-domino logic is similar to conventional domino logic except the transistors are operated in sub-threshold region. There exist two types of Sub-Domino logic in which the dynamic node (i.e. the input to CMOS inverter) is pre-charged high in one case and pre-charged low in the other. Static CMOS inverter is needed to enable cascading of similar logic gates. Domino logic circuits are usually faster than static counterparts, and require less surface area, but are more difficult to design, and have higher power dissipation . This work discuses several domino circuit design techniques to reduce the power dissipation of domino logic while simultaneously improving noise immunity. When the clock is low, the NMOS device is cutoff while the PMOS is turned ON. This has the effect of disconnecting the output node from ground while simultaneously connecting the node to Vdd. Since the input to the next stage is charged up through the PMOS transistor when the clock is low, this phase of the clock is known as the "precharge" phase. When the clock is high however, the Cutoff and the bottom NMOS is turned ON, thereby disconnecting the output node from Vdd and providing a possible pull-down path to ground through the bottom NMOS transistor. This part of the clock cycle is known as the "evaluation phase", and bottom NMOS is called the "evaluation NMOS". When the clock is in the evaluation phase, the output node will either be maintained at its previous logic level or discharged to GND. In other words, the output node may be selectively discharged through the NMOS logic structure depending upon whether or not a path to GND is formed due to inputs of the NMOS logic block. If a path to ground is not formed during the evaluation phase, the output node will maintain its previous voltage level since no path exists from the output to Vdd or Ground for the charge to flow away. The sub domino logic inverter is as shown in the fig 12. In a domino logic cascade structure consisting of several stages, the evaluation of each stage ripples the next stage evaluation, similar to a domino falling one after the other. Once fallen, the node states cannot return to "1" (until the next clock cycle) just as dominos, once fallen, cannot stand up. The structure is hence called Domino CMOS Logic. It contrasts with other solutions to the cascade problem in which cascading is interrupted by clocks or other means. The NAND and NOR gates is designed in the Sub-Domino logic are shown in the fig.13 and fig 14 respectively.

3.5 SUBTHRESHOLD PASSTRANSISTOR LOGIC

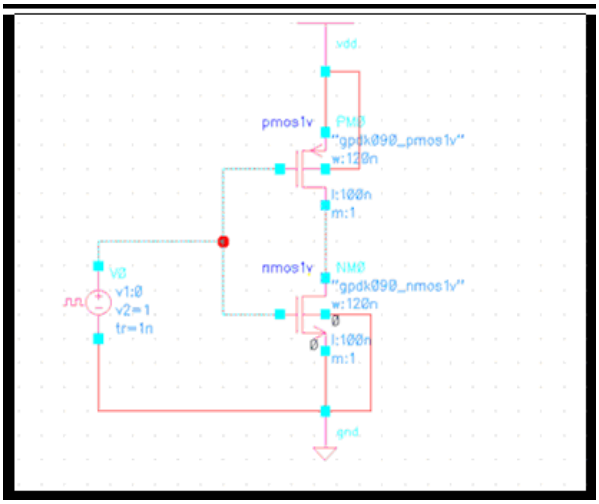
The subthreshold PTL inverter design is as shown in the figure 15. In contrast to classic static CMOS logic, in PTL two input logic signals are applied at the gate and at the drain of a MOS transistor. Considering an ideal case, without load, the transistor is saturated when its gate and drain voltages are equal to *VDD*. Thus, the source voltage is *VDD-VT*. However, the source will be in high impedance state for 0V gate voltage, no matter what the drain voltage is. Therefore, another NMOS is added and sources are connected to a single node to ensure that the logic function is valid for both values of the input logic signals. A significant disadvantage of PTL is that the output voltage is lower than the input and that it does not allow series connections of large numbers of transistors [9]. The addition of a static inverter, recovers the voltage swing to appropriate values. The NAND and NOR gates is designed in the Subthreshold PTL are shown in the fig.16 and fig 17 respectively.

3.6 Sub threshold Dynamic Threshold PT (DTPT) Logic

One of the major concerns in the subthreshold operation is the sensitivities to the temperature and the process variation which is common to all subthreshold logics. Using DTMOS in pass-gate logic is a fairly new idea. Restoration has commonly been used to alleviate the drop problem by assisting the pass-gate pull-up at the output. DTMOS could be substituted for restoration in pass-gate logic, but a combination of the two can help scale the voltage even further.. The augmented circuit style needed to be customized for pass gate logic, so a second auxiliary device was added to provide a new, symmetric design. Pass-transistor logic can continue to be used in low-power applications and that a combination of DTMOS and restoration can provide the best performance. The Sub- DTPT logic inverter is as shown in fig 18. The NAND and NOR gates is designed in the Subthreshold DTPT logic are shown in the fig 19 and fig 20 respectively.

IV. Design And Simulations

The circuits are designed in cadence and the designed circuits are simulated using 90nm technology circuit simulation tools. The simulation waveforms clearly depict the advantages in different logic families that are operating subthreshold region. The designs and simulation waveforms of different CMOS logic family circuits are as in the following figures:



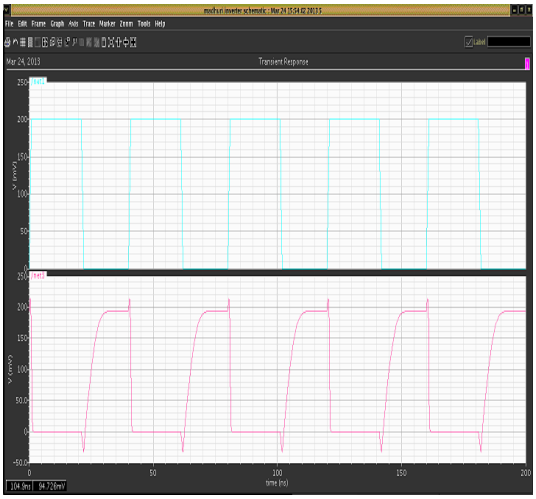
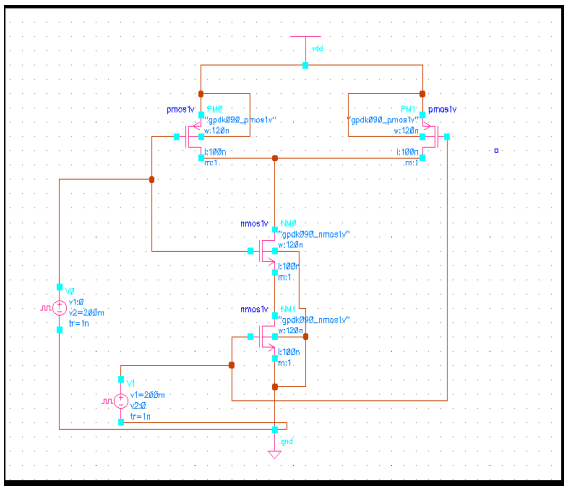


Fig 3. Design and simulation of subthreshold CMOS inverter



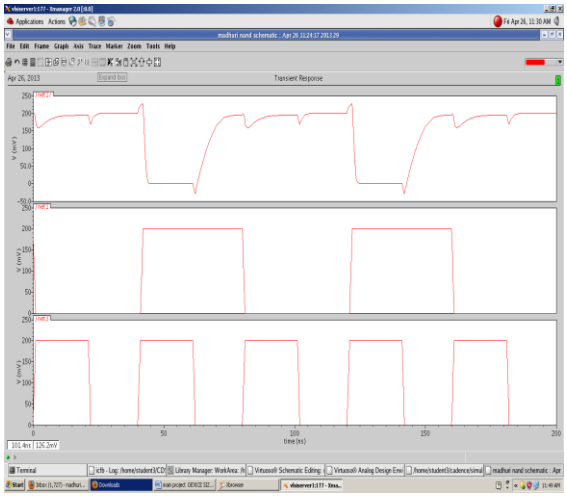
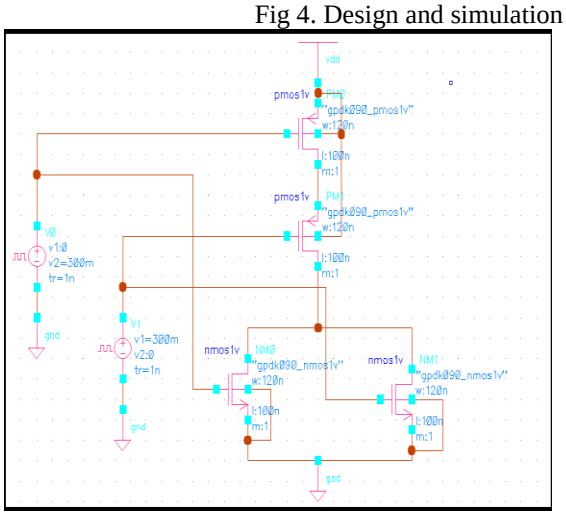


Fig 4. Design and simulation of Subthreshold CMOS NAND gate



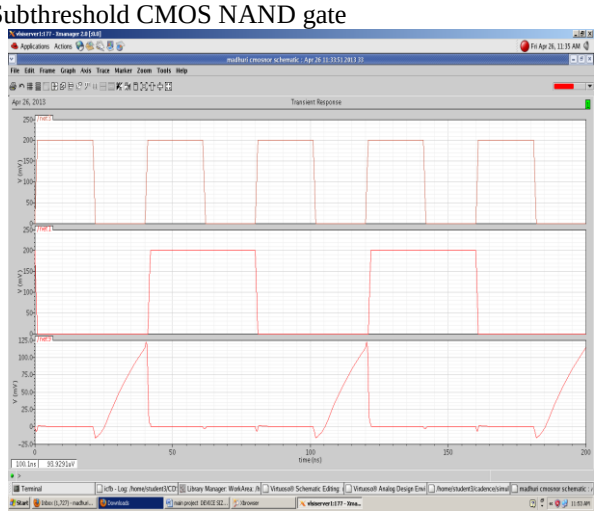


fig 5. Design and simulation of Subthreshold CMOS NOR gate

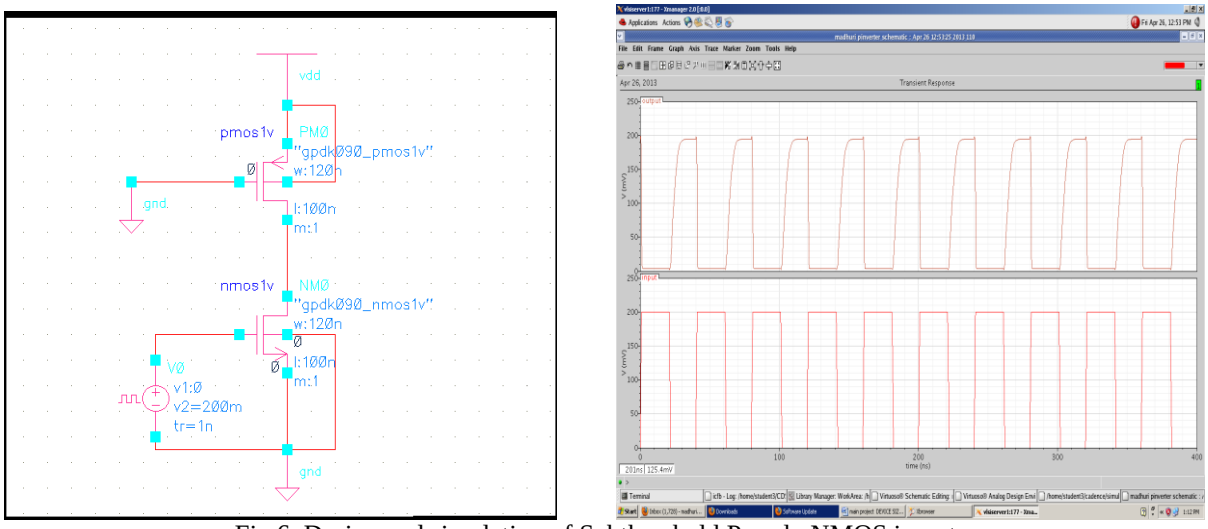


Fig 6. Design and simulation of Subthreshold Pseudo NMOS inverter

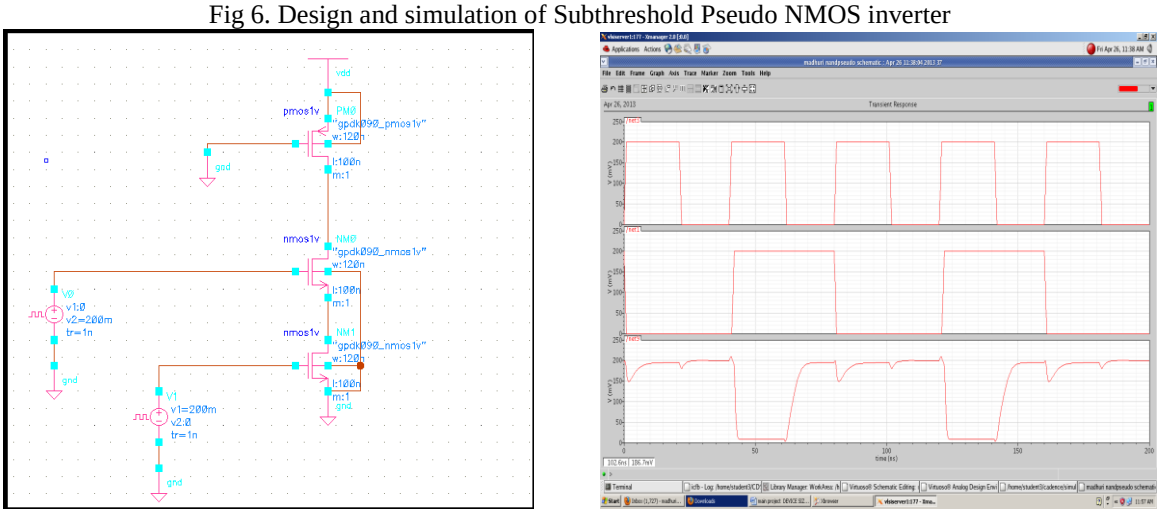


Fig 7. Design and simulation of Subthreshold Pseudo NMOS NAND gate

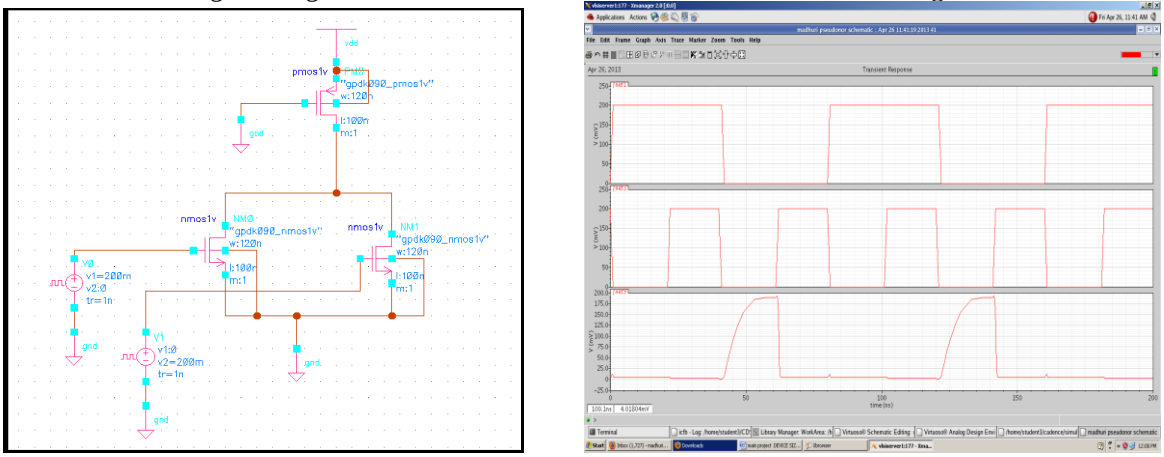


Fig 8.Design and simulation of subthreshold Pseudo-NMOS logic NOR gate

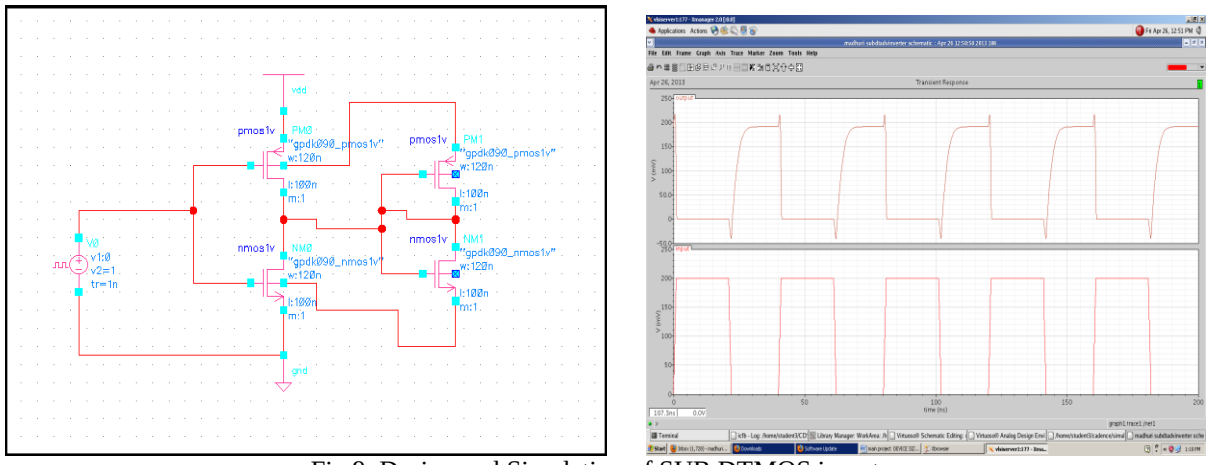


Fig 9. Design and Simulation of SUB DTMOS inverter

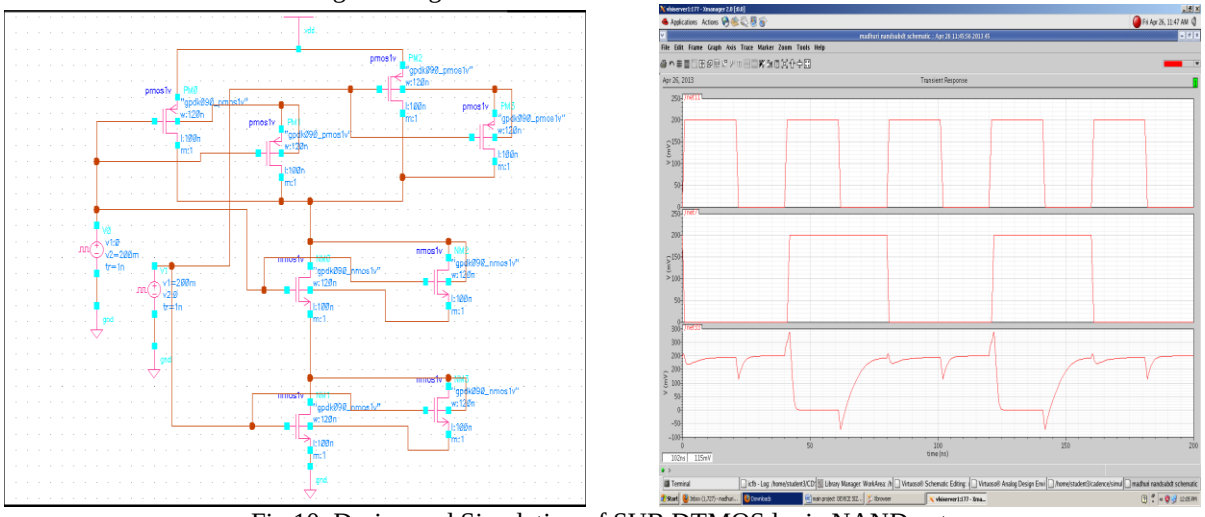


Fig 10. Design and Simulation of SUB DTMOS logic NAND gate

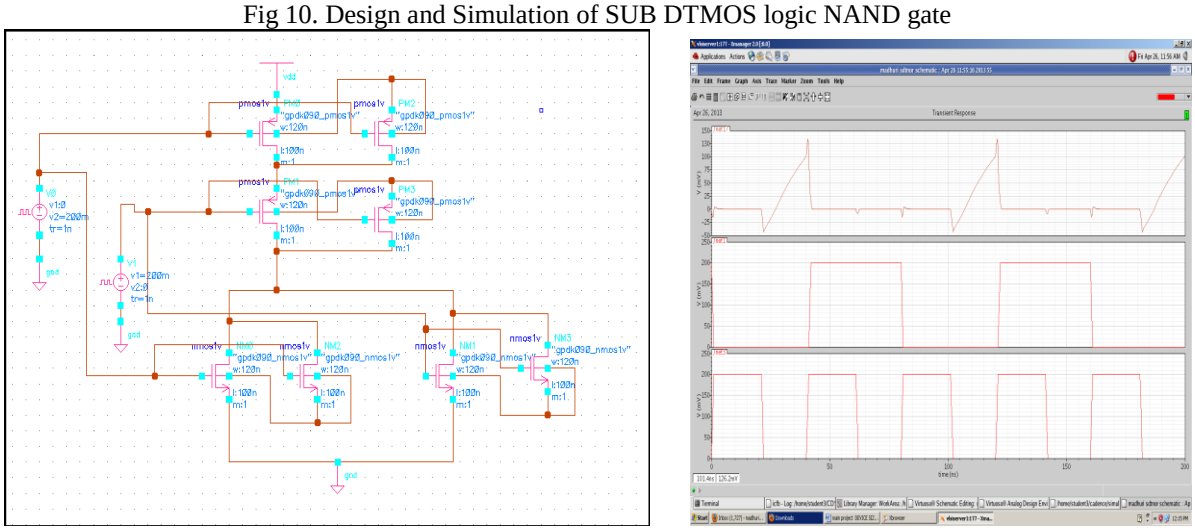


Fig 11. Design and Simulation of sub DTMOS Nor gate in subthreshold region

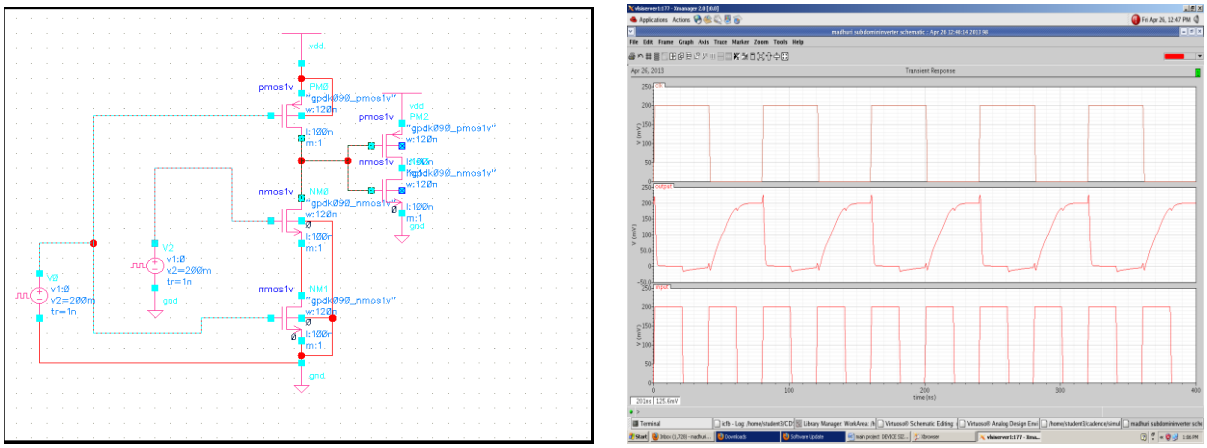


Fig 12. Design and simulation of Sub- Domino logic Inverter.

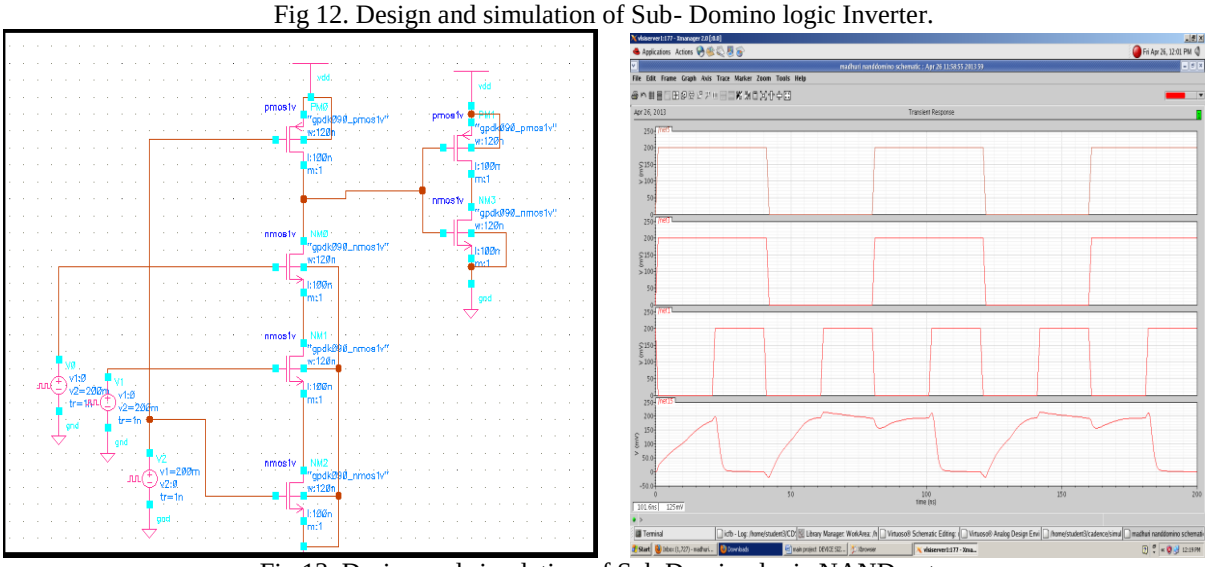


Fig 13. Design and simulation of Sub Domino logic NAND gate

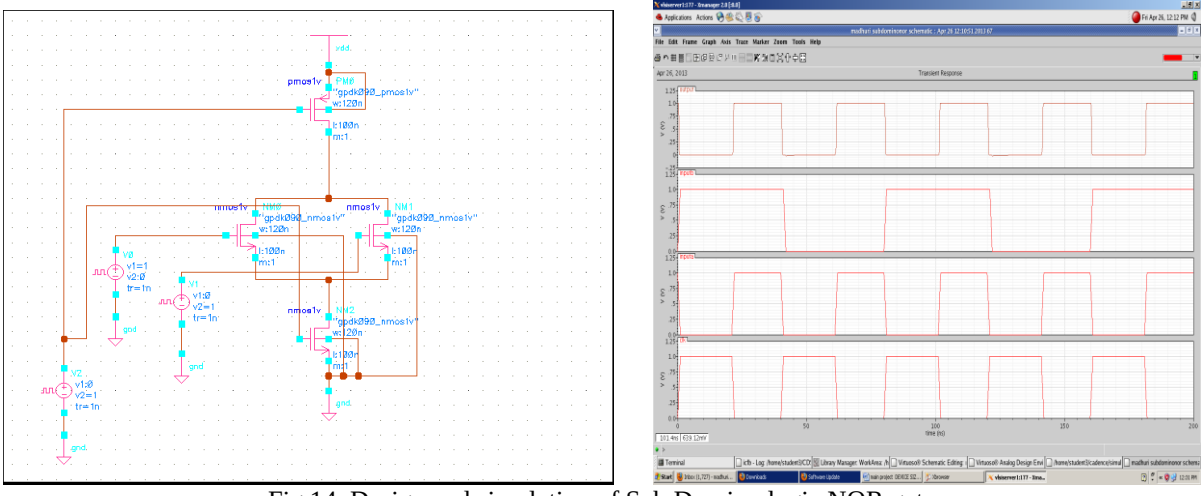


Fig 14. Design and simulation of Sub Domino logic NOR gate

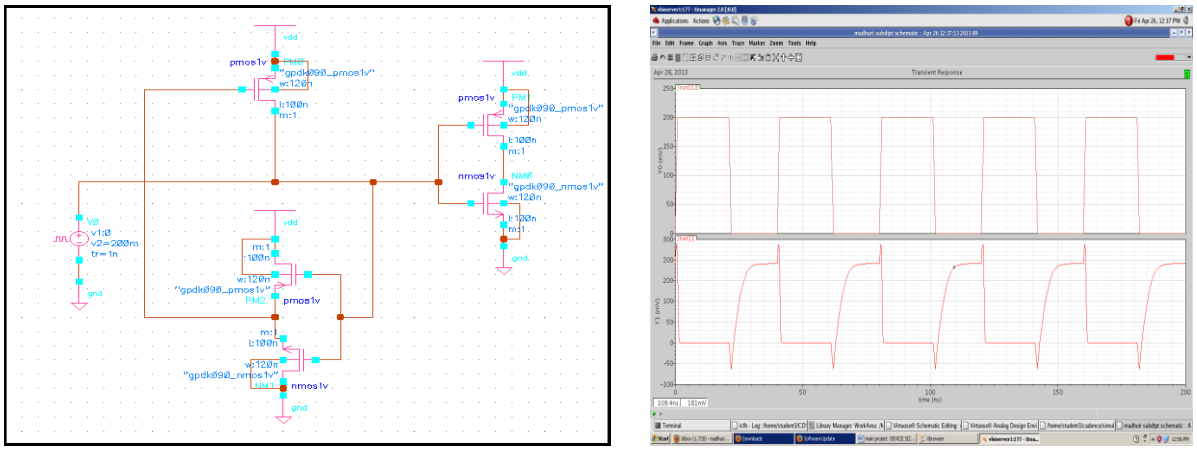


Fig 15. Design and Simulation of sub PT logic inverter in sub threshold region

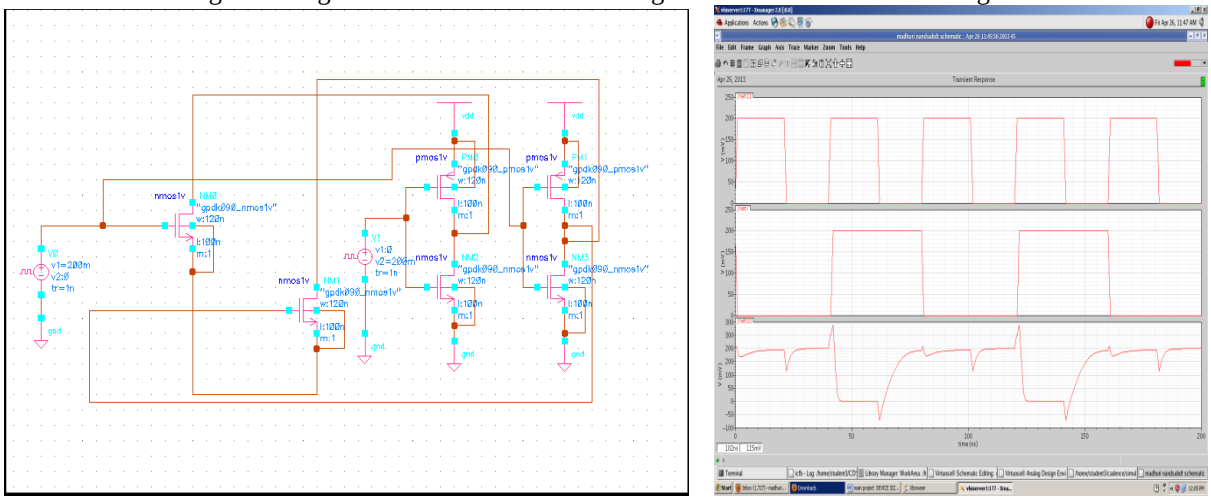


Fig 16. Design and Simulation of sub PT logic NAND gate in sub threshold region

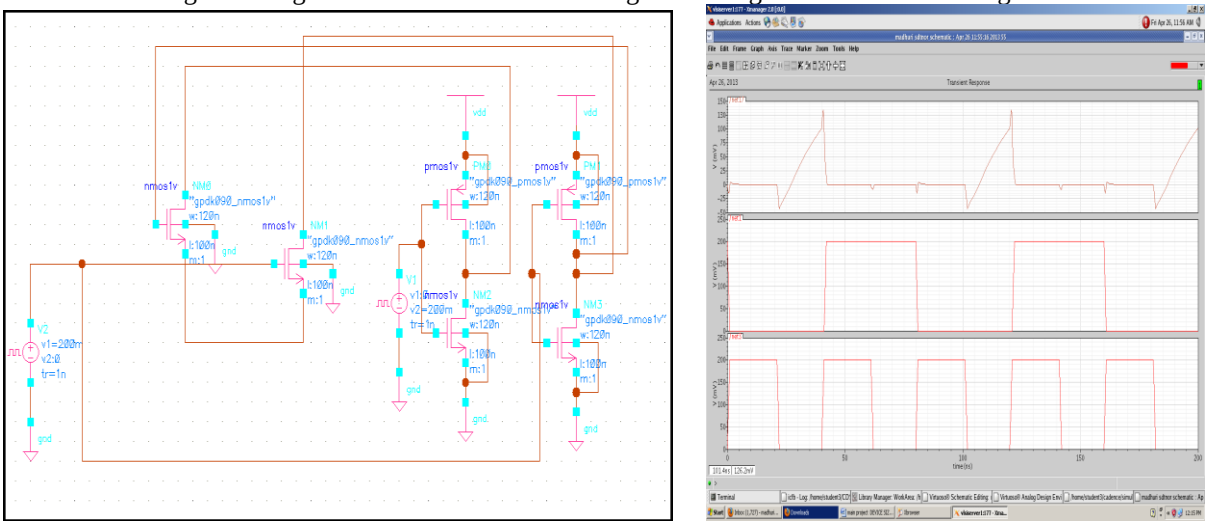


Fig 17. Design and Simulation of sub PT logic NOR gate in sub threshold region

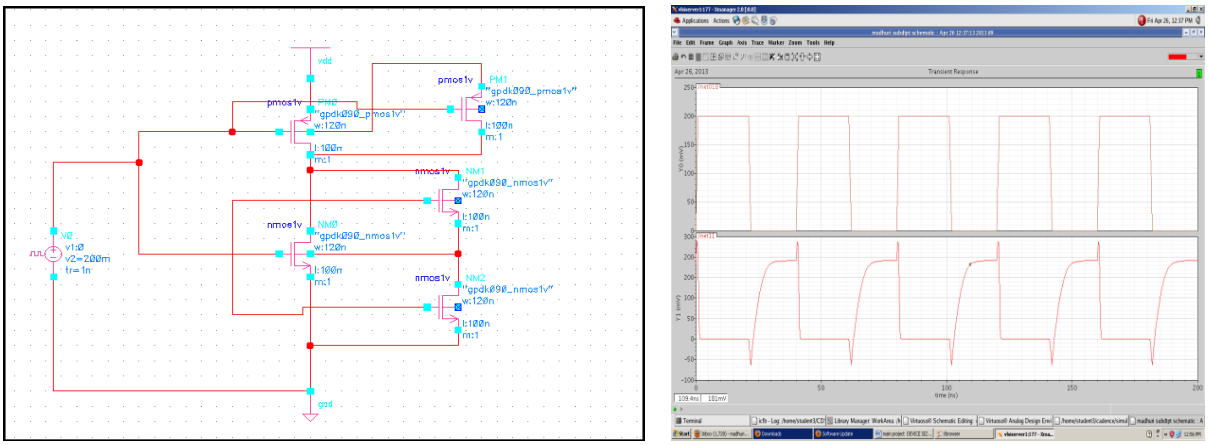


Fig 18. Design and Simulation of Sub DTPT inverter in subthreshold region

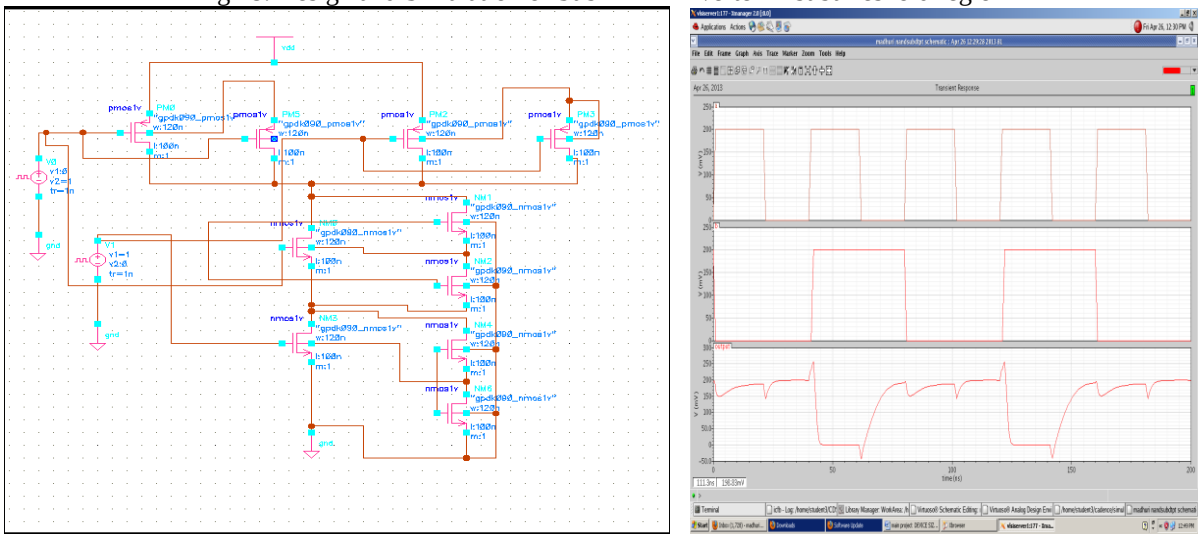


Fig 19. Design and Simulation of Sub DTPT logic NAND gate in subthreshold region

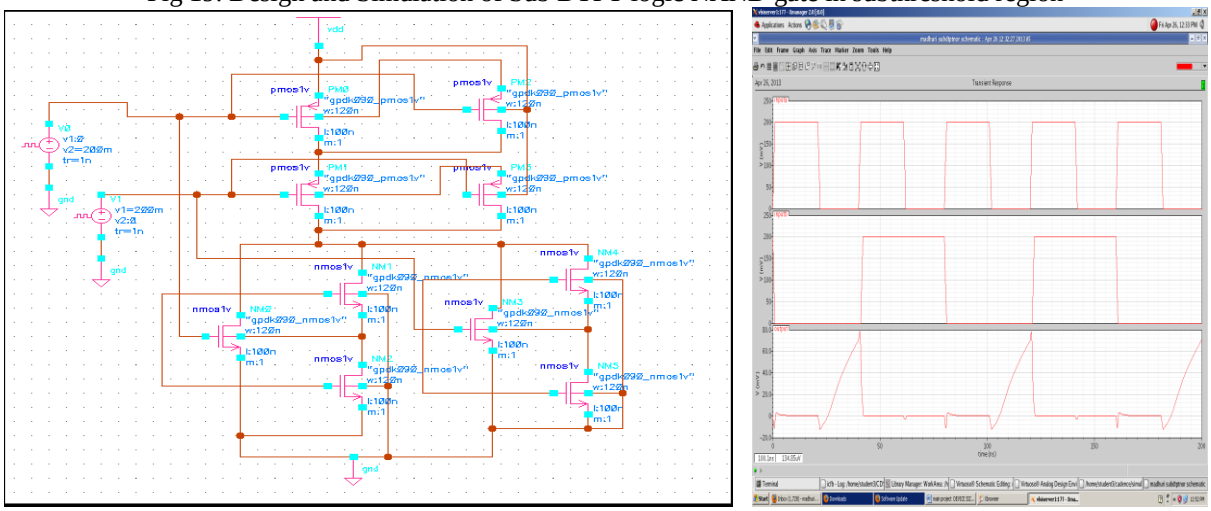


Fig 20. Design and Simulation of Sub DTPT logic NOR gate in subthreshold region

V. Results

The power and delay are calculated for different cmos logic families designed in subthreshold region and the obtained values are summarized and are compared in Table 1. From the table 1 mentioned below clearly indicates that the sub threshold dynamic threshold pass transistor logic is best for low power applications and sub threshold DTMOS logic is best for high speed applications in ultra low power applications.

Table1. Comparison Table

LOGIC FAMILY LOGIC FAMILIES		POWER POWER(W)	DELAY DELAY(S)
SUB CMOS	INVERTER	6.237e-10	6.764e-9
	NAND	5.86055e-9	6.5949e-8
	NOR	9.8404e-10	3.7147e-8
PSEUDO NMOS	INVERTER	1.745e-9	2.693e-9
	NAND	1.0564e-9	6.373e-8
	NOR	2.8515e-9	4.5198e-8
SUBPASS TRANSISTOR	INVERTER	2.27e-9	3.5373e-9
	NAND	1.3459e-9	6.544e-8
	NOR	1.6544e-9	4.9887e-8
SUB DTMOS	INVERTER	1.979e-9	2.47326e-9
	NAND	1.0514e-9	6.215e-10
	NOR	6.9214e-10	2.93474e-8
SUB DOMINO	INVERTER	9.9688e-10	2.9846e-8
	NAND	1.2145e-9	3.25e-9
	NOR	9.45032e-10	2.977e-8
SUB DTPT	INVERTER	9.69299e-10	3.63918e-9
	NAND	9.92257e-10	6.6394e-8
	NOR	5.752576e-10	4.9887e-8

VI. Conclusion

As technology continues to scale, subthreshold region has gained a lot of importance. This paper has explored the relevance of different CMOS logic families operating in the sub threshold region. Hence, using a basic inverter circuit as a comparison unit, it is shown that the sub threshold dynamic threshold pass transistor logic (sub DTPT) is best for ultra low power applications and sub dynamic threshold MOS transistor logic (sub DTMOS) has better speed when compared to other logic families. These designs can be used as library component for future design. The design can be extended for incorporating or implementing data path blocks like subtractor block, multiplier block and in many arithmetic blocks. Using latest technology and newer design techniques further modification can be implemented.

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