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Low Power Digital Signal Processor Architecture For Wireless Sensor Nodes By Using Parallel Prefix Technique

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Abstract:*Radio communication has highest energy consumption. To reduce the energy and power parallel prefix technique is used. This paper describes the design and implementation of newly proposed folded tree architecture. Folded tree architecture has two phases. They are trunk and twig phase. Normally the power is reduced to 60-70% compared to existing methods. Measurements of the silicon implementation show an improvement of 10-20 × in terms of energy as compared to traditional modern micro controllers found in sensor nodes. Commonly this technique is used to wireless communication.*
KeyWords:*Parallel prefix, Radio Communication, Wireless communication, Folded tree.*

I. Introduction

Wireless sensor network (WSN) applications are medical field, environmental sensing, industrial inspection and military surveillance. WSN node has three parts. They are sensors, radio, and micro controller. These three parts are combined with a limited power supply. Since radio transmissions are very expensive in terms of energy. The ratio of communication to computation energy cost range from 100 to 3000. So data communication must be traded for on the node processing which in turn can convert the many sensor readings into a few useful data values. The goal of this paper is to design low power WSN digital processor using parallel prefix technique.

II. Related Requirements For Processing

Two key requirements are used to improve existing processing and control architectures can be identified.

2.1 .Minimize Memory Access:

Modern micro controllers are based on the principles of divide and conquer strategy of ultra fast processors. In addition the lack of task specific operations leads to inefficient execution, which results in longer algorithms and significant memory book keeping.

2.2Combine Data and Control Flow Principles:

To manage the data stream and the instruction stream in the core functional unit, two approaches exist. Under control flow, the data stream is a consequence of the data stream. A traditional processor architecture is a control flow machine, with programs that execute sequentially as a stream of instructions. The data flow program identifies the data dependencies. The latter approach has been hugely successful in specialized high throughput applications, such as multimedia and graphics processing. The characteristics of wireless sensor networks are Data driven, Many to few, Application specific.

III. Existing Method

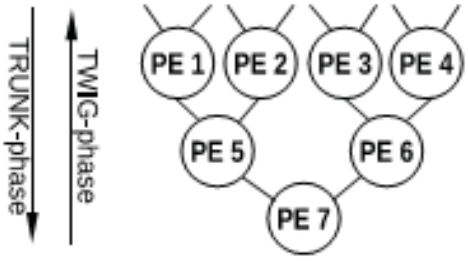


Fig. 3.1A binary tree.

In existing method binary tree is used. The disadvantages of this method is at a time only one node act as root nodes, other node act as leaves. So at a time only one data is send. Hence the power as well as energy is

increased. Time requirement is high and interconnection is high. The proposed approach gives the limited power and energy. The time requirement is low as well as interconnection path is increased. So Folded tree architecture is proposed to send the data in the way of wireless communication technique.

IV. Proposed Approach

4.1 Parallel prefix operations

In the digital design world, prefix operations are best known for their application in the class of carry look- ahead adders. The addition of two inputs A and B in this case consists of three stages. A bitwise propagate-generate(PG) logic stage, a group of logic stage, and a sum stage. The output of bitwise PG stage is given below.

Pi=Ai (xor) Bi , Gi = Ai . Bi

Group PG logic stage, which implements the following expression.

(Pi,Gi) (Pi+1,Gi+1) = (Pi.Pi+1, Gi+Pi.Gi+1)

Consider the given example A= "1001" and B= "0101" are added together. The bitwise PG logic of LSB first noted A={1001} and B={1010} returns the PG pairs for these values are(P,G)={(0,1);(0,0);(1,0);(1,0)}The carry array results are G = {1,0,0,0}.The sum results are S= {0,1,1,1}.The prefix element of the ordered set [3,1,2,0,4,1,1,3] is ∑ai=15. To calculate the prefix operations need two phases. They are Trunk phase and twig phase. In trunk phase the data is transmitted in the way of folded tree architecture. Twig phase is used to receive the data. The saved elements of trunk phase and twig phase are same. But the input of trunk phase and output of twig phase are different. The first two values of the input of trunk phase are denoted as left and right side value. Each left side value is saved, the saved element is called Lsave. Left side value only saved then it is added to the right side value. Again this value is saved to left side and The explanations of trunk and twig phases are given below.

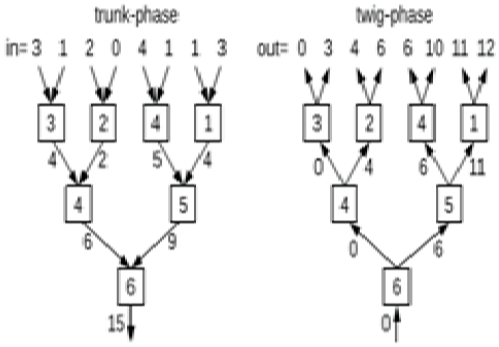


Fig.4.1.1. Example of a prefix calculation with sum operator using Blelloch generic approach in a trunk and twig phase.

4.2 Trunk phase:

In the trunk phase the left value L is saved locally as Lsave and it is added to the right value R, which is passed on toward the root. This continues until the parallel prefix element 15 is found at the root. Note that each time, a store and calculate operation is executed.

4.3.Twig phase:

The twig phase starts, during which data moves in the opposite direction, from the root to the leaves. Now the incoming value, beginning with the sum identity element 0 at the root, is passed to the left child, while it is also added to the previously saved Lsave and passed to the right child. In the end, the reduced prefix set is found at the leaves.

4.4 Folded tree:

To use folded tree architecture the area and power is reduced. The idea here is to fold the tree back onto the itself to maximally reuse the PEs. In doing so, P becomes proportional to n/2 and the area is cut in half. Note that also the interconnect is reduced. On the other hand, throughput decreases by a factor of log(n) but since the sample rate of different physical phenomena relevant for WSNs does not exceed 100 kHz, this leaves enough room for this trade off to be made.

V. Programming And Using The Folded Tree

First the trunk phase is considered. The figure shows four processing elements. The letters L and R indicates left and right value of inputs A and B. According to Blelloch approach, L is saved as Lsave and the sum L+R is passed.

To see exactly how the folded tree functionally becomes a binary tree, all nodes of the binary tree are assigned numbers that correspond to the PE, which will act like that node at that stage. As can be seen, PE1 and PE2 are only used once, PE3 is used twice and PE4 is used three times. This corresponds to a decreasing number of active PEs while progressing from stage to stage. The first stage has all four PEs active. The second stage has two active PEs: PE3 and PE4. The third and last stage has only one active PE: PE4

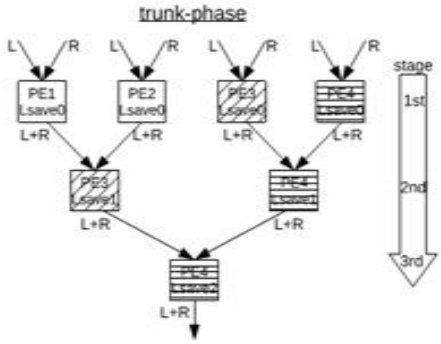


Fig. 5.1 Trunk Phase implementation

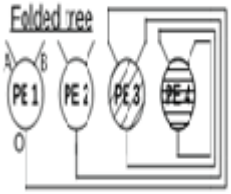
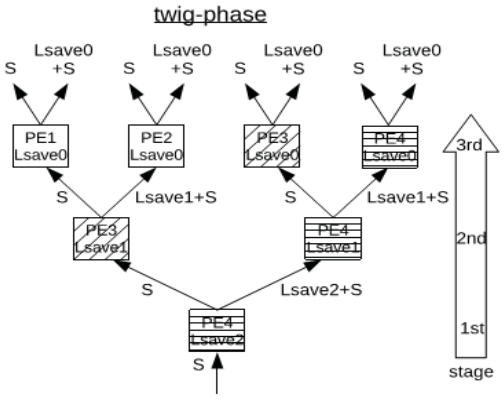


Fig. 5.2 Annotated twig phase graph of 4 PE folded tree.

More importantly, it can also be seen that PE3 and PE4 have to store multiple Lsave values. PE4 must keep three: Lsave0 through Lsave2, while Pe3 keeps two: Lsave0 and Lsave1. PE1 and PE2 each only keep one: Lsave0. The trunk phase PE program here has three instructions, which are identical, apart from the different RF addresses that are used. Due to the fact that multiple Lsave's have to be stored, each stage will have its own RF address to store and retrieve them. This is why PE4 needs three instructions, PE3 needs two instructions and PE1 and PE2 need one instruction.



In twig phase the tree operates in the opposite direction. According to Blelloch approach S is passed to the left and the sum S+L save is passed to the right. Note that here as well none of these annotations are global. The way the PEs are activated during the twig phase again influences how the programming of the folded tree must happen.

VI. Experimental Results

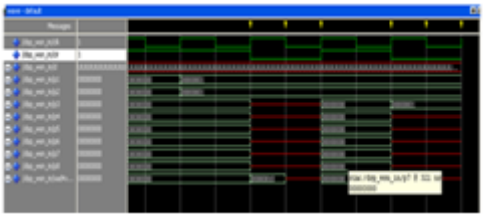


Fig. 6.1 Outputof folded tree architecture

This result shows eight inputs and only one output. Sad signal is used to select the path. At 250ns the data was transmitted. At this time the power and energy is saved. Hence the time requirement is low.

Table6.1
Leakage Power and Dynamic Energy for One PE under nominal conditions (20 mhz, 1.2v)

PE	Active PE core	Idle PE core	PE instr. Mem
Dynamic energy (PJ)	14.6	4.7	2.10
Leakage power (µW)	0.03	0.03	0.01
Total power (µW)	41.7	13.5	6.0

The PE table in Table 1 gives the dynamic energy and leakage power for one PE core running at 20 MHz and 1.2 V supply under full stress with varying data inputs. It consumes 42 µW or 2.1 µW/MHz, including 0.03 µW leakage. The register based instruction memory power values are presented in last column of the PE table and consume 6 µW. When going into idle mode, a processing element will consume 60 percentage (60%) less than in active mode.

VII.Conclusion

This paper describes the folded tree architecture of a digital signal processor for WSN applications. The design exploits the fact that many data processing algorithms for WSN applications can be described using parallel prefix operations, introducingthe much needed flexibility energy is saved to the following conditions.

1)Limiting the data set by pre processing with parallel prefix operations.
2)The reuse of the binary tree as a folded tree

The future Scope of this project is the end of architecture router is included. It is used to reduce the delay as well as congestion.

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