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# PV panel based Half Bridge Three level DC/DC Converter using Capacitor Voltage Control Strategy

M. Narender Reddy[1], P. Sravan Kumar[2], G. Revan Sidda[3]
[1](Asso.prof, Dept of EEE in Aurora's Scientific Technological and Research Academy, (JNTUH), INDIA)
[2](Sr.Asst. Prof, Dept of EEE in Aurora's Scientific Technological and Research Academy, (JNTU-H), INDIA)
[3](Asst. Prof, Dept of EEE in Aurora's Scientific Technological and Research Academy, (JNTU-H), INDIA)

***Abstract :*** *Three-level (TL) dc–dc converters are widely used in high-voltage input applications for the reason that the voltage stress on the power switches is only half of the input voltage. For the half-bridge TL dc–dc converter, the asymmetry of the main circuit and drive circuit result in voltage unbalance among the input divided capacitors and blocking capacitor, which will cause higher voltage stress on the power switches and the rectifier diodes. This paper proposes a novel capacitor voltage control strategy based on PV panel to adjust duty cycle and phase shift of the positive and negative half-cycles so that the voltage of the input-divided capacitors and blocking capacitor are corrected and the reliability of the converter can be guaranteed. An 800-V input from the PV panel to 28-V/2-kW output simulation is done. The experimental results are shown to verify the theoretical analysis and the proposed control strategy*

***Keywords:*** *PV Source Modeling, Capacitor voltage control, half-bridge three-level (TL) converter, voltage unbalance.*

## I. INTRODUCTION

**T**HREE-LEVEL (TL) converters have the advantages that the voltage stress on the power switches is only half of the input voltage [1] so that they are very suitable for the high-voltage input applications, such as subway, high-speed train, ship-electric-power-distribution system, and so on [2]–[4]. Meanwhile, half-bridge TL dc–dc converters can achieve zero-voltage switching (ZVS) of the power switches [5].Ruan *et al.* [6] presented the derivation process of half-bridge TL converter and the voltage stress of each switch is half of the input voltage $V_{in}$ . However, because of the asymmetry of the switches in series and the drive circuits, the switches suffer different voltage stress when they are shut down. So the free-wheeling diodes are introduced to ensure that the voltage stress on the switches is $V_{in}$ /2 [7]. But the outer two switches have to be shut down prior to the corresponding inner switches to keep the converter operating normally. In order to decouple the switching process of the two switches in series, the flying capacitor is employed [8], [9]. Then, there is no limit to the switching sequence of the outer and inner switches. The converter achieves ZVS for the switches with the use of a leakage inductor and the output capacitors of the switches. But, the rectifier diodes suffer volt-age oscillation and spikes. In order to solve this problem, Ruan *et al.* [10], [11] introduced two clamping diodes to eliminate the oscillation and clamp the rectified voltage. The input-divided capacitors will be paralleled with the flying capacitor though the clamping diodes, respectively, in different switching mode. If the voltage of the flying capacitor is not equal to $V_{in}$ /2, the voltage difference between the input-divided capacitors and the flying capacitor will result in large current spike surges through the clamping diodes and damage them. Considering of the re-liability of the clamped diodes and conduction losses of the freewheeling diodes, Barbi *et al.* [12] proposed the four-switch half-bridge TL converter without clamping diodes and flying capacitor. It can still make sure that the voltage stress of four switches is $V_{in}$ /2 and has no rush current in circuit. However, if the voltage of the input divided capacitors and blocking capacitor is not equal to $V_{in}$ /2, the voltage stress on the power switches and the rectifier diodes will be raised and damage the converter.

Based on the four-switch half-bridge TL converter [12], a novel capacitor voltage control strategy is proposed to correct the voltage unbalance and keep the converter operating safely.

## II. PV SOURCE MODELING

PV generator as input source has significant effect on the converter dynamics. The nonlinear V −I characteristic of a PV generator can be modeled using current source, diode, and resistors. The single-diode model shown in Fig. 2 (a) is widely used for the PV source modeling. This model provides a trade- off between accuracy and complexity. Thevenin's equivalent model with non constant voltages and resistances has been proposed in to closely approximate the characteristic of PV generator. The Thevenin's based model provides simpler prediction and computation for the maximum power point of PV array under different operating conditions. Thevenin's theorem is not valid for a nonlinear model, but the nonlinear model could be represented by a linear one with non constant parameters. In for example, the piece- wise linearization is used

to linearize the diode. The parameters in Fig. 2(a) can be estimated using the manufacturer's datasheet. As shown in Fig. 2(b), the actual diode characteristic has been divided into three regions and the characteristic in each region is approximated as a straight line. Each line can be further represented by a set of voltage source $V_{x,n}$ and resistance one of the boundary points such that the operation at this point has no approximation error. The single-diode model of the PV generator with linearized diode is shown in Fig. 2(c), where the diode is approximated by the voltage source $V_{x,n}$ and resistance $R_d$ . The values of $V_x$ and $R_d$ are dependent on the operation region of the PV generator. The Thevenin's equivalent model of Fig. 2(c) is shown in Fig. 2(d). From the derivation in, the $V_{pv\_th,n}$ and $R_{pv\_th,n}$ can be calculated by

$$V_{\mathrm{pv\_th},n} = V_{x,n} + R_{D,n} \cdot \frac{R_{\mathrm{sh}} \cdot I_{\mathrm{ph}} - V_{x,n}}{R_{\mathrm{sh}} + R_{D,n}}$$

$$R_{\mathrm{pv\_th},n} = R_s + \frac{R_{\mathrm{sh}} \cdot R_{D,n}}{R_{\mathrm{sh}} + R_{D,n}}.$$

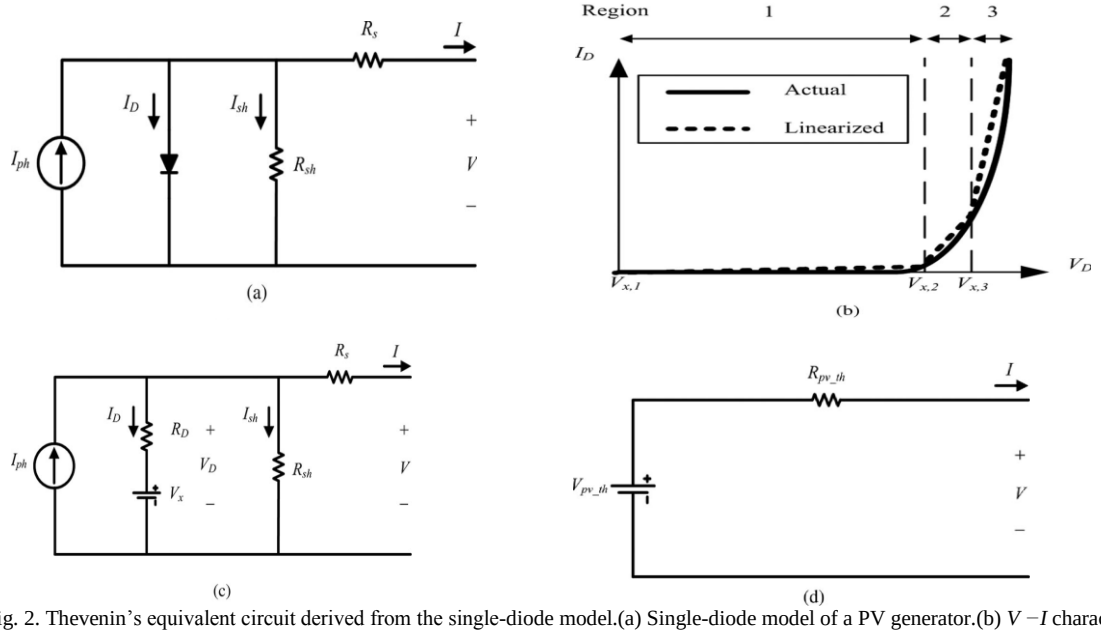


Fig. 2. Thevenin's equivalent circuit derived from the single-diode model.(a) Single-diode model of a PV generator.(b) $V-I$ characteristic of diode: actual
and linear approximation . (c) Single-diode model with linearized diode.(d) Thevenin's equivalent circuit for a single-diode model with linearized diode.

## III. Analysis Of Voltage Unbalance

Fig.3.1 (a) shows the main circuit and key waveforms of the half-bridge TL dc–dc converter. $C_{d1}$ and $C_{d2}$ are the input-divided capacitors. $C_b$ is the blocking capacitor. $Q_1$–$Q_4$ are the power switches, $D_1$–$D_4$ are the body diodes of $Q_1$–$Q_4$ , and $C_1$–$C_4$ are the parasitic capacitors of $Q_1$–$Q_4$ . $T_{R1}$ and $T_{R2}$ are the transformers, turn ratio (primary to secondary): $K$ . $L_{f1}$ and $L_{f2}$ are the output inductors. $D_{R1}$ and $D_{R2}$ are the rectifier diodes. Considering the duty cycle loss, $D_p$ is the duty cycle of the positive half-cycle, $D_n$ is that of the negative half-cycle. $T_{pf}$ is the freewheeling time of the positive half-cycle; $T_{nf}$ is that of the negative half-cycle. $T_s$ is the switching cycle. $v_{AB}$ is the voltage between $A$ and $B$, $i_p$ is the primary current, $V_{in}$ is the input voltage, $V_{Cb}$ is the voltage of $C_b$ , $V_{Cd1}$ and $V_{Cd2}$ are, respectively, the voltage of $C_{d1}$ and $C_{d2}$ . $V_o$ is the output voltage. $i_{DR1}$ and $i_{DR2}$ are the current of $D_{R1}$ and $D_{R2}$ . $i_{Lf1}$ and $i_{Lf2}$ are the current of $L_{f1}$ and $L_{f2}$ . $I_o$ is the output current

When the converter operates at a steady state, the magnetic flux distribution of the transformer is balanced. Operation modes are shown in Fig. 2(a)–(c), the equation can be derived:

$$(V_{\mathrm{in}} - V_{\mathrm{Cb}})\, D_{\mathrm{p}} T_{\mathrm{s}} = V_{\mathrm{Cb}} D_{\mathrm{n}} T_{\mathrm{s}}. \qquad (1)$$

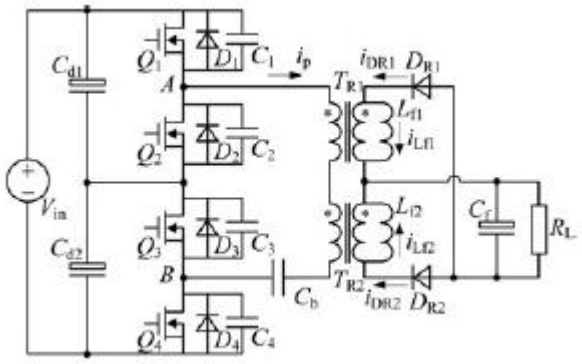

Fig. 3.1(a)

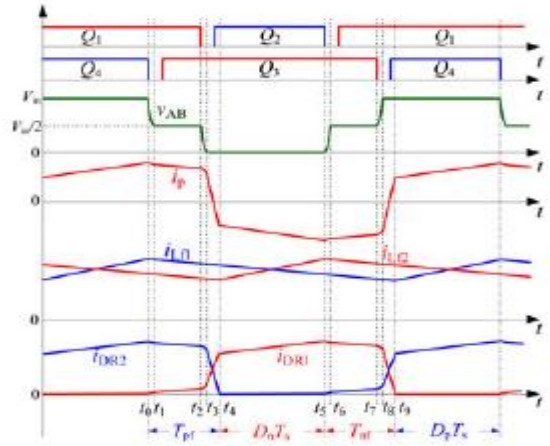

Fig. 3.1(b)

Fig. 3.1. Four-switch half-bridge TL converter. (a) Main circuit. (b) Keywaveforms.

In the ideal operation conditions, the driving signals are symmetrical and $D_p = D_n$, so $V_{Cb} = V_{in}/2$. In the freewheeling modes, as shown in Fig. 4.1(b)–(d), $T_{pf} = T_{nf}$ . The initial current of the freewheeling modes are equal, so $V_{Cd1} = V_{Cd2} = V_{in}/2$.

In practice, there is time delay of the control and drive circuits $D_p \neq D_n$, $T_{pf} \neq T_{nf}$ , which results in the voltage of the input divided capacitors and the blocking capacitor not equal to $V_{in}/2$. The voltage stress and current stress of the primary-side switches and rectifier diodes are raised. The detailed analysis is as follows.

**A. Duty Cycle Unbalanced of Positive and Negative Half-Cycles**

If $D_p \neq D_n$, $V_{Cb}$ can be derived from (1)

$$V_{Cb} = \frac{D_p V_{in}}{D_p + D_n}. \qquad (2)$$

If$D_p > D_n$, $V_{Cb} > V_{in}/2$; conversely, $D_p < D_n$, $V_{Cb} < V_{in}/2$. Let $D_p > D_n$, $V_{Cb} > V_{in}/2$, as shown in Fig. 4.2(a). Ignoring the process of soft switching, the ampere-second product of $C_b$ in $D_pT_s$, $D_nT_s$ is zero and the initial current $I_p$, $I_n$ in $T_{pf}$, $T_{nf}$ can be derived as follows:

$$I_p = \frac{D_n I_o}{K(D_p + D_n)} + \frac{V_o(1 - D_p)T_s}{2KL}$$

$$I_n = \frac{D_p I_o}{K(D_p + D_n)} + \frac{V_o(1 - D_n)T_s}{2KL} \qquad (3)$$

where $L$ is the output inductance. From (3), the average current and current ripple in $D_pT_s$ is smaller than in $D_nT_s$, $I_p < I$n, so there is voltage unbalance between the input-divided capacitors. $T_{pf} = T_{nf}$ , at steady-state, the ampere-second product of $C_{d1}$ is zero in $T_{pf}$ and $T_{nf}$

$$I_pT_{pf} = I_nT_{nf} \quad (4)$$

where $I_p$, $I_n$ are, respectively, the average current in $T_{pf}$, $T_{nf}$ .Then, $I_p = I_n$. Thus,$V_{Cd1} > V_{Cb}$ so that the primary currentin $T_{pf}$ is raised and in $T_{nf}$ is reduced. Finally, $I_p = I_n$. Therefore, it can be concluded that when $D_p \neq D_n$, if $D_p > D_n$, $V_{Cb}$ is higher than $V_{in}$ /2 and $V_{Cd1}$ is higher than $V_{Cb}$.

**B. Phase Shift Between Positive and Negative Half-Cycles is not 180◦**

the phase shift between the positive and negative half-cycles is not equal to 180◦, but $D_p = D_n = D$, as shown in Fig. 4.2(b),
from (2), $V_{Cb} = V_{in}$ /2.

If $T_{pf} \neq T_{nf}$ , let the angle of the phase shift between the positive and negative half-cycles be $180◦-\theta(\theta > 0)$, $T$pf, $T_{nf}$ are
derived as follows:

$$T_{pf} = \left(\frac{1}{2} - D\right)T_s - \frac{\theta}{180}T_s, T_{nf} = \left(\frac{1}{2} - D\right)T_s + \frac{\theta}{180}T_s. \quad (5)$$

So, $T_{pf} < T_{nf}$ . From (3), it can be drawn that $\boldsymbol{I_p} = I_n$. From(4), it can be drawn that $I_p > I_n$. So $V_{Cd1}$ must be higher than $V_{Cb}$ so that the current in $T_{pf}$ is raised and in $T_{nf}$ is reduced. Then, $I_p$ is higher than $I_n$. So $V_{Cd1} > V_{Cb} = V_{in}$ /2.Therefore, the conclusion can be drawn that when the phase shift between the positive and negative half-cycles is not equal to 180◦, the smaller the phase shift, the higher the $V_{Cd1}$. The voltage of the blocking capacitor $C_b$ is not affected.

## IV. Capacitor Voltage Control Strategy

This paper proposes a novel capacitor voltage control strategy to solve the issue of voltage unbalance among the blocking capacitor and the input-divided capacitors by regulating the duty cycle and phase shift. Fig. 4.3 shows the key waveforms of capacitor voltage control circuit. Triangle carriers $VTRI_1$ and $VTRI_2$ have the same amplitude and 180◦ phase shift. The driving signals $Q_2$ dri and $Q_4$ dri are generated by comparing the error signal of the output voltage regulator VEA Vo with $VTRI_1$ and $VTRI_2$, respectively, as Drive1 shows. In the ideal conditions, $Q_2$ dri,$Q_4$ dri , and the main circuit are absolutely symmetrical. The voltages of $C_{d1}$, $C_{d2}$, and $C_b$ are all equal to $V_{in}$ /2. Fig. 5 shows the capacitor voltage control circuit diagram. If voltage unbalance occurs in the converter, the operation process is analyzed in the following. Vof is the sampling voltage of Vo, $V_o$ ref is the voltage reference of the output, $V_{Cb}$ f is the sampling voltage of $V_{Cb}$, $V_{cin\ f}$ is the sampling voltage of $V_{in}$ , and $V_{Cd1}$ f is the sampling voltage of $V_{Cd1}$. VEA $C_b$ is the error output of the blocking capacitor voltage regulator, and VEA Cd is the error output of the input-divided capacitor Cd1 voltage regulator. The corrected signal VEA $C_b$ is added to VEA $V_o$ as $VEA_1$ and subtracted from VEA $V_o$ as $VEA_2$. VEA $C_d$ is added to $VEA_1$ as $VEA_3$ and subtracted from $VEA_1$ as $VEA_4$; VEA $C_d$ is added to $VEA_2$ as $VEA_5$ and subtracted from $VEA_2$ as $VEA_6$. $A_1$ and $A_2$ are generated by comparing $VEA_3$ and $VEA_4$ with $VTRI_1$, respectively, $A_3$ and $A_4$ are generated by comparing $VEA_5$ and $VEA_6$ with $VTRI_2$, respectively. $Clock_1$ and $Clock_4$ can be obtained by capturing the trailing edge of$A_1$ and$A_4$ with the trailing edge capture pulse generator, respectively, $Clock_2$ and $Clock_3$ can be obtained by capturing the rising edge of $A_2$ and$A_3$ with the rising edge capture pulse generator, respectively. $Clock_1$, $Clock_2$ generate $Q_2$ dri and $Clock_3$, $Clock_4$ generate $Q_4$ dri by the RS triggers.

In the blocking capacitor voltage control circuit, if $V_{Cb} < V_{in}$ /2, $V$EA $C_b$ is positive to increase $V$EA$_1$ and reduce $V$EA$_2$. So the duty cycle of$Q_2$ dri is reduced and that of$Q_4$ dri is increased, as *Drive*2 shows in Fig. 4.4. $V_{Cb}$ is raised quickly. Otherwise, $V_{Cb}$ is reduced quickly. Finally, $V_{Cb}$ is corrected to $V_{in}$ /2. In the voltage sharing circuit of the input divided capacitors, if $V_{Cd1} > V_{in}$ /2, $V$EA $C_d$ is negative to reduce $V$EA$_3$, $V$EA$_5$ and increase $V$EA$_4$, $V$EA$_6$. The pulse width of $A_1$,$A_3$ is increased and that of $A_2$,$A_4$ is reduced. The rising edge and trailing edge of $Q_2$ dri are all moved back, and those of $Q_4$ dri are all moved toward, as *Drive*3 shows. $T_{pf}$ is increased and $T_{nf}$ is reduced. So the time in which $C_{d1}$ is discharged is increased and $C_{d2}$ is charged is reduced. Thus, $V_{Cd1}$ is reduced. Otherwise, $V_{Cd1}$ is raised. Finally, $V_{Cd1} = V_{Cd2} = V_{in}$ /2.

From the analysis before, the blocking capacitor voltage control circuit and the divided capacitors voltage sharing circuit only regulate one controlled signal, respectively, so that the converter can tend toward stability quickly.

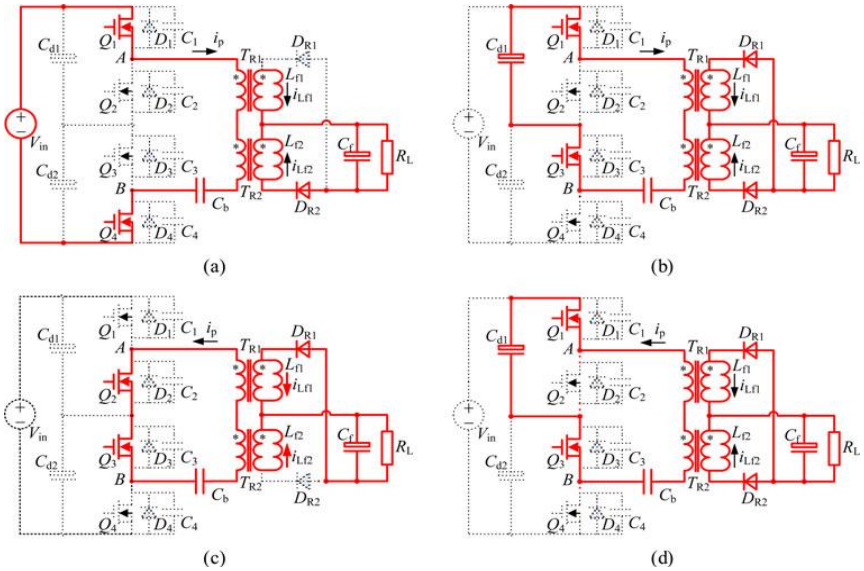


Fig. 4.1. Operation modes of the converter. (a) [Prior to $t_0$ ], (b) [$t_1$ –$t_2$ ], (c) [$t_4$ –$t_5$ ], (d) [$t_6$ –$t_7$ ].

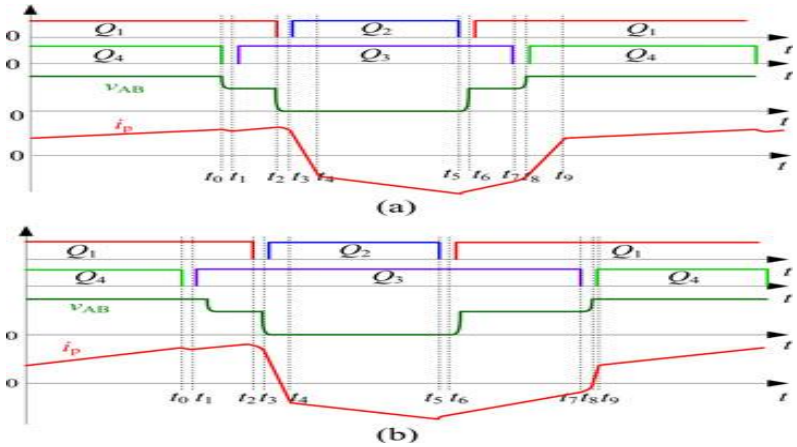


Fig. 4.2. Asymmetrical drive signals operation conditions. (a) Duty cycle unbalanced in positive and negative half cycles. (b) Phase shift of positive and negative half-cycles not 180◦.

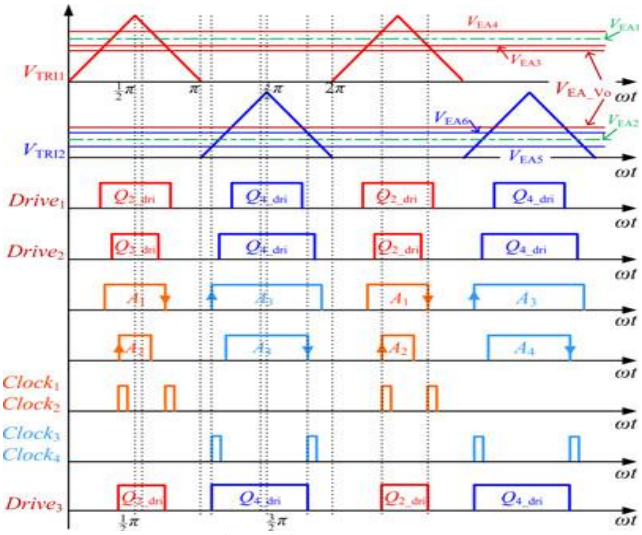

Fig. 4.3. Key waveforms of capacitor voltage control strategy

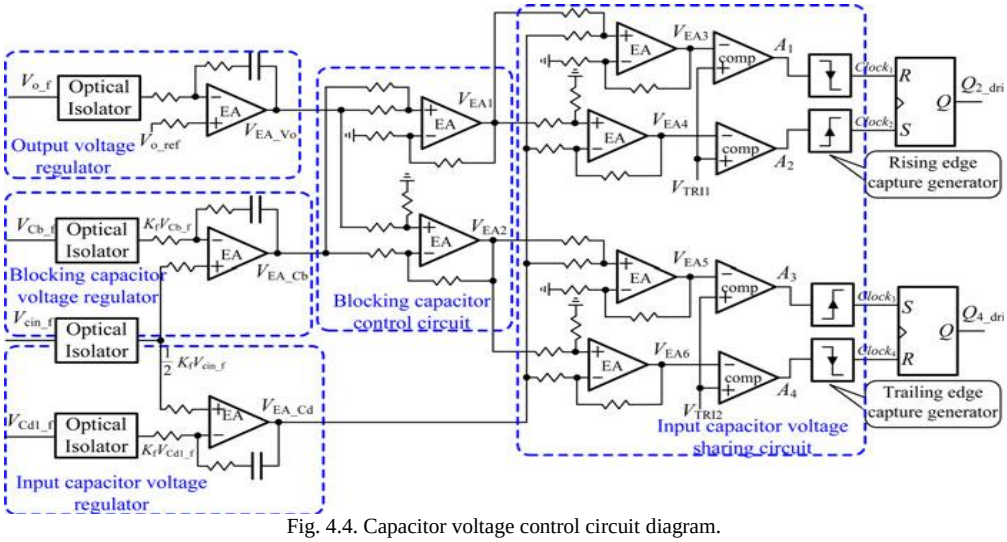


Fig. 4.4. Capacitor voltage control circuit diagram.

## V. CONCLUSION

This paper analyzed the reasons that result in voltage unbalance among the divided capacitors and blocking capacitor in the four-switch half-bridge TL converter. Then, a novel capacitor voltage control strategy was proposed to control the capacitor voltage by regulating the duty cycle and phase shift of the positive and negative half-cycles. Finally, an PV panel based 800-V input 28-V/2-kW output are verified the theoretical analysis.

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About the Authors:

M. Narender Reddy, Obtained his B.Tech Degree from JNTU in 2002, and he has done his post graduation in power electronics and Industrial drives in 2008 from J.N.T.U Hyderabad. He is currently pursuing Ph.D in energy systems, J.N.T.U Hyderabad. His research interests are in the area Energy systems, Power electronics and electrical machines. Presently, he is working as Associate professor and also heading the department of EEE at Aurora's Scientific, Technological & Research academy Hyderabad Andhra Pradesh, India. As the head of Department in he has published several papers and also organized various workshops for the benefit of the students.

Mr. P. Sravan kumar, at present is a Sr. Assistant Professor department of Electrical & Electronics Engineering, Aurora's Scientific, Technological & Research academy Hyderabad Andhra Pradesh, India. He received B.Tech. degree in Electrical and Electronics Engineering from J.N.T.U Hyderabad in2008 , M.Tech (Power Electronics) from J.N.T.U, Hyderabad India He published several papers in various National, International Conferences and Journals. His research interests accumulate in the area of Power Electronics, DC-DC Converters, and Renewable energy sources and Electrical Machines.

Mr. G. Revan Sidda , at present is a Assistant Professor department of Electrical & Electronics Engineering, Aurora's Scientific, Technological & Research academy Hyderabad Andhra Pradesh, India. He received B.Tech. degree in Electrical and Electronics Engineering from J.N.T.U Hyderabad in2010 , He is currently pursuing M.Tech (Power Electronics and Electrical Drives) from J.N.T.U, Hyderabad India. His research interests accumulate in the area of Power Electronics, Drives, DC-DC Converters, AC-DC Converters and Renewable energy sources and Electrical Machines.

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