Generation and Implementation of Barker and Nested Binary codes

A.NagaJyothi[1], K. Raja Rajeswari[2]

[1](Research Scholar, Department of Electronics & Communication Engineering, Andhra University, Visakhapatnam, India ,
[2](Professor Department of Electronics & Communication Engineering, Andhra University, Visakhapatnam, India

Abstract: *Recent advances in the development of semiconductors allow the realization of low cost hardware architecture for implementing Barker and Nested binary codes suitable for radar applications. Due to the fast development in Digital Signal Processors (DSP) they are used in radar signal processing. Radar signal processing is defined as exploitation of the received signal represented in digital form to extract the desired information while rejecting unwanted signals. DSP's are used for implementing many of the radar applications. FPGA based implementation of Barker and Nested binary codes are presented and are suitable for real time applications. FPGA provides a reconfigurable solution for implementing DSP applications. Since FPGA's can be reconfigured in hardware, FPGA's offers complete hardware customization for implementing various pulse compression codes. The implementation of Barker and Nested binary codes utilizes the Linear Feedback Shift Registers [LFSR], exhaustive search method. The performance of these codes is given in terms of MeritFactor(MF). The performance measures are calculated offline on a host PC in Matlab for the codes generated by VHDL program. The synthesized binary sequences have good MF values compared with previous work in the literature.*

Keywords: *Linear Feedback Shift Register(LFSR), Barker codes, Nested binary codes, Linear feedback shift registers, Merit Factor (MF), Auto Correlation function(ACF), Ambiguity Function (AF).*

I. INTRODUCTION

Phase coding in analog or digital form are widely used in power limited radar systems for pulse compression to achieve high range resolution. Recent advances in the development of semiconductors allow the realization of low cost hardware architecture for implementing Barker and Nested binary codes suitable for radar applications. Due to the cheap availability of Digital Signal Processors (DSP's), they are used in radar signal processing. Radar signal processing is defined as exploitation of the received signal represented in digital form to extract the desired information while rejecting unwanted signals. DSP processors are used for implementing many of the radar applications. Although DSP processors are programmable through software the architecture is not flexible. DSP processors are limited by fixed hardware architecture such as bus performance, fixed memory and fixed data widths. The DSP processor's fixed hardware architecture is not suitable for radar applications. Radar applications need customized functions, therefore most of the radar applications donot use DSP processors.

Turin.George.L [1] has given the methods for design and synthesis of matched filter. H.Orazi and et.al[2] proposed matched filter design using dispersive networks made with lumped constant .Y.Wang[3] used the theory of mutual exchange between clock frequency and design size via recursive delay line and implemented matched filter. Balaji.N[4] has proposed an VSLI architecture for generation of ternary codes with good discrimination factors. The best known binary sequences are the Barker sequences [5]. The existence of the Barker codes for length greater than 13 have not been found and Turyn [6] conjectured that no Barker sequences exist for lengths beyond 13. This has been proved by Rao and Deshpande [7]. Later radar systems designers started searching for binary biphase sequences. Levanon. N[8] has combined two binary barker sequences to form a longer length code by using Kronecker product and referred them as combined or Nested binary codes. With this correspondence, in this paper a novel and efficient VLSI architecture is proposed to implement Barker and Nested binary codes. This VLSI architecture is implemented on the FPGA as it provides the flexibility of reconfigurability and reprogramability.

The motivation behind this paper is to achieve the high mainlobe and low sidelobes, phase coded pulse compression codes which are widely used. The simple phase code is obtained from Binary phase coding, in which the phase of the radio frequency signal flips within the duration of the phase, according to the given binary codes. Output of the matched filter for biphase radar signals creates unwanted sidelobes which masks the useful information. Therefore the studies of polyphase codes are needed, and for this implementation techniques are carried out. The polyphase codes offers low sidelobes and are Doppler tolerant.

II. PHASE CODED WAVEFORMS

In this type of pulse compression, a long pulse of duration T is divided into N subpulses each of width τ. Bandwidth can be increased by changing the phase of each subpulse. The phase of each subpulse is chosen to be either 0 or π radians [8,9]. The output of the matched filter will be a spike of width T with an amplitude N times greater than that of long pulse. The output waveform extends a distance T to either side of the peak response, or central spike. In the output waveform the portions other than the main spike are called time sidelobes.

2.1 Binary Phase Coded Pulse Compression

It is a form of phase coded waveform which employs two phases i.e. 1 and -1. In this type of pulse compression method a long pulse of duration T is divided into N subpulses, each of width τ, where

$$\tau = T/N \qquad (1)$$

The phase of each segment is set to 0^0 and 180° in accordance with the sequence of element in the phase code as shown in Fig. 1.
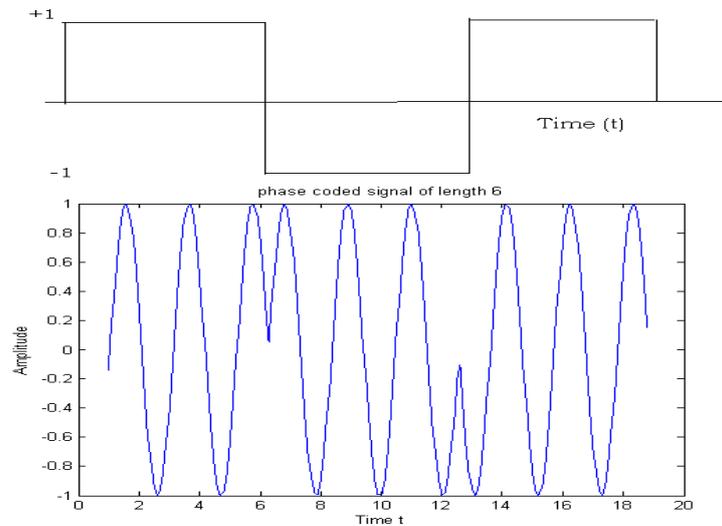
Figure 1 Graphical Representation of Binary phase coded waveform

2.2 Barker Codes

Barker code is a special type of binary code, which belongs to a class of sophisticated signal. The binary phase coded sequence of 0^0, 180^0 values that result in equal sidelobes after passing through the matched filter is called Barker code. A Barker is a sequence of N values of +1 and -1, for i=1 to N such that

$$x(n) = \sum_{j=1}^{n-1} a(j)a(j+1) \qquad for\,all \quad i = 1\,to\,n \qquad (2)$$
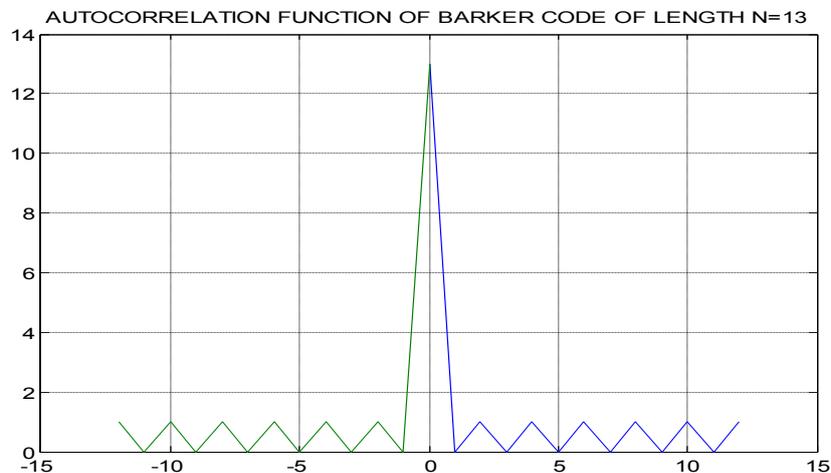
Figure 2 Auto Correlation Function of Barker code Length 13

2.3   Nested Barker Codes

Barker codes are the only biphase codes with smallest achievable sidelobes. However , the longest Barker code of odd length is proven to be of 13 [6] and considered to be major disadvantage. There is also a strong conjecture that Barker codes of length 2 and 4 are the only ones of even length. The code of length 13 achieves a mainlobe to peak side lobe ratio of only 22.8 dB which is less than the practical requirement of at least 30dB[9]. In literature mismatched filters are proposed to improve this ratio. In this paper Nested binary codes are considered and these has an improvement in PSLR compared to the Barker codes[10].

Nested binary codes can be obtained by using the Kronecker product of two Barker codes whose initial matched filter response is good. If an N-bit Barker code is denoted by B_N, and another B_M , then an MN bit code can be constructed as $B_N \otimes B_M$. The Kronecker product is simply the B_M code repeated N times, with each repetition multiplied by the corresponding element of the B_N code. For example, a 20 bit code can be constructed as the product $B_4 \otimes B_5$. These codes have a peak sidelobe greater than 1.
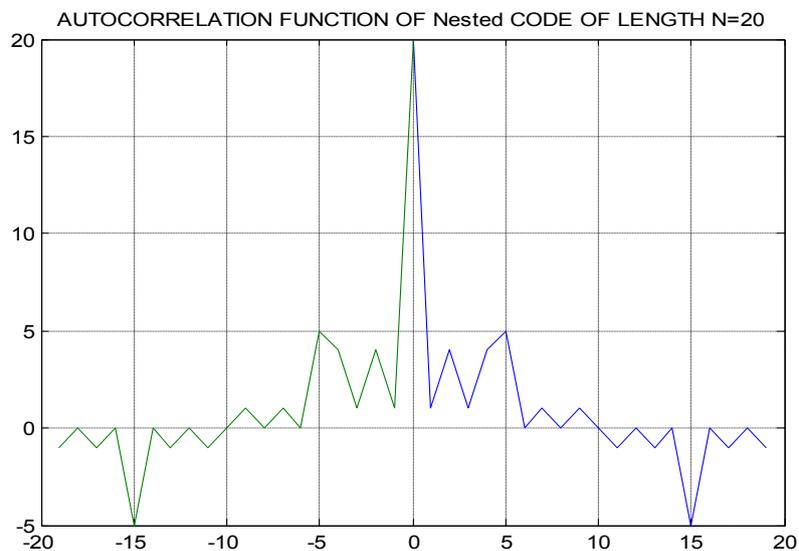
Figure 3 Auto Correlation Function of Nested binary code of Length 20

III.   SIGNAL CANDIDATES

A number of signals are designed for target identification. For comparison of signal performance, goodness measures are required. An ideal AF requires narrow central peak and low sidelobe. This implies that the ratio between mainlobe peak and sidelobe peak should be as high as possible. The concept of invariance property of AF is given in Levanon. N, Eli Mozeson in 2004 [8]. Invariance property says that the energy reduced at one place has to appear at another place. This requires that most of the energy is to be contained in the mainlobe and as less as possible in the sidelobe. Taking this principle into consideration the signal performances are evaluated. Most of the criteria given in literature are for ACF and these have been used for comparison [8-9,15-16]. In this paper an efficient VLSI architecture using LFSRs is proposed for generation of Barker and Nested binary codes with high MF values and are implemented on FPGA.

Merit Factor (MF): Merit factor, F, is defined as the ratio of energy in the mainlobe of Auto Correlation Function to the total signal energy in sidelobes.

$$MF = \frac{x^2(0)}{2 \sum_{k=1}^{N-1} x^2(k)}$$ (3)

IV.   METHODOLOGY FOR IMPLEMENTATION OF BARKER AND NESTED BINARY CODES

A binary sequences is a sequence of N bits, a_j for j=0,1,---N-1, i.e. n values will be of 0's and 1's and the ACF of such a sequence is given in Eq. 2. If m ones and zeros are present in a sequence then the duty cycle can be given as

$$c = (m - 1)/(N - 1)$$ (4)

The implementation of Barker and Nested binary sequence generator is based on LFSR which consists of 'n' D flip-flops. The generator produces predefined sequences of 1's and 0's.

4.1 Linear Feedback Shift Register (LFSR)

LFSR is a n-bit shift register with feedback to its input. The feedback is provided with XORing or XNORing the outputs of selected stages of the shift register which are referred as 'taps' by John G. Proakis[11] and then inputting this into the least significant bit (i.e. stage 0). Each stage has a common clock. The taps can be placed at any stage with XOR or XNOR feedback. The Least Significant (LS) bit of the shift register is shown at the left hand side of the shift register with the output being taken from the Most Significant (MS) bit from the right hand side and is shown in the Fig. 5.

The Fig 4. produces random sequence of Length 2^{n-1} states (n is no.of flip-flops). By the exhaustive search method the Barker code is selected. Peterson, William Wesley and Weldm E.J [17] proved that the LFSR sequences depend on the seed value (which is neither all zeros nor all ones), the tap positions and the feedback type.
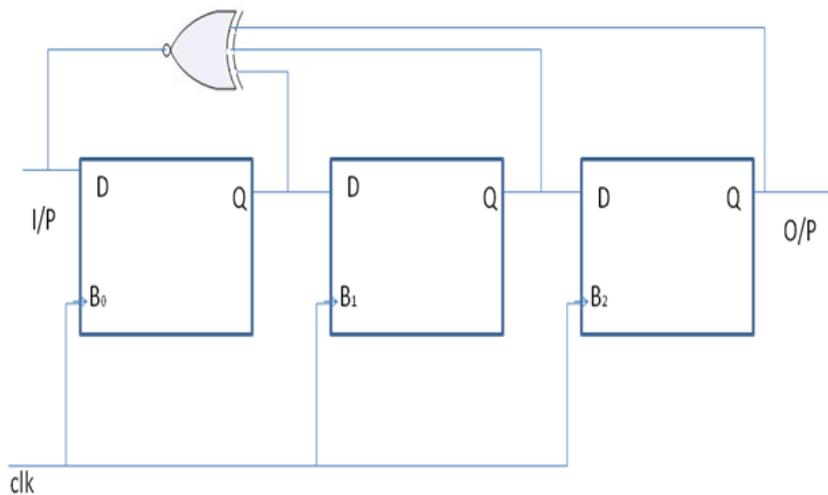
Figure 4 1:3 bit LFSR

Bo	B1	B2	Output Stream
0	1	0	
1	0	1	0
1	1	0	1
1	1	0	0
1	1	1	0
0	1	1	1
1	0	1	1
1	1	0	1
1	1	1	0

Table. 1: 1:3 bit LFSR sequence

Brown, Stephen D., and Zvonko G. Vranesic [13] stated that through feedback the system will be more stable and it will be free from errors. Table 3.2. is an example of LFSR and the initial value is set to 010. The output of the feedback is XNOR of B_0, B_1 and the output stream. One of the important component in LFSR is shift register and feedback loop.

Shift Register: A shift register is a device used for shifting its contents into adjacent positions within the register or to a position at the end of the register. The position from where the bit is shifted is left empty unless some new content is shifted into the position. The contents of a shift register are usually binary bits. If a shift register contains the bit pattern 1101 a shift to right would result in 0110; another shift yields 0011 [11-12].
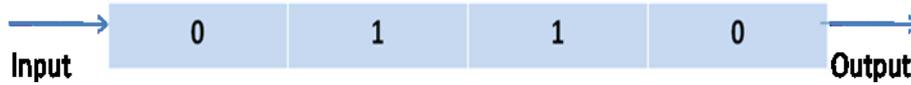
Figure 5. Shift Register

Clocking: One of the input to a shift register is the clock; a shift occurs in the register when this clock input changes state from one to zero. Activation of a shift is done by clock.

Shift Direction: A shift register can shift its contents in either direction. In this paper the shift direction is considered left to right.

Input and output: During a shift , the bit on the far right end of the shift register is moved out of the register. After a shift , the bit on the left end of the shift register is left empty unless a new bit is put into it. The input is fed through feedback action.

Feedback Mechanism: In LFSR, the bits contained in selected positions in the shift register are combined by using XNOR operation and the resultant is feedback as input bit. Sklar, Bernard[14] given that the selected bit values are collected before the register is clocked and the resultant of the feedback loop is inserted into the shift register during the shift, filling the position that is emptied .

V. DESIGN STRATEGIES

The concept of design strategies is to keep the design as portable as possible. It avoids using language features that are specific to a particular manufactures or target technology. This will make the program possible to use for different devices with a minimum of redesign [12].

5.1 Register Transfer Level (RTL) Design:

RTL description describes sequence of transfers between the registers but doesnot describe the hardware for these operations.

The steps in RTL design are
(1) The number and size of the registers needed to hold the data are to be determined.
(2) Logic and Arithmetic operations which are to be performed on these registers must be specified.
(3) Design of State machines is to be updated in order to achieve the desired results.

RTL design of Barker sequence and Nested binary sequences are composed of
(1) Registers and Combinational functional blocks called as the data path.
(2) Finite state machine called the controller that controls the transfer of data through the functional blocks and the registers.
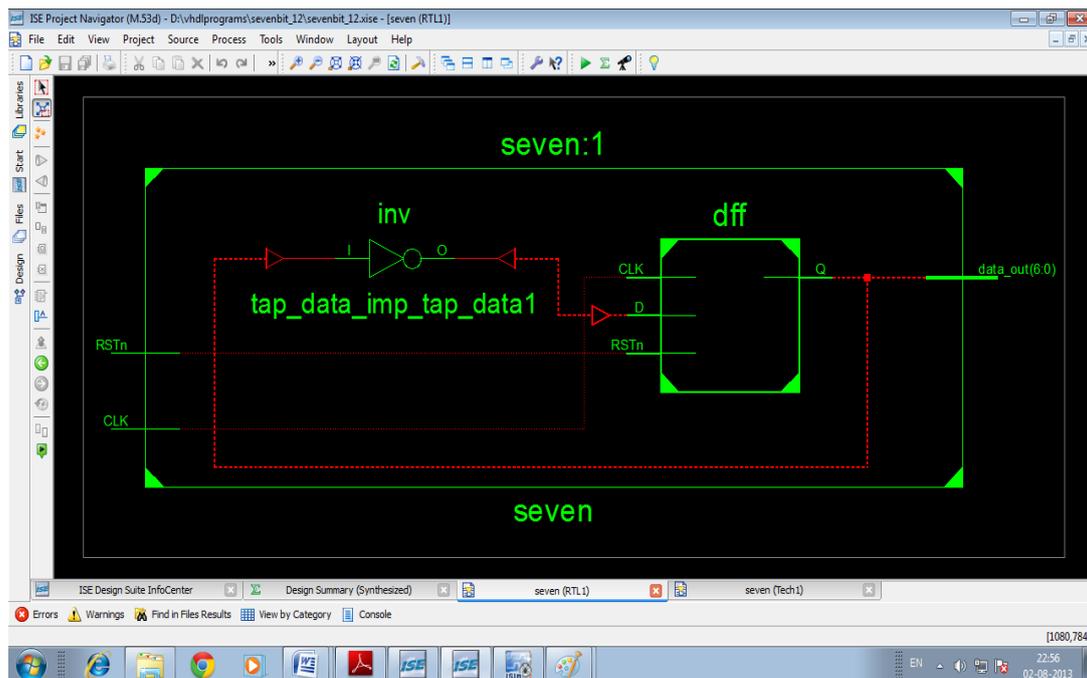
Figure6 RTL Schematic for Barker code of Length 7
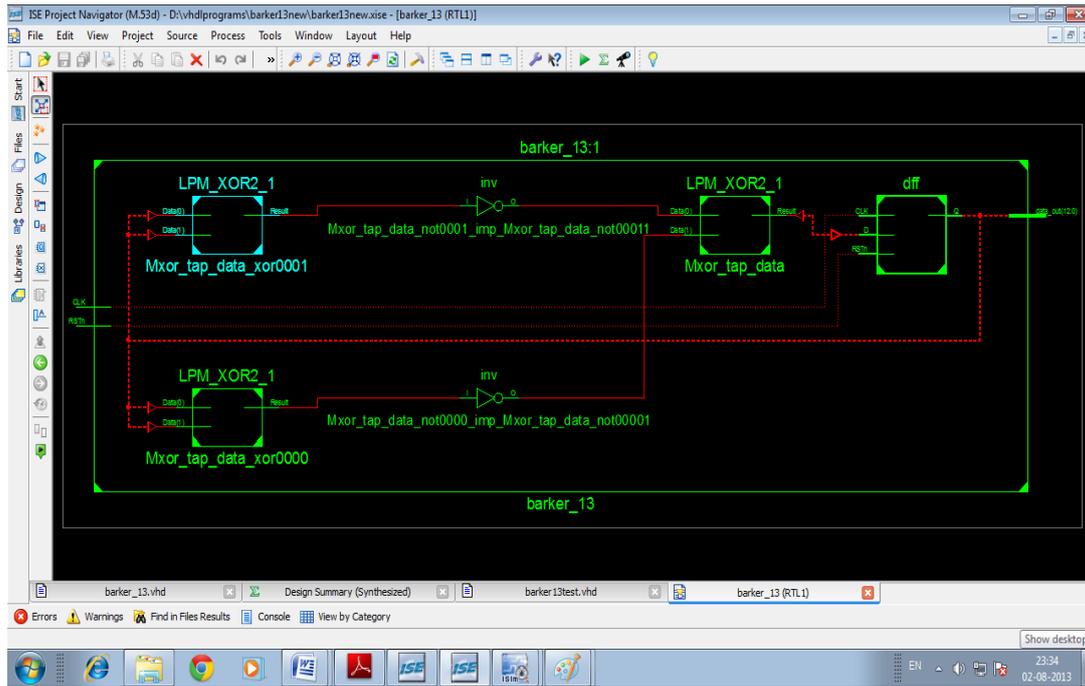
Figure 7 RTL Schematic for Barker code of Length 13
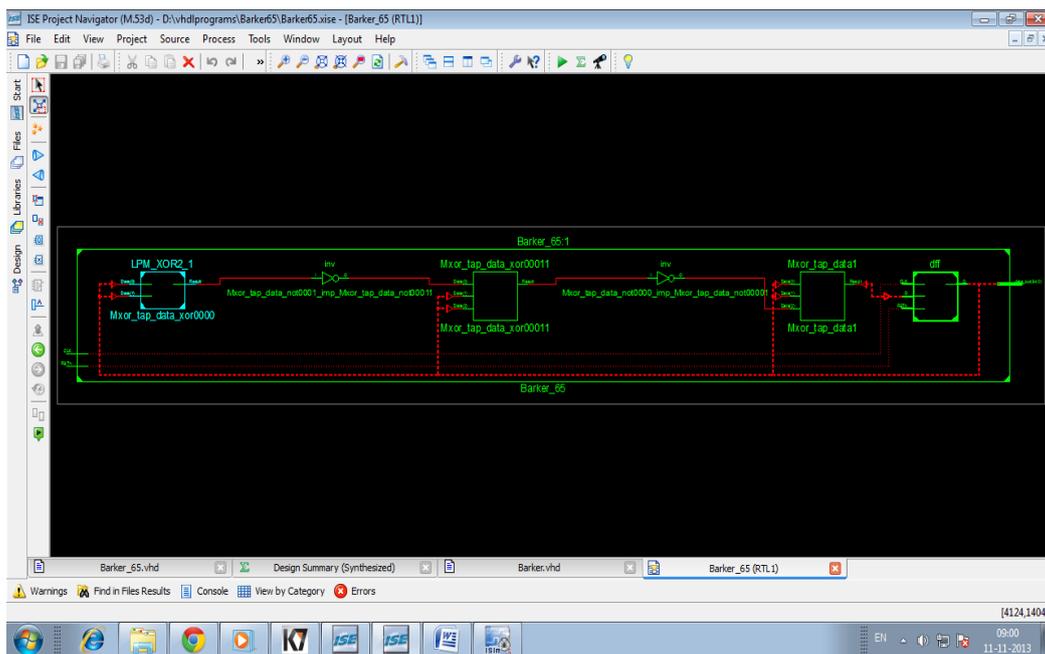
Figure 8 RTL Schematic for Binary code of Length 65

VI.   SYNTHESIS AND IN-CIRCUIT VERIFICATION

An efficient VLSI architecture for making exhaustive search for the identification of the best pulse compression codes is proposed and implemented for the design of binary sequences used in radar and communication systems for significantly improving the system performance. The architecture shown in Fig 4 has been implemented in VHDL for 7bit, 13 bit and 65 bit sequences and its synthesis was carried in Xilinx XST ISE foundation 12.1i. For Behavioral simulation, place and route simulation Xilinx ISE Modelsim@6.3 was used. The Barker 7 , Barker 13 and Nested binary code of length 65 were considered[10].
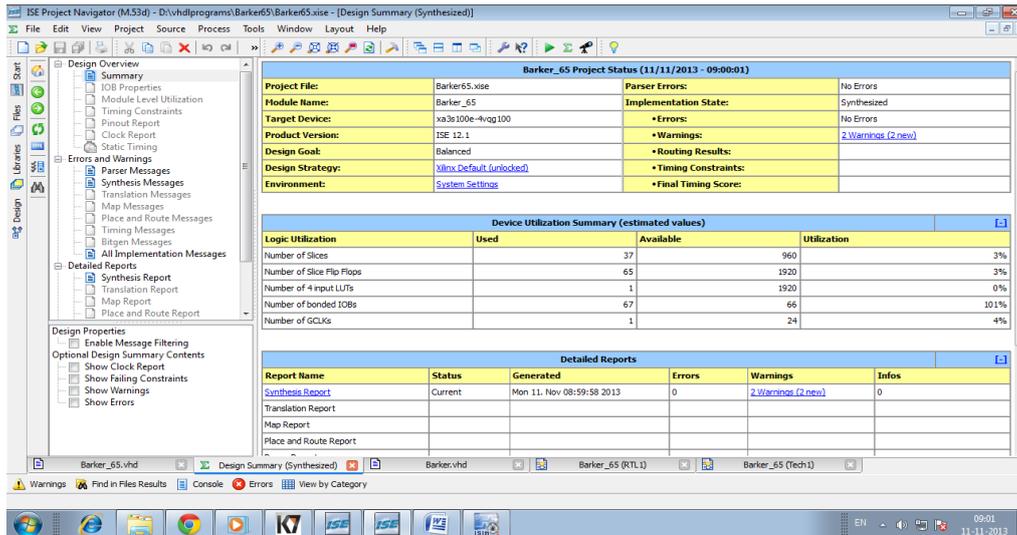
Figure 9 Design summary of Binary code of Length 65

VII.   Results

Exhaustive searches for obtaining good binary sequences by varying the tap positions are carried out at lengths of 7 to 65 and MF at different lengths are calculated. The values are tabulated in Table 2.

S.No	Length of the Sequence	Merit Factor(MF)
1	7	8.01
2	11	12.10
3	13	14.08
4	14	10.06
5	16	10.48
6	18	10.49
7	20	10.51
8	27	10.9
9	30	10.97
10	35	10.24
11	40	10.14
12	45	11.07
13	49	10.82
14	55	10.72
15	57	10.97
16	65	11.81

Table: 3 Merit Factor of binary sequences at different lengths

Fig 10 clearly shows the variation of MF with respect to the length of the sequence generated using LFSRs. The synthesized binary sequences have good MF compared to I A Pasha, 2000[18]. The synthesized binary sequences are promising for practical application to radars and communications. It is also proposed that the proposed architecture is giving good MF values for not only Barker sequences but also to Nested binary sequences.
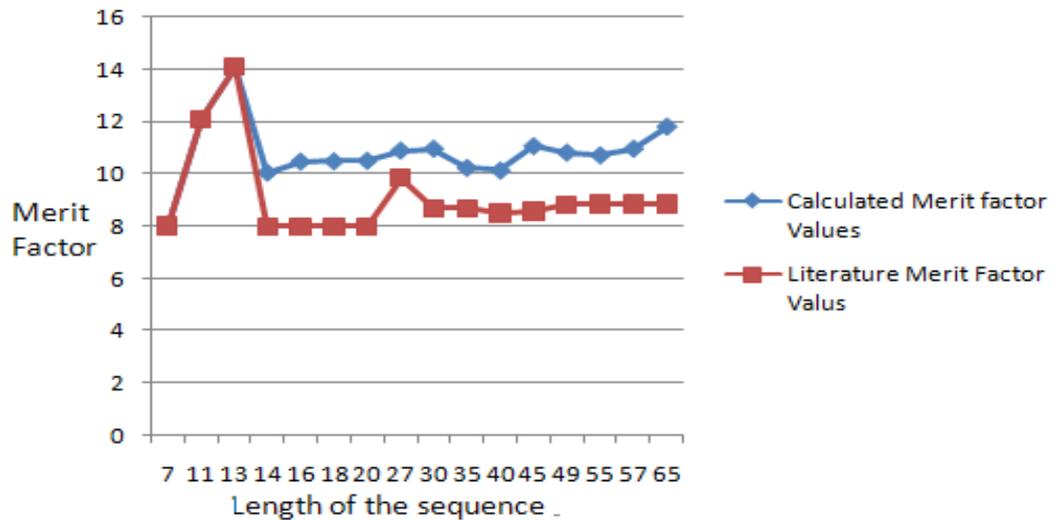
Figure 10: Merit Factor of binary sequences at different lengths

The VLSI architecture for implementing Barker and Nested binary codes has been authored in VHDL and the Xilinx XST, ISE Foundation 12.1i has been used for performing mapping, placing and routing. For Behavioral simulation and Place and route simulation Modelsim 6.3 has been used. The Synthesis tool was configured to optimize for area and high effort considerations. The target device was Spartan-2 (SESP2BRD). The Barker and Nested binary pulse compression sequences implementation reports are presented in   Fig. 5-7. From the device utilization summary same architecture is useful for implementation of higher lengths of binary sequences.

VIII.   Conclusions

In this paper the implementation of FPGA based generation of Barker and Nested binar codes has been described using LFSR's and allows rapid modifications especially for testing of different sequences. This design presents fully digitized approach for generation of Barker and Nested binary codes. The hardware design is divided into two modules: one block for simply generating the codes using LFSR's, D flip flops and one block for implementing the codes in a sequential manner.

The performance of these codes is given in terms of MF values. The performance measures are calculated offline on a host PC in Matlab for the codes generated by VHDL program.

The synthesized binary sequences have good MF values compared with previous work in the literature. The synthesized binary sequences are promising for practical application to radars and communications. It is also proposed that the proposed architecture is giving good MF values for not only Barker sequences but also to binary sequences.

Acknowledgements

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Authors

A.NagaJyothi was born in 1982 at Visakhapatnam. She received her B.Tech (ECE) from Nagarjuna University and M.Tech(Radar & Microwave Engineering) from Andhra University College of Engineering(A). She has a teaching experience of 3 years. Presently she is perusing her Ph.D in the area of Signal Processing in Andhra University, Visakhapatnam.	
K. Raja Rajeswari obtained her B.E., M.E. and Ph.D. degrees from Andhra University, Visakhapatnam, India in 1976, 1978 and 1992 respectively. Presently she is professor in the Department of Electronics and Communication Engineering, Andhra University and Dean for Academics & Research, Andhra University College of Engineering. She has published over 200 papers in various National, International Journals and conferences. She is author of the textbook *Signals and Systems* published by PHI. She is co-author of the textbook *Electronics Devices and Circuits* published by Pearson Education. Her research interests include Radar and Sonar Signal Processing, Wireless Communication Technologies. She has guided fifteen Ph.D.s and presently she is guiding *twenty* students for Doctoral degree. She served as Chairperson IETE Visakhapatnam Centre for two consecutive terms (2006 t0 2010) . Present she is Governing Council Member of IETE, New Delhi. She is zonal coordinate(for south) and Technical Program Committee Chairperson. She is recipient of prestigious IETE Prof SVC Aiya Memorial National Award for the year 2009, Best Researcher Awardee by Andhra University for the year 2004 and recipient Dr. Sarvepalli Radhakrishnan Best Academician Award of the year 2009 by Andhra University. She is Senior Member in IEEE. She is expert member for various national level academic and research committees and reviewer for various national/international journals.	