An Improved Phase Disposition Pulse Width Modulation (PDPWM) For a Modular Multilevel Inverter Used For Photovoltaic Grid Connection

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Abstract: *This modulation method is based on selective virtual loop mapping, to achieve dynamic capacitor voltage balance without the help of an extra compensation signal. The concept of virtual sub module (VSM) is first established, and by changing the loop mapping relationships between the VSMs and the real sub modules, the voltages of the upper/lower arm's capacitors can be well balanced. This method does not requiring sorting voltages from highest to lowest, and just identifies the MIN and MAX capacitor voltage's index which makes it suitable for a modular multilevel converter with a large number of sub modules in one arm. Compared to carrier phase-shifted PWM (CPSPWM), this method is more easily to be realized in field-programmable gate array and is conducive to the control of circulating current. Its feasibility and validity have been verified by simulations.*

Key terms: *Dynamic voltage balance (DVB), modular multilevel converter (MMC), phase disposition pulse width modulation (PDPWM), Photovoltaic (PV),selective virtual loop mapping (SVLM).*

I. Introduction

In recent years, with the development of a large-scale photovoltaic (PV) power plant system, as well as smart grid and multilevel technologies, higher requirements in voltage level, modular structure, and flexibility and reliability of the next-generation large-scale PV grid-connected inverter have been put forward. The features include the following:

1) Power peaking capacity: PV systems should be able to store the electrical energy which is issued by itself as needed during light load conditions; meanwhile, this part of electrical energy would be released again for the load when the load is at the peak. As a result, the peak power of the grid and the reliability of power supply can be improved.

2) Fault ride-through capacity: A large-scale PV system has been required to have the ability to withstand short periods of voltage abnormality, such as the voltage short-term drop caused by short-circuit fault. The PV system should maintain the connection of the inverter and the grid in addition to providing support to the grid.

3) Power quality control: More stable power supply performance could be achieved by introducing suitable inverter control strategy including voltage stability, phase regulation, active filter.

4) Higher redundancy and error correction capacity: The PV system should have the capacity to work efficiently when the failure occurs in some of the modules of the inverter system and should be "smart" enough to correct the situation.

The aforementioned requirements drive the research and development of the next-generation PV inverter, and the topologies of utility PV inverters are moving toward multilevel structure, which could provide better harmonic spectra and reduce the weight of the filtering components. In many of the multilevel structures, a modular multilevel converter (MMC) has attracted many researchers recently. MMC-related application research has mostly concentrated on high-voltage direct current transmission, high-power motor drives, integrated energy storage and medium-voltage STATCOM. The MMC used in the PV grid-connected system is just mentioned in the reasons of this situation are as follows:

1) MMC related research is mostly in theoretical research stage.

2) the characteristic of the photovoltaic power generation is that PV panels are intermittent sources, and their output voltages continuously vary; the dc link's voltage has to be regulated to keep them working in maximum power point tracking (MPPT) status.

3) the dynamic voltage balance has to be considered in multilevel PWM, while the system stability would be damaged by adding improper signals to the reference voltage and the unique circulating current of the MMC will increase the system losses and is not conducive for improving the efficiency of the inverter output and the most important point is that the uncontrolled circulating current threatens the stability of the MMC. Among them, the first two points do not seem to be big problems, because as a new modular converter for medium and high-voltage applications, the MMC has been tested and works well in a back-to-back structure and has much better four-quadrant performance. So, the third and fourth points are the keys to MMC used as a PV inverter.

Many papers have discussed MMC modulation methods. The amplitude modulation has been widely used in the HVDC system; its core idea is to first calculate how many sub modules should be put into action, and the capacitors' sorting voltage and the final working sequence should be determined by the direction of the arm current. The method is simple and practical, but there are frequent sorting issues with the capacitor voltage which would be a burden to the controller if the number of sub modules is large. Phase-shifted pulse width modulation (PSPWM) is a more in-depth method and also studied in the field of MMC modulation. In order to balance the capacitor voltage, an extra signal generated by a PI regulator of each sub module has to be added to both the upper and lower arms' modulation signals. It means that a specialized balance controller has to be designed and with the increase of levels, the difficulty of control will increase and bring the risk of instability. At the same time, some new PWM methods have been proposed with different purposes, for example, the fundamental switching frequency modulation and the improved sub module unified PWM (SUPWM).This paper proposes a new selective virtual loop mapping (SVLM) method based on phase disposition PWM (PDPWM) which has voltage balance capability. The concept of virtual sub module (VSM) is established, and by changing the mapping routines between the VSM and the real sub module (RSM) with SVLM, the capacitor voltages of the upper and lower arms can be balanced even if the inverter loses its symmetry. The method has been designed to consider the following situations:

1) No extra signal should be added to the reference voltage to provide a good basis for the suppression of the circulating current.

2) The possibility of a large number of sub modules in one arm.

3) Retain the equivalent switching frequency of the PDPWM.

4) It could be easily realized in field-programmable gate array (FPGA) for a large-scale converter which has a large number of sub modules. The method is verified through simulations and experiments. The modular multilevel converter (MMC) is an emerging and attractive topology for the high-voltage direct current (HVDC) transmission system. This paper presents a generalized mathematical model for MMC in HVDC applications under balanced and unbalanced grid conditions. The dynamics of the positive-, negative-, and zero-sequence components are derived from the model. Then, a dual current control scheme with positive and negative-equence current controllers is applied to MMC. The power controller to eliminate negative-sequence current components and the other one to eliminate double-line-frequency voltage ripple are compared. Moreover, a zero-sequence current controller is proposed in addition to the positive- and negative-sequence current controllers. Time-domain simulations on a 61-level MMCHVDC test system are performed in the PSCAD/EMTDC software environment. The results demonstrate that the MMC-HVDC system with or without converter transformer is able to operate under unbalanced conditions by the use of the proposed control scheme. [1]This paper makes an attempt to develop grid connected solar photovoltaic array power conversion using modular multilevel converter. The proposed system makes use of single stage power conversion with maximum power point tracking and modular multilevel converter (MMC) as interfacing unit into the grid. Here perturb & observe method of maximum power point algorithm is used to regulate the DC link voltage of the MMC and to synchronize the grid utility voltage with the current for attaining near unity power factor operation under varying environmental conditions. The simulation results presented in this paper verifies the operation of proposed MMC topology such that the AC output is free from the higher order harmonics and grid voltage and current are in phase. The simulation studies are carried out under power system computer aided design PSCAD/EMTDC 4.2 environment. [2]This paper presents the modular multilevel cascade converter (MMCC) family based on cascade connection of multiple reversible-chopper cells or multiple single-phase full bridge cells. This converter family are classified from circuit configuration as follows; single-star bridge-cells (SSBC), single delta bridge-cells (SDBC), double-star chopper-cells (DSCC), and double-star bridge-cells (DSBC). The term MMCC corresponds to a family name in a person while, for example, the term SSBC corresponds to a given name. Therefore, the term "MMCCSSBC" can identify the circuit configuration without any confusion. Among the four circuit configurations, SSBC and DSCC are the most practical than the others in terms of cost and performance, although a distinct difference exists in application between SSBC and DSCC. This paper describes applications of SSBC and DSCC to a battery energy storage system and a motor drive, respectively.[3]The modular multilevel converter (M2C) is a promising converter technology for various high-voltage high power applications. The reason to this is that low-distortion output quantities can be achieved with low average switching frequencies per switch and without output filters. With the M2C the output voltage has such a low harmonic content that high power motors can be operated without any derating. However, the apparent large number of devices, requires more complex converter control techniques than a two-level counterpart. Even though there have been several ways suggested to control the converter itself, it is still a challenge to investigate the interaction of these controllers with an external motor current controller. It is shown in the paper that the anticipated interaction will not result in any problems neither for the converter nor for the motor control itself.[4]This paper describes the operation of modular multilevel converter, an emerging and highly attractive topology for medium- and high-voltage applications. A new pulse width modulation (PWM)

scheme for an arbitrary number of voltage levels is introduced and evaluated. On the basis of this PWM scheme, the semiconductor losses are calculated, and the loss distribution is illustrated.[5]The modular multilevel converter (MMC) is a newly introduced switch-mode converter topology with the potential for high-voltage direct current (HVDC) transmission applications. This paper focuses on the dynamic performance of an MMC-based, back-to-back HVDC system. A phase-disposition (PD) sinusoidal pulse width modulation (SPWM) strategy, including a voltage balancing method, for the operation of an MMC is presented in this paper. Based on the proposed PD-SPWM switching strategy, a mathematical model for the MMC-HVDC system, under both balanced and unbalanced grid operation modes, is developed. Dynamic performance of the MMC-based back-to-back HVDC converter system, based on time-domain simulation studies in the PSCAD/EMTDC environment, is then evaluated. The reported time-domain simulation results show that based on the adopted PD-SPWM switching strategy, the MMC-HVDC station can respond satisfactorily to the system dynamics and control commands under balanced and unbalanced conditions while maintaining voltage balance of the dc capacitors.[6] This paper presents integrated level-shifted and phase-shifted multi carrier modulation schemes that ensures PWM and local capacitor voltage balancing of the Modular Multilevel Converter (M2LC) for medium voltage applications. The integration of either of the modulation schemes with the cell voltage balancing algorithm ensures the floating capacitor voltages are balanced throughout the operation of the M2LC voltage source converter. A comparison of the two schemes is presented based on the harmonic content of the synthesized output waveforms and peak to-peak ripple of the local capacitor voltages. The converter semiconductor losses are also evaluated and compared for these modulation schemes in a typical medium voltage grid application. It is shown that both schemes are competitive in terms of the synthesized output waveform quality. However the phase shifted scheme offers less capacitor voltage ripple while the level shifted scheme offers low converter loss. The concepts are confirmed with both PLECS simulation package and a 10kVA 9-level experimental prototype.[7]The above Phase-shifted pulse width modulation (PSPWM) is a more in-depth method and also studied in the field of MMC modulation. In order to balance the capacitor voltage, an extra signal generated by a PI regulator of each sub module has to be added to both the upper and lower arms' modulation signals. It means that a specialized balance controller has to be designed and with the increase of levels, the difficulty of control will increase and bring the risk of instability. At the same time, some new PWM methods have been proposed with different purposes, for example, the fundamental switching frequency modulation and the improved sub module unified PWM (SUPWM).

II.   Proposed Method

a) Phase Disposition PWM

To overcome the previous disadvantages we proposed a new selective virtual loop mapping (SVLM) method based on phase disposition PWM (PDPWM) which has voltage balance capability. The concept of virtual sub module(VSM) is established, and by changing the mapping routines between the VSM and the real sub module(RSM) with SVLM, the capacitor voltages of the upper and lower arms can be balanced even if the inverter loses its symmetry. The method has been designed to consider the following situations: 1) no extra signal should be added to the reference voltage to provide a good basis for the suppression of the circulating current; 2) the possibility of a large number of sub modules in one arm; 3) retain the equivalent switching frequency of the PDPWM; 4) it could be easily realized in field-programmable gate array (FPGA) for a large-scale converter which has a large number of sub modules. As an important modulation method, carrier disposition (CD) PWM has been widely used in multilevel modulation, and it can be divided into three types: phase disposition (PD), phase opposition disposition (POD), and alternative phase opposition disposition (APOD). For simplicity, this paper will focus on the PDPWM to discuss MMC modulation. PDPWM has been studied for MMC modulation in order to balance capacitor voltages, rotating carrier waves were used, but it seems that they can only work under symmetric condition. For convenience, it is assumed that the number of RSMs of the upper and lower arms is 4 ($N = 4$). And the RSMs are numbered from 1 to 8 (from top to bottom). The difference of the capacitor voltage can be greatly reduced, and the system output voltage and current waveforms are improved. Since no additional signals are added to the reference voltage, the overall characteristics of the MMC do not need to be changed, such as the internal circulating current, which can be observed This characteristic provides a good basis to eliminate the circulating current further. To improve the PDPWM, the concept of VSM can be first established, which means that the VSMs are not the RSMs, and the PWM output gained by the comparison of the modulation signals and the carriers will be transferred to the VSM at first, and VSMs are numbered by 1' to 2N'. The transfer relationships are illustrated as Figs. 3 and 4. According to Figs. 1 and 2, $2N + 1$ level modulation truth table can be shown as in Table I. 1' to 4' are for the upper arm's VSMs, while 5' to 8' represent the lower arm's VSMs. Here, "1" means that the corresponding VSM is ON while "0" means that it is OFF.
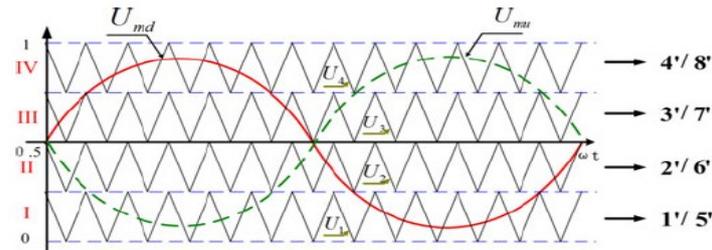
Fig. 1. Transfer relationships of VSM.
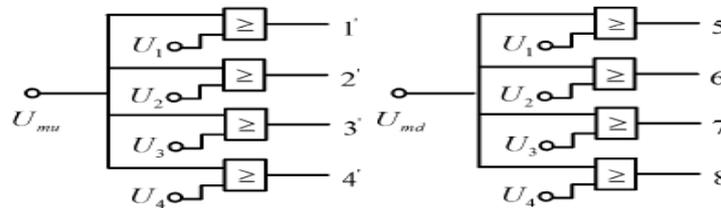
Fig.2. VSM's input.

TABLE I
Switch Combinations Of Vsm ($2n + 1$ Level)

Region	1'	2'	3'	4'	5'	6'	7'	8'	Range of normalized voltage
I	P1	0	0	0	P5	0	0	0	0-0.25
II	1	P2	0	0	1	P6	0	0	0.25-0.5
III	1	1	P3	0	1	1	P7	0	0.5-0.75
IV	1	1	1	P4	1	1	1	P8	0.75-1

P1-P8 is the corresponding PWM signals of each VSM's input

TABLE II
Switch Combinations Of Vsm ($N+ 1$ Level)

Region	1'	2'	3'	4'	5'	6'	7'	8'	Range of normalized voltage
I	P1	0	0	0	P5	1	1	1	0-0.25
II	1	P2	0	0	0	P6	1	1	0.25-0.5
III	1	1	P3	0	0	0	P7	1	0.5-0.75
IV	1	1	1	P4	0	0	0	P8	0.75-1

P5-P8 is the corresponding negative PWM signal of P1-P4 respectively

P1–P4 are the comparison results of the carriers and the modulation signals. The range of normalized voltage corresponds to Regions I–IV. In each region, each VSM has its own PWM signal. For example, when the modulation signal Umu is in Region II, P2 and P6 will be transferred to VSMs 2*'* and 6', while at the same time, "1" will be output to VSMs 1' and 5', and "0" will be output to VSMs 3', 4', 7,*'* and 8'. Other regions can also be analyzed like this. Table II shows the $N + 1$ level modulation, compared with Table I; the driving signals of the lower arm's VSMs are complementary to the upper arm. Because the $2N + 1$ level modulation has higher dc-link voltage ripple, this paper chooses the $N + 1$ level modulation as the PV grid-connected inverter's modulation method. The driving signals of VSMs would be transferred to the RSM by the following mapping rules described in the next section.
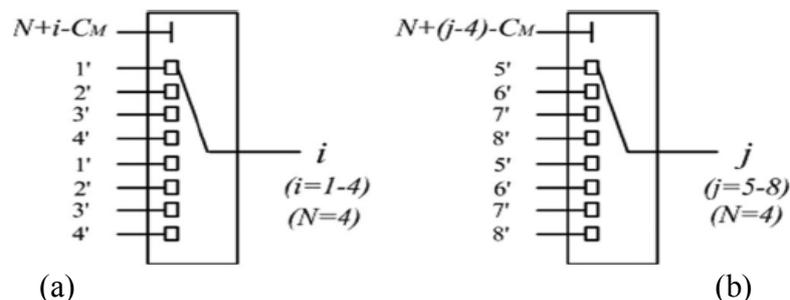
(a)   (b)
Fig. 3. VLM's mapping relationship. (a) Upper arm's mapping. (b) Lower arm's mapping.

III. Capacitor Voltage Virtual Loop Mapping
Balance Control

To solve the sub module capacitor voltage balance control problems, there are two mechanisms: the virtual loop mapping (VLM) method and the enhanced SVLM based on the comparison of capacitor voltage MIN and MAX values. The VLM's principle is using a count-up counter "CM" to control the mapping relationships between the VSMs and the RSMs. The CM 's working frequency can be set equal to the carrier frequency or less, and its counting range is $0 - (N - 1)$. Different counter number means different mappings. The VLM can be realized easily by using multiplexer with single-pass transistor in FPGA like Fig. 4 ($N = 4$); the double input buffer (DIB) structure is also used here. i and j in Fig. 3 are the index numbers of the RSM, respectively, which work with the counter to realize the mapping between the VSMs and the RSMs. For example, if $CM = 0$, $N + i - CM = 4 + i - 0 = 4 + i$, VSMs 1'-2'-3'-4' would be mapped to RSMs 1-2-3-4 as shown in Fig.4(a); likely, if $CM = 1$, $N + i - CM = 4 + i - 1 = 3 + i$, VSMs 4'-1'-2'-3' would be mapped to RSMs 1-2-3-4 [see Fig. 4(b)], and so on. The VLM's final results of both arms are illustrated in Fig. 5.This method can achieve capacitor voltage balance in the case of system symmetry.

IV. Capacitor Voltage Svlm Balance Control

A practical modulation method should not only be effective in a symmetrical system, but also have the ability to regulate dynamically and provide some error finding to correction capabilities to ensure that the system works well under conditions such as error accumulation and device parameter deviation. For the basic cells in the upper bridge, the capacitors are bypassed at on-state and charged at off-state when iPa > 0. For the basic cells in the lower bridge, the capacitors are discharged at on-state and bypassed at off-state when iNa > 0. For the middle cell, the capacitor is discharged at on-state and charged at off-state when $i$oa > 0, where $i$oa is the phase current and is the sum of iPa and iNa. For example, commonly used phase-shift PWM, by changing the modulation signals of the upper and lower arms to get the dynamic balance adjustment capacity of the capacitor voltage, will bring more harmonics to the arm current, change the circulating current' characteristics, and may cause instability. Therefore, changing the modulation signals to achieve the dynamic adjustment capability would be valid only to a certain extent. The new method is mainly through the SVLM to achieve the effect of dynamic regulation ability; here, "selective" means just taking out the capacitor voltage of MIN and MAX values and their corresponding index selectively.
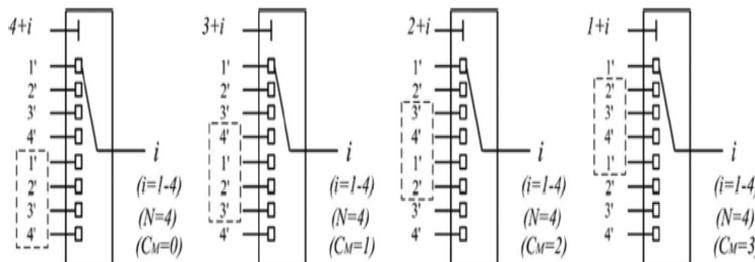
Fig. 4. Upper arm's VLM procedures.
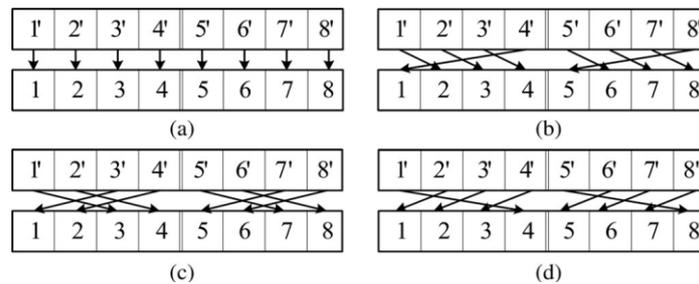
Fig. 5. VLM final results. (a) $CM = 0$. (b) $CM = 1$. (c) $CM = 2$. (d) $CM = 3$.

Before introducing the SVLM rules, note that there are four interesting SMs in Table II, which are 1', 4', 5', and 8'. VSMs 1' and 8' output PWM in regions I and IV, respectively, and output "1" in other regions. Likewise, VSMs 4' and 5' output PWM in regions IV and I, and output "0" in other regions. Table V shows that if some capacitor voltage of the leg is less than the others (means needing more charge and less discharge), it would be right to map the SMs 1' and 8' to this sub module when the corresponding current Ism is positive and mapping the SMs 4' and 5' to it when Ism is negative. To achieve the SVLM, it needs to sort the capacitor voltage as described, but frequent sorting is very time consuming, and requires more hardware resources, which would be a

large burden especially for high-voltage applications needing more sub modules. Other disadvantages of sorting are a reduction in system equivalent frequency and an increase in switching losses. Therefore, the actual method of selective mapping in this paper is just picking the MIN and MAX capacitor voltages and their corresponding index directly and make sure that it can be easily implemented in FPGA. The rules of the SVLM are as follows (just taking the upper arm as an example).

1) First, all of the individual capacitor voltages are compared, and the corresponding RSM indexes of the maximum voltage and minimum voltage are obtained. The MIN index block diagram is shown in Fig. 6(a) (N =4). Y is an array, and $Y(1)$ is the first element. $Udc1 - Udc4$ are the SM's capacitor voltage of the upper arm separately and they are compared to each other at the same time which means that the time is limited. $Y(1)$ would be equal to the capacitor index having the minimum voltage: for example, if the voltage of $Udc3$ is the minimum, $Y(1)$ would be equal to 3. Priority check is just for the case of more than one input of X1−X4 equal to 1, so that X1 could be set up to the highest priority in the MIN check, while X4 has the lowest priority. For the MAX check, "≤" would be replaced by "≥," while $Y(2)$ provides the corresponding index of the maximum capacitor voltage [see Fig. 6(b)], and X4 should have the highest priority while X1 should have the lowest priority.

2) The corresponding truth table of the priority check and index number output function for $Y(1)$ is shown in Table III. $Y(2)$ can be acquired by the same method (see Table IV).

TABLE III
Priority Check And Index Number Output Truth Table Of $Y(1)$

X1	X2	X3	X4	Y(1)
1	x	x	x	1
0	1	x	x	2
0	0	1	x	3
0	0	0	1	4

X means any state.

TABLE IV
Priority Check And Index Number Output Truth Table Of $Y(2)$

X1	X2	X3	X4	Y(2)
x	x	x	1	4
x	x	1	0	3
x	1	0	0	2
1	0	0	0	1

X means any state.

3) The other SMs' indexes except the minimum and maximum capacitor voltages would also be assigned to the Y array by sequence after $Y(2)$.The main difference between them is that the proposed new MMC employs a middle cell in each phase, which can reduce the number of basic cells while producing the same number of voltage levels. Of course, it also has some drawbacks due to the employment of middle cell, such as that the voltage balancing becomes more complex and the redundancy of middle cell is hard to realize. For example, if SM 3 has the lowest voltage and SM 2 has the highest voltage, the Y array would be assigned like this, as shown in Fig. 7. 4) Change the mapping route as shown in Fig. 8,$N[Y(i)]$ is the multiport switch selector array, whose index is $Y(i)$ (I= 1−4). $FlagI$ is the symbol of the arm's current direction. If the upper arm's current is positive ($Ijp > 0$), $FlagI = 0$; $N[Y(1)]$ would be equal to 3, which means that VSM 1'would be mapped to RSM 3. At the same time, $N[Y(2)]$ would be equal to 4, andVSM4' would be mapped to RSM 2. In contrast, if $Ijp < 0$, $Flag\,I$ = 1, $N[Y(1)]$ is assigned to 2, and VSM 4' is mapped to RSM 3, while VSM 1' is mapped to RSM 2.The rest of the mappings follow the aforementioned VLM, as can be seen in Fig. 8. Just take Fig. 7 as an example.
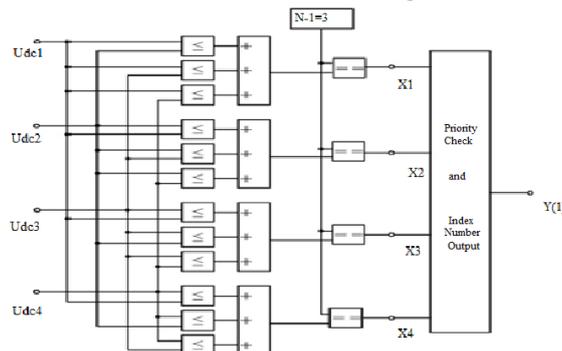
Fig. 6 (a) Index acquirement method of the MIN voltages block diagram.
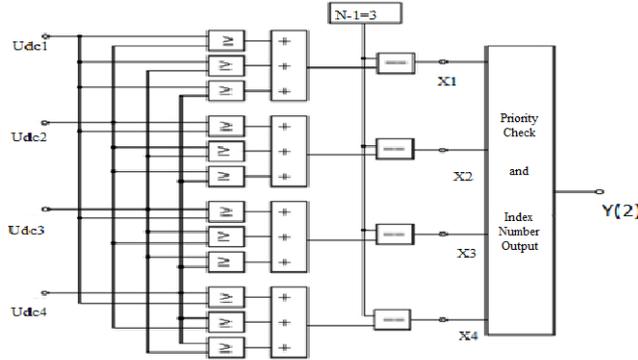
Fig.6 (b).Index acquirement method of the MAX voltages block diagram.

If $Ijp > 0$
$N[Y(1)] = N[3] = 3$
$N[Y(2)] = N[2] = 4.$
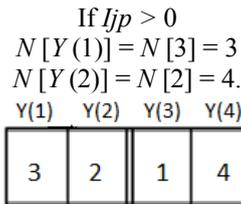
Fig. 7. Assignment of the Y array.
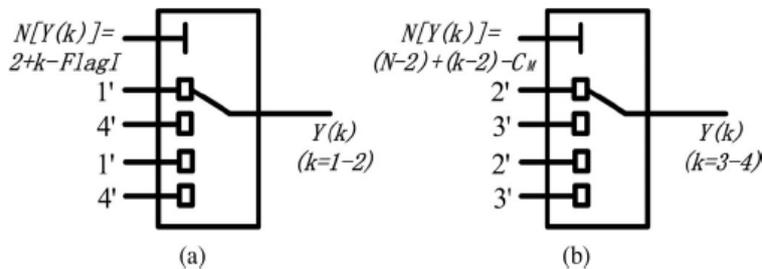
Fig. 8. Mapping route control of each RSM.
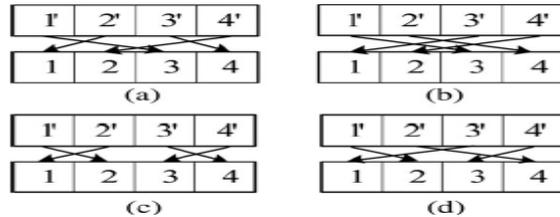
Fig. 9. SVLM. (a) $CM = 0$. (b) $CM = 1$.
(c) $CM = 0$. (d) $CM = 1$.

If $Ijp < 0$
$N[Y(1)] = N[3] = 2$
$N[Y(2)] = N[2] = 3$

At the same time, the rest of the RSMs would still follow the previously described VLM rule. But the maximum counter range of CM would be set equal to $N - 2$.

If $CM = 0$
$N[Y(3)] = N[1] = 3$
$N[Y(4)] = N[4] = 4.$

If $CM = 1$
$N[Y(3)] = N[1] = 2$
$N[Y(4)] = N[4] = 3.$

5) The final mapping route would be as follows:
$Ijp>0(j = a, b, c)$, SVLM is given in Fig. 9 (a) and (b).$Ijp<0(j = a$, b, c), SVLM is given in Fig. 9 (c) and (d). 6) In order to minimize the delay of the PWM signal, a synchronous sampling control should be adopted to

the SVLM .*U*mu is the reference voltage, and *Y* array is sampled at the intersection point of two triangular carriers.

V.   Operating Principle Of Phase Disposition Pwm Method

a**). Modulation Principles**

Fig. 10 shows the single-phase equivalent circuit of the MMC, which has two arms including the upper arm and the lower arm, with each arm having *N* sub modules (SM), one buffer inductor *L*, and equivalent resistor *R*. The dc link of the MMC is floated or connected to high-voltage sources depending on the working purpose of the converter. The output of the converter is the connection point of the upper and lower arms. *Ls* is the ac-link inductor, and *Z0* is the equivalent impedance of the ac side. The working states of SM are shown in TableV. Each SM has two states ("ON" and "OFF"), and the corresponding output voltage (*U*sm) of the SM is *Vc* or 0. The capacitor will charge or discharge during the period of the "ON" state of the SM depending on the direction of *I*sm. For example, if *I*sm > 0, the capacitor would be charged, and if *I*sm < 0, the capacitor would be discharged.
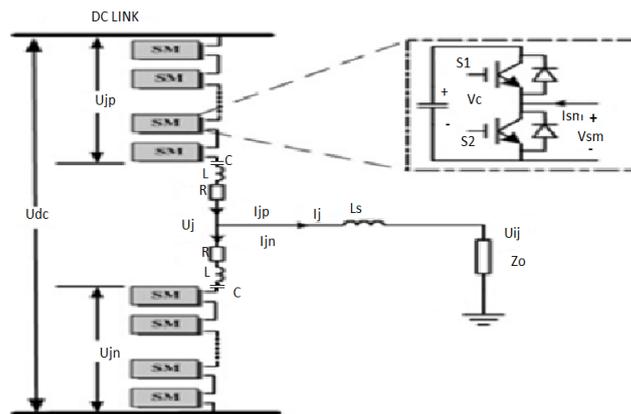
Fig.10. Single phase equivalent circuit of multilevel inverter

To see how the system works, a simplified single phase topology is shown in Fig. 10.1. The output voltage v1 of this leg of the bottom inverter (with respect to the ground) is either +vdc/2 (*S5* closed) or −dc/2 (*S6* closed). This leg is connected in series with a full H-bridge, which, in turn, is supplied by a capacitor voltage. If the capacitor is kept charged to vdc/2, then the output voltage of the H-bridge can take on the values +*V*dc/2 (*S1* and *S4* closed), 0 (*S1* and *S2* closed or *S3* and *S4* closed), or −*V*dc/2 (*S2* and *S3* closed). An example output waveform from this topology is shown in Fig. 3(a).When the output voltage *v* = *v1* + *v2* is required to be zero, one can either set *v1* = +*V*dc/2 and *v2* = −*V*dc/2 or *v1* = −*V*dc/2 and *v2* = +*V*dc/2.Additional capacitor's voltage regulation control detail is shown in Fig. 3. To explain how the capacitor is kept charged,consider the interval $\theta 1 \leq \theta \leq \pi$, the output voltage in Fig. 3(a)is zero, and the current *i* > 0. If *S1* and *S4* are closed (so that *v2* = +*V*dc/2) and *S6* is closed (so that *v1* = −*V*dc/2), then the capacitor is discharging [*ic* = −*i* < 0; see Fig. 3(b)], and *v* = *v1* + *v2* = 0. On the other hand, if *S2* and *S3* are closed (so that *v2* = −*V*dc/2) and *S5* is also closed (so that *v1* = +*V*dc/2), then the capacitor is charging [*ic* = *i* > 0; and v = *v1* + *v2* = 0. The case *i* < 0 is accomplished by simply reversing the switch positions of the *i* > 0 case for charging and discharging of the capacitor. Consequently, the method consists of monitoring the output current and the capacitor voltage, so that during periods of zero voltage output, either the switches *S1*, *S4*, and *S6* are closed or the switches *S2*, *S3*, and *S5* are closed, depending on whether it is necessary to charge or discharge the capacitor. It is this flexibility in choosing how to make that output voltage zero that is exploited to regulate the capacitor voltage. The goal of using fundamental frequency switching modulation control is to output a five-level voltage waveform, with a sinusoidal load current waveform, as shown in Fig. 3(a). If the capacitor's voltage is higher than Vdc/2,switches *S5* and *S6* are controlled to output voltage waveform *v1*, and the switches *S1*, *S2*, *S3*, and *S4* are controlled to output voltage waveform *v2*, shown in Fig. 3(b). The highlighted part of the waveform in Fig. 3(b) is the capacitor discharging period, during which the inverter's output voltage is 0 V. If the capacitor's voltage is lower than *V*dc/2, the switches *S5* and *S6* are controlled to output voltage waveform *v1*, and switches *S1*, *S2*, *S3*, and *S4* are controlled to output voltage waveform *v2*, shown in Fig. 3(c). The highlighted part of the waveform in Fig. 3(c) is the capacitor charging period, when the inverter's output voltage is 0 V. Therefore, the capacitors' voltage can be regulated by alternating the capacitor's charging and discharging control, when the inverter output is 0 V. This method of regulating the capacitor voltage depends on the voltage and current not being in phase. That is, one needs positive (or negative) current when the voltage is passing through zero in order to

charge or discharge the capacitor. Consequently, the amount of capacitor voltage the scheme can regulate depends on the phase angle difference of output voltage and current. In other words, the highest output ac voltage of the inverter depends on the displacement power factor of the load.
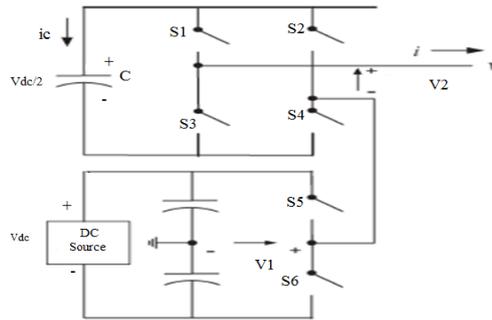
Fig.10.1.Circuit diagram of single phase multilevel inverter with capacitor
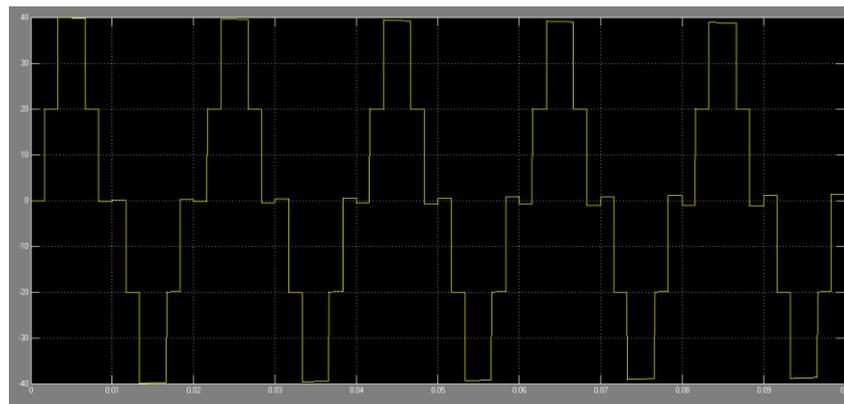
Fig. 11. single phase multilevel inverter with capacitor output voltage
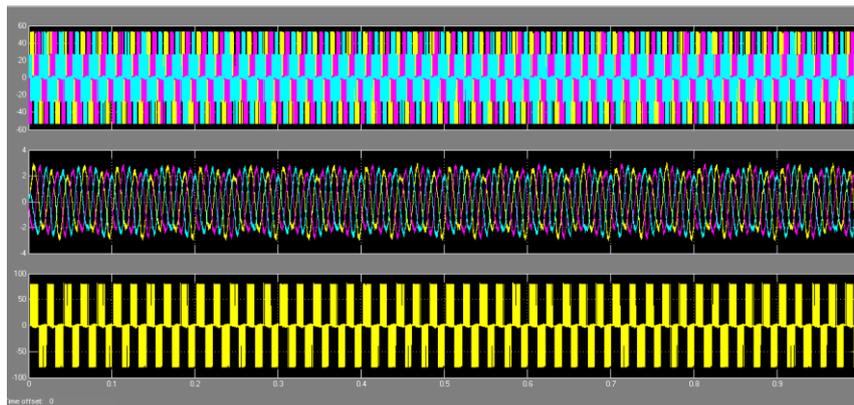
Fig. 12. Grid voltage, output voltage, and output current inverter

TABLE V
Half-Bridge Sub module Working States

MODE	S1	S2	Usm	Ism	STATE	CAPACITOR
1	1	0	Vc	>0	On	Charging
2	1	0	Vc	<0	On	Discharging
3	0	1	0	>0	Off	Unchanged
4	0	1	0	<0	Off	Unchanged

The capacitor voltage will be kept while the SM is "OFF." Seen from Fig. 1, the *j* phase output voltage *Uj* can be expressed as (*j = a b, c*)

Uj=1/2[Ujn+L (dIjn/dt)+IjnR]-1/2[Ujp+L(dIjp/dt)+IjpR]... (1)

where U_{jp} represents the sum of the upper arm's capacitor voltage while U_{jn} represents the sum of the lower arm's capacitor voltage. I_{jp} and I_{jn} are the upper arm's current and the lower arm's current, respectively. L and R are the buffer inductor and resistor of the arm.

$$2U_j = (U_{jn}-U_{jp})+L\, d(I_{jn}-I_{jp})/dt + R(I_{jn}-I_{jp}) \dots\dots\dots (2)$$

$$I_j=I_{ip}-I_{jn} \dots\dots\dots (3)$$

$$I_{circ\,j} = I_{jp} + I_{jn}/2 \dots\dots\dots (4)$$

$$2U_j = (U_{jn} - U_{jp}) - L\,dI_j dt - RI_j \dots\dots\dots (5)$$

$$U_{dc}=(U_{jn} + L\,dI_{jn}dt + RI_{jn}+U_{jp} + L\,dI_{jp}dt + RI_{jp})$$
$$=(U_{jn} + U_{jp}) + L\,d(I_{jn} + I_{jp})dt + R(I_{jn} + I_{jp})$$
$$=(U_{jn}+U_{jp})+2L(dI_{circj}/dt)+2RI_{circj} \dots\dots\dots (6)$$

$$L(dI_{circj}dt)+RI_{circj}=1/2(U_{dc}-U_{jp}-U_{jn}) \dots\dots\dots (7)$$

Defining two variables e and U_{circj} as the following equations:

$$e =1/2(U_{jn} - U_{jp}) \dots\dots\dots (8)$$

$$U_{circ\,j} = L(dI_{circj}/dt)+ RI_{circj}$$
$$=1/2(U_{dc} - U_{jp} - U_{jn}) \dots\dots\dots (9)$$

From (8) and (9), the reference signals of upper and lower arms can be expressed by

$$U_{jp}=1/2(U_{dc}-e-U_{cirj}) \ \&$$
$$U_{jn}=1/2(U_{dc} +e-U_{cirj}) \dots\dots\dots (10)$$

where U_{circj} can be used to suppress the circulating current.

b) Basic Structure and Control

There are two structures which can be used in medium- and high-voltage PV grid-connected inverters with MMC: single stage and two-stage structures. The series-connected PV modules of a single-stage structure access the dc link directly, while in a two-stage structure the procedure is different: PV panels could be connected to the dc link by cascaded dc/dc circuits [24], [25]. The differences are that voltage ripples of the single stage structure are bigger than those of the two-stage structure, and the two-stage structure has more complex control [26]. Fig. 11 shows the control block diagram of a modular multilevel PV inverter where U_{dcref} is the reference of the dc-link voltage and U_{dc} is the real dc-link voltage; they are compared with each other to produce the active reference current i_{dref} after the PI controller i_{qref} is the reactive reference current. U_s (a, b, c) is the ac-side grid voltage and I (a, b, c) is the output current of the MMC. S_j (1, . .,2N, j = a, b, c) are the PWM signals of the MMC. It can be seen that the reference voltage can be acquired by decoupled control, and the circulating current suppression compensation signal should be added to it. Meanwhile, it is no longer possible to balance the system capacitor voltage dynamically by generating the appropriate balance compensation signal, but solely by the adjustment of the PWM method. This approach has the advantage of not only avoiding excessive compensation signal mutual interference (which increases system stability), but also provides a good basis for circulating current suppression and promotes high dc voltage utilization ratio.
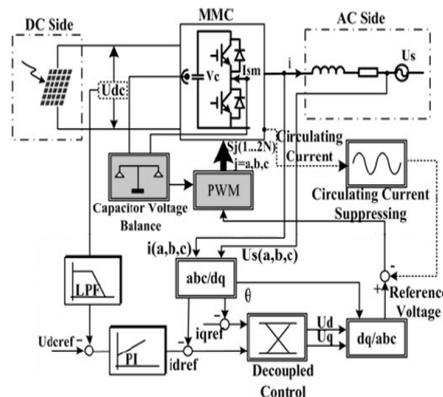
Fig.13. Modular multilevel PV inverter overall control block diagram.

TABLE VI
Simulation And Experiment Parameters

PARAMETERS	VALUES
No of PV panels	4
No of sub-modules in each arm	4
Sub-module Capacitor C	2200 uF
Arm Inductor L	2 mH
Arm Equivalent Resistance	0.1 Ω
AC Link Inductor Ls	5 mH
Carrier frequency	2400 Hz
AC system voltage Us (rms)	115 V
Power frequency	60 Hz
Transformer	600 V/ 240 V

VI.   Challenges In Proposed Converter

The capacitor voltages of the upper and lower arms can be balanced even if the inverter loses its symmetry. The method has been designed to consider the following situations: 1) no extra signal should be added to the reference voltage to provide a good basis for the suppression of the circulating current; 2) the possibility of a large number of sub modules in one arm; 3) retain the equivalent switching frequency of the PDPWM; 4) it could be easily realized in field-programmable gate array (FPGA) for a large-scale converter which has a large number of sub modules.

VII.   Conclusion

This paper first discussed the possibilities of the MMC being used as an interface between the grid and PV panels, and proposed an improved SVLM method based on the PDPWM. This method can produce $2N+1$ and $N+1$ level outputs in the MMC, and achieve sub module capacitor voltage dynamic balance compensation control while not changing the reference signal. The whole mapping rules are presented and it is easy to be implemented in FPGA and the effectiveness of the method was proved well.

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