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Multi-level Inverters and Its Application of Statcom Using Svpwm and Spwm Techniques

[1]D. V. N.Ananth, [2]Y. Naveen Kumar, [3]B. B. G. Tilak, [4]P. Sai Raghunath
[1,2]Assistant Professor, Department of EEE, VITAM College of Engineering, Vishakhapatnam-531173
[3]PG Student, VITAM College of Engineering, Vishakhapatnam-531173
[4]PG Student, National Institute of Technology (NIT), Calicut-673601

Abstract: *Power quality in distribution system has been the major issue now-a-days. Utility distribution networks, sensitive industrial loads and critical commercial operations suffer from various types of power quality problems like voltage sag, service interruptions total harmonic distortion (THD) etc. A voltage dip is a short time (10 ms to 1 minute) event during which a reduction in r.m.s voltage magnitude occurs.. Multi-level inverters are the best form to solve these problems. The general structure of multilevel inverter is to synthesize sinusoidal voltage waveform from several levels of voltages typically obtained from capacitor voltage source. In this paper both the Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Pulse Width Modulation (SVPWM) techniques are employed for the 3-level multi inverter and both these techniques are compared along with the application of STATCOM. All the results are studied through MATLAB Simulink by designing a 10KV, 400V, 50Hz system by applying 3-Φ to ground fault using RL load.*

Keywords: *Multi-level inverter, SPWM technique, SVPWM technique, STATCOM, Total Harmonic Distortion (THD).*

I. Introduction

Recent advances in power electronics have made the multilevel concept practical. In fact, the concept is so advantageous that several major drives manufacturers have obtained recent patents on multilevel power converters and associated switching techniques. It is evident that the multilevel concept will be a prominent choice for power electronic systems in future years, especially for medium voltage operation. They are normally connected in series to form stacks of level. The number of levels in an inverter bridge defines the number of direct current (DC) voltage steps that are required by the inverter bridge in order to achieve a certain voltage level at its output. Because power semiconductor switches have limited voltage capability, the total DC bus voltage of an inverter bridge is divided into a number of voltage steps, such that each voltage step can be handled by one power switch.

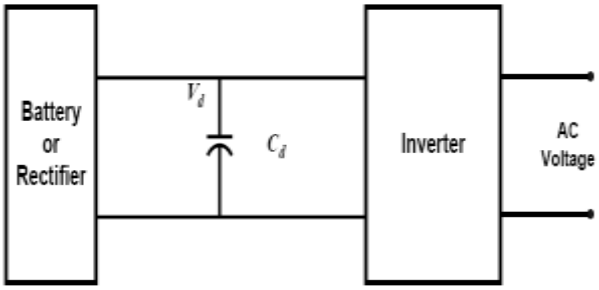

Fig (1): Schematic diagram for Inverter System

In most of the applications inverter is used to control the fundamental voltage magnitude and the frequency of the ac output voltage. AC loads may require constant or adjustable voltage at their input terminals, when such loads are fed by inverters, it is essential that the output voltage of the inverters is so controlled as to fulfill the requirement of the loads. For example if the inverter supplies power to a magnetic circuit, such as a induction motor, the voltage to frequency ratio at the inverter output terminals must be kept constant. This avoids saturation in the magnetic circuit of the device fed by the inverter. Multilevel inverters are increasingly being used in high-power medium voltage applications due to their superior performance compared to two-level inverters. If more than two voltage levels were available to the inverter output terminals, the AC output could better approximate a sine wave. Low ratio of carrier frequency to modulation frequency is the best form of modulation for high power application, which is operating domain for multilevel inverters. For this reason multilevel inverters offer superior performance.

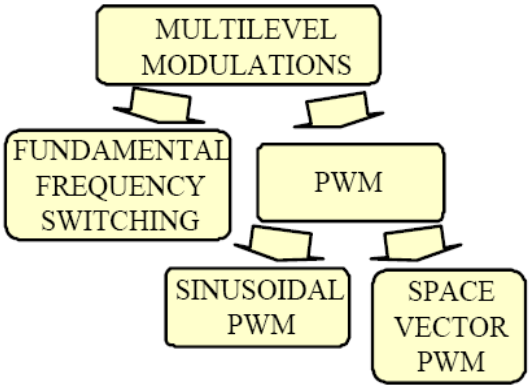

Fig (2): Different types of modulation techniques

Fig (2) shows the different types of modulations that can be employed for multi-level inverters. The sinusoidal pulse width modulation (SPWM) is one of the most popular modulation technique used in wide range of industrial application where power switching converters are employed. SPWM technique is based on classical SPWM technique with carriers and reference sine waveform. Space Vector PWM (SVPWM) refers to a special switching sequence of the upper three power IGBT of a three-phase inverter. Space-vector modulation offers a greater number of fixed voltage vectors to be used in approximating the modulation signal, and therefore allows more effective space vector PWM strategies to be accomplished. The major reason for using multi-level inverters with PWM techniques is to improve the power quality and to reduce the harmonic content present in the power system networks. In general the total harmonics distortion (THD) is mathematically given by

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} H_{(n)}^{\,2}}}{H_1}$$

Let H(n)= hn , then

$$h_n = \frac{4E}{n\pi} \sum_{k=1}^{S} \cos(n\alpha_k)$$

In addition to this application, if we use static shunt devices to the network then the performance of the network will increase. One of such device which is used in most of the applications is a static compensator (STATCOM). Fig (3) shows the schematic diagram of STATCOM.

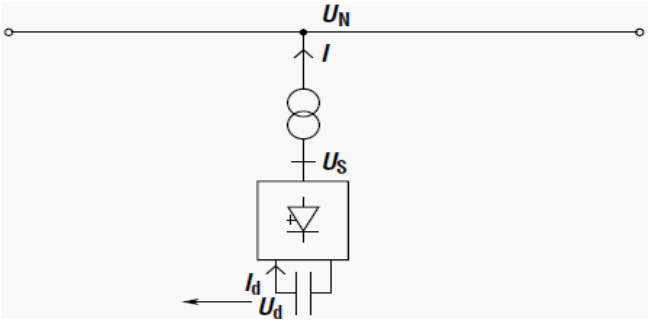

Fig (3): Schematic diagram of STATCOM

STATCOM injects reactive component into the network thereby provides the reactive power to the system under abnormal conditions and can withstand for a few minutes for the system to reach its normal state thereby improving the stability.

II. Design of multi-level inverter

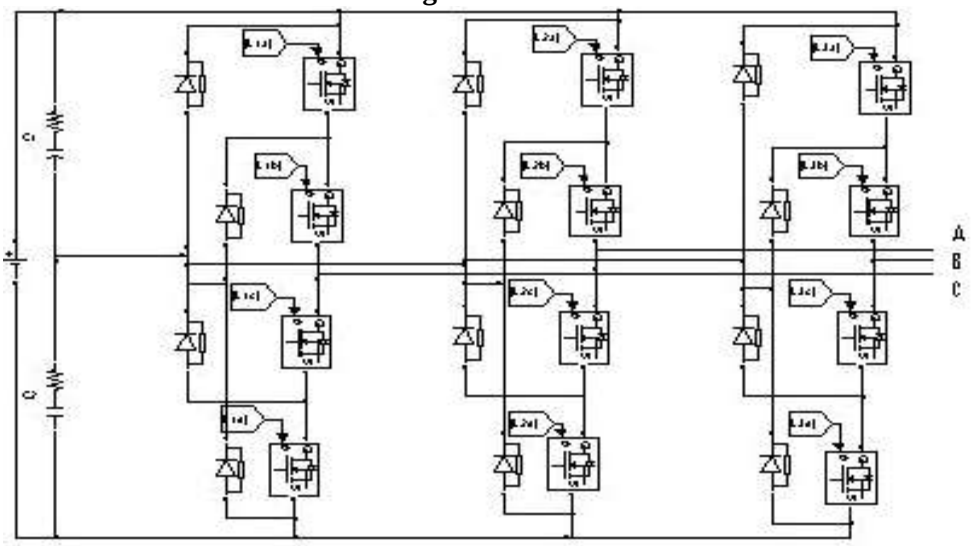

Fig (4): 3-level multi-inverter circuit topology

Three-level pulse-width modulation (PWM) voltage-source inverters (VSI) are the choice for many high-power applications such as medium-voltage motor drives both in industrial and other applications. Fig(4) shows the most popular type of three-level inverters, the three-phase diode clamped voltage source inverter. Compared with conventional two-level inverters, a three-level inverter has several favorable features of blocking the dc link voltage to half thus reduce the voltage stress on switching devices to half, lower common mode voltage steps, low output voltage harmonic and current ripple for the same switching frequency in addition to the capability of handling higher voltages.

As shown in fig (4) each leg in three-level inverter is constituted by four controllable switches with clamping diodes. Two equal capacitors splits the DC bus voltage into three voltage levels +E/2, 0, -E/2 thus the name 3-level. Clamping diodes blocks the reverse voltage of the capacitor and provide connection to the neutral point. The three states available with a single leg are shown in Table-1. The complementary switch pairs are (SP1, $SP1^{l}$) and (SP2, $SP2^{l}$) where P is the phase indicator (P = a, b, c). Vi is the voltage between phase and fictive mid-point of the dc link.

Table (1): Inverter switching states

State	SP1	SP2	$SP1^{l}$	$SP2^{l}$	V_i
1	ON	ON	OFF	OFF	V/2
0	OFF	ON	ON	OFF	0
-1	OFF	OFF	ON	ON	-V/2

2.1. SVPWM technique

The principle of A three phase inverter is, the right must be controlled so that at no time are both switches in the same leg turned on or else the DC supply would be shorted. This requirement may be met by the complementary operation of the switches within a leg. i.e. if SP1 is on then SP1l is off and vice versa. Several works apply the SVPWM to the three level inverter. These works use a typical SVPWM method, which approximate the output voltage by using the nearest three output vectors. When the reference vector changes from one region to another, it may induce an output vector abrupt change. In addition we need to calculate the switching sequences and switching time of the states at every change of the reference voltage location. Thus the computational complexity is greatly increasing with the increasing number of the reference vectors, and it is a main limitation of the application of this typical SVPWM.

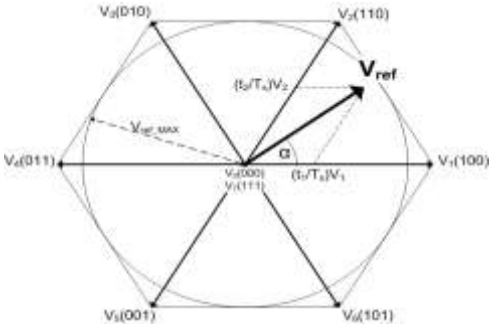

Fig (5): All eight possible switching vectors for a three-leg inverter using space vector modulation.

For industrial applications, variation in the output voltage of inverter is often required. This is mainly for

(1) Overcoming the variation in dc input voltage.
(2) Maintaining the v/f ratio of induction motor constant.
(3) Compensating for regulation of inverters.

In SVPWM there are totally 24 minor sectors in the plane. And the vertices of these sectors represent the voltage vectors. Each small voltage vector and zero voltage vectors have 2 and 3 redundant switching states, respectively. In three-phase three-level inverter, when the rotating voltage vectors falls into one certain sector, adjacent voltage vectors are selected to synthesize the desired rotating voltage vector based on the vector synthesis principle, resulting in three-phase PWM waveforms. Fig (5) shows the switching vectors of 3-level inverter in hexagon. Generally the three phase voltages are obtained from AC machines. The three phase voltages obtained are

$$V_a = V_m \text{Sin}\omega t \quad \ldots\ldots\ldots(1)$$
$$V_b = V_m \text{Sin}(\omega t - 2\pi/3) \quad \ldots\ldots\ldots(2)$$
$$V_c = V_m \text{Sin}(\omega t - 4\pi/3) \quad \ldots\ldots\ldots(3)$$

Space vector modulation (SVM) is based on vector selection in the q-d stationary reference frame. The first step in the SVM scheme is to identify the three nearest vectors. The magnitude and angle of the rotating vector can be found by means of Clark's Transformation. To implement the space vector PWM, the voltage equations in the a-b-c reference frame can be transformed into the stationary d-q reference frame that consists of the horizontal (d) and vertical (q) axes.

The SVPWM scheme is used for the PWM signal generation, based on the sampled amplitudes of reference phase voltages. The line voltage, line current & THD of Line Voltage and Line Current waveforms for inverter operation are presented for three level inverter simulation circuit model for SVPWM generator circuit is shown in fig (6).

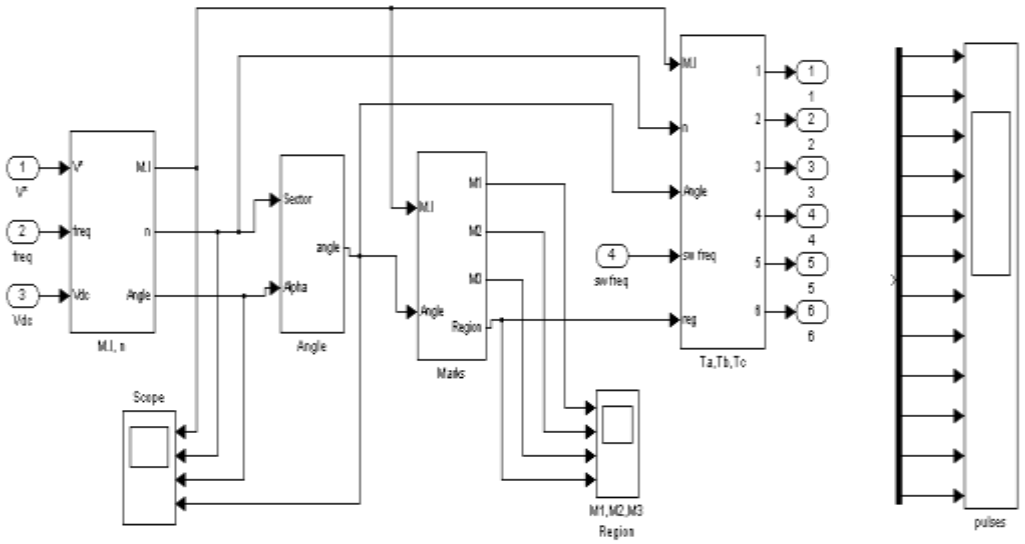

Fig (6): Gate pulse generation circuit of SVPWM for 3-level multi-inverter

2.2. SPWM technique

Operation of a multilevel inverter at low switching frequency is the Sinusoidal natural PWM and alternately sinusoidal PWM technique is operation at high switching frequency. This paper provides analytical methods for the study, performance evaluation, and design of the modern carrier- based PWM methods which are widely employed in PWM multilevel voltage-source inverter drives due to the low-harmonic distortion waveform.

The two main advantages of PWM inverters in comparison to other inverters are (i) control over output voltage magnitude (ii) reduction in magnitudes of redundant harmonic voltages. Good quality output voltage in SPWM requires the modulation index (m) to be less than or equal to one. For m>1 (over-modulation), the fundamental voltage magnitude increases but at the cost of decreased quality of output waveform. The maximum fundamental voltage that the SPWM inverter output (without resorting to over-modulation) is only 78.5% of the fundamental voltage of other techniques. In SPWM technique carrier based modulation strategies are used which are derived from disposition techniques developed by Carrara et al, where for an M level inverter, M-1 carriers of identical frequency and amplitude are arranged to occupy contiguous bands between +VDC and -VDC. These carriers can be arranged in:

(1) Alternative Phase Opposition Disposition (APOD), where each carrier is phase shifted by 180^0 from its adjacent carriers.
(2) Phase Opposition Disposition (POD) where the carriers above the reference zero point is out of phase with those below the zero point by 180^0.
(3) Phase Disposition (PD) where all carriers are in phase.

In this paper we are using Phase Disposition strategy for SPWM, which all the carriers are in phase. The SPWM generator circuit is shown in fig(7).

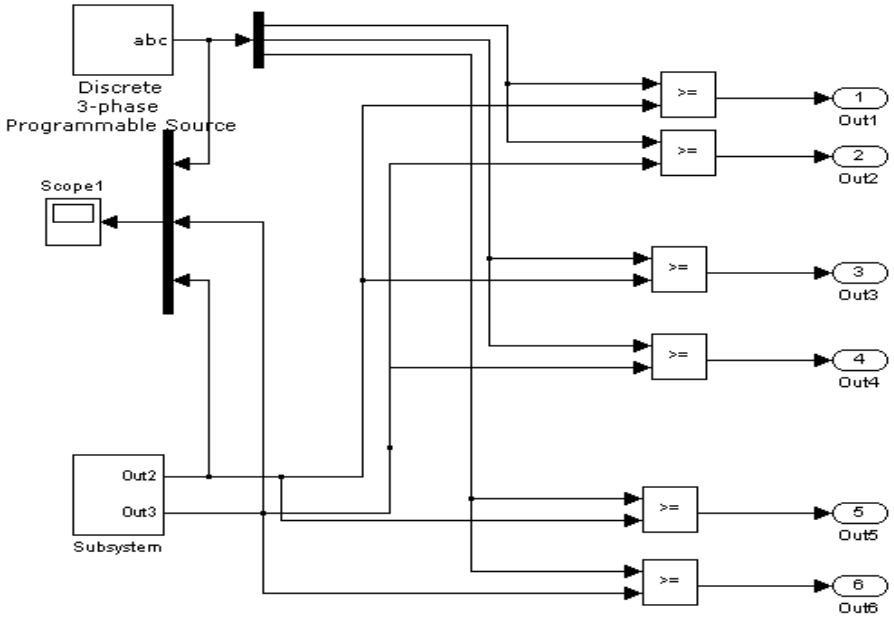

Fig (7): Gate pulse circuit of SPWM for 3-level inverter

SPWM technology corrects the output voltage according to the value of the load by changing the Width of the switching frequency in the oscillator section. As a result of this, the AC voltage from the Inverter changes depending on the width of the switching pulse. To achieve this effect, the SPWM Inverter has a SPWM controller IC which takes a part of output through a feedback loop. The PWM controller in the Inverter will makes corrections in the pulse width of the switching pulse based on the feedback voltage. This will cancel the changes in the output voltage and the Inverter will give a steady output voltage irrespective of the load characteristics.

III. MATLAB Simulation

The topology using for construction of multi-level inverter using SVPWM and SPWM is same. In this paper comparison is drawn between SVPWM and SPWM on the basis of THD of the output voltage and current waveforms. The simulation circuits of SVPWM and SPWM are shown fig (8) and fig (9) respectively.

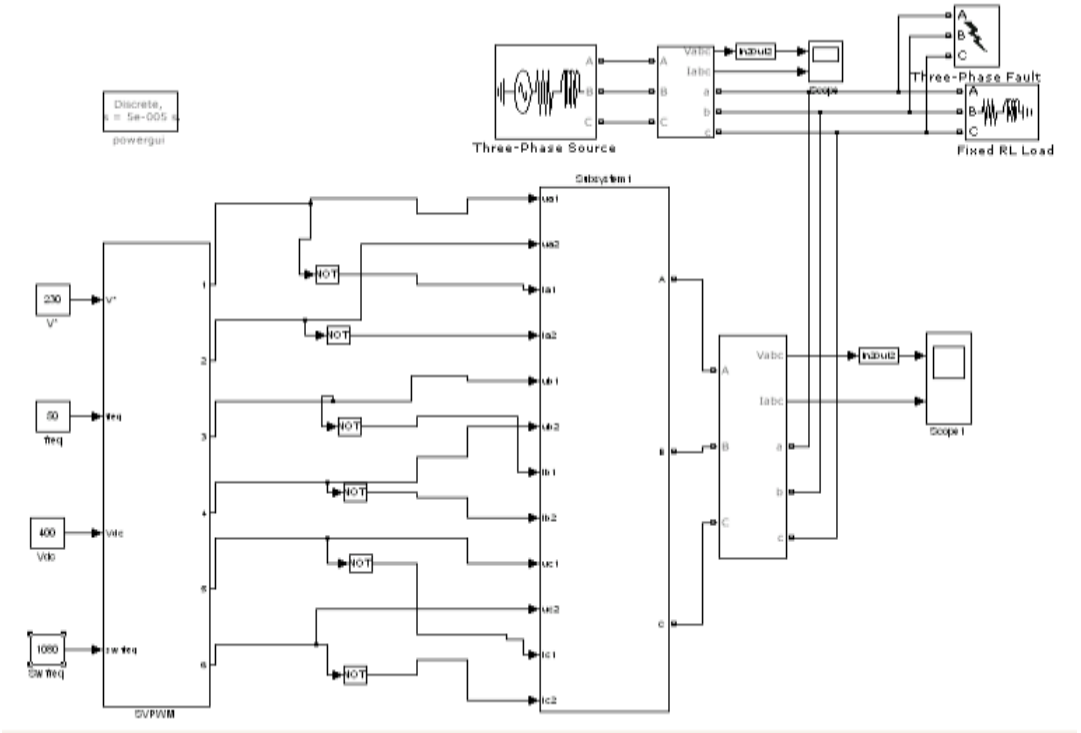

Fig (8): Simulation circuit of 3-level inverter for SVPWM circuit

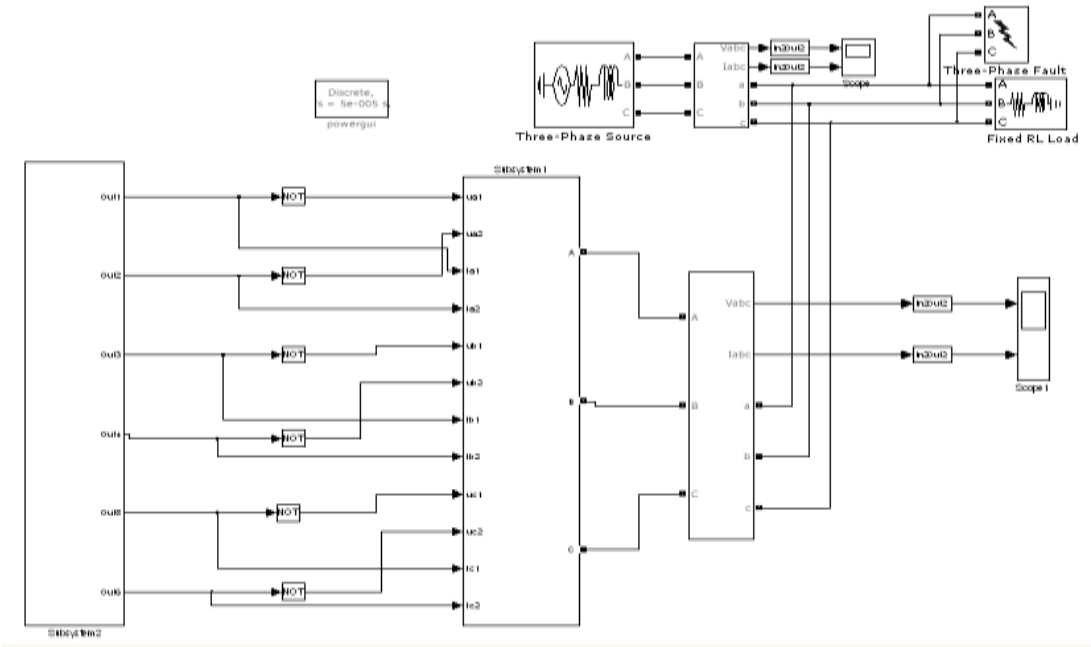

Fig (9): SPWM simulation circuit for 3-level multi-inverter

IV. Results

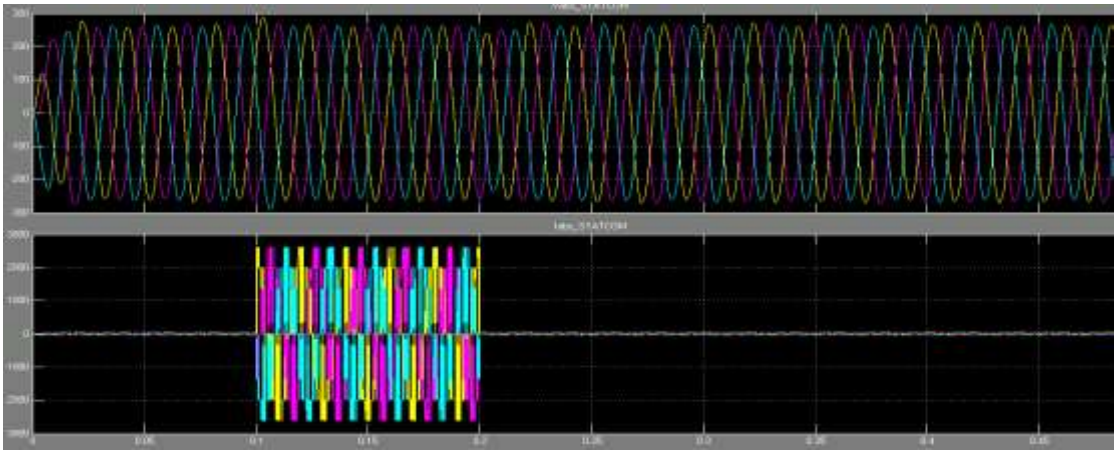

Fig (10a): Voltage & current waveforms across STATCOM for SVPWM

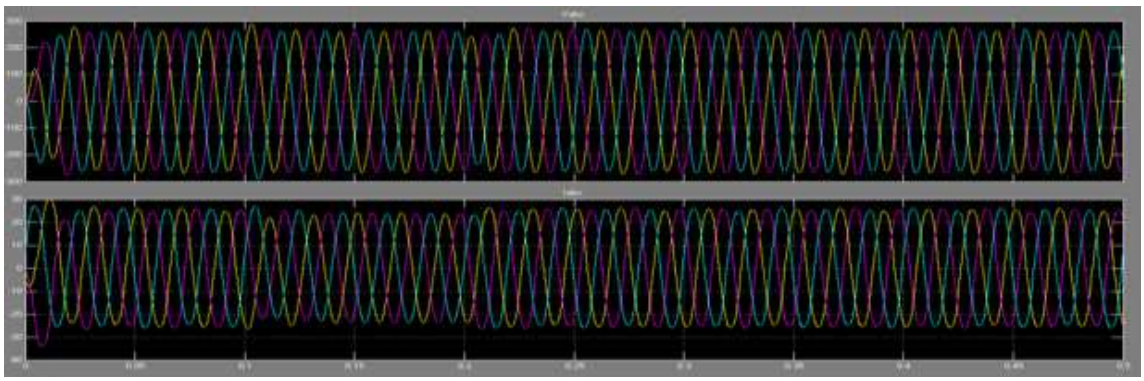

Fig (10b): Output voltage & current waveforms of 3-level SVPWM multi-inverter

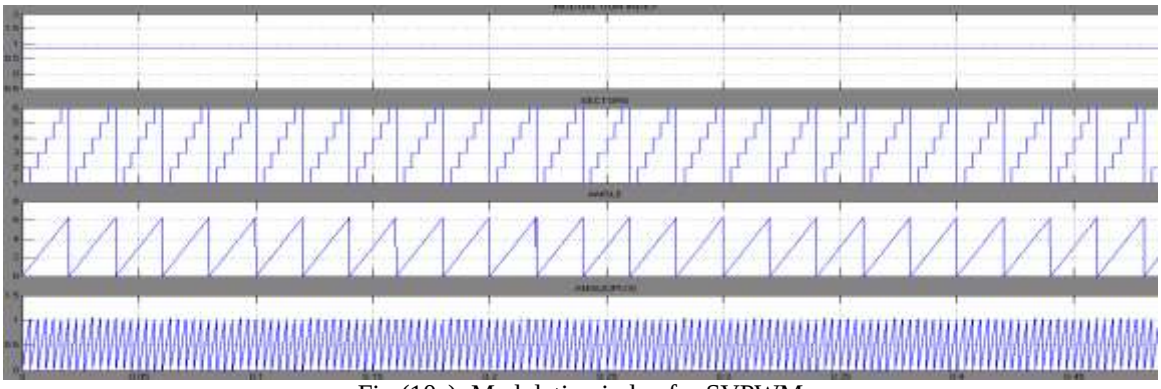

Fig (10c): Modulation index for SVPWM

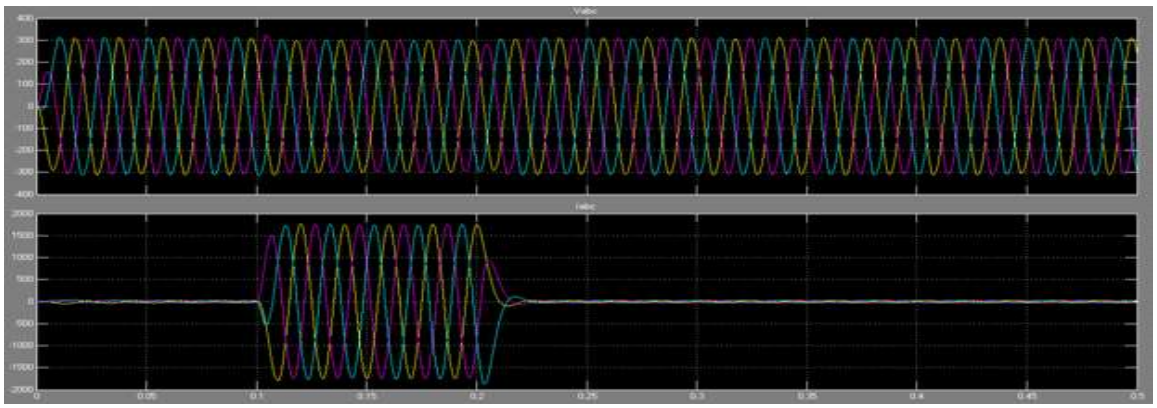

Fig (11a): Voltage & current waveforms across STATCOM for SPWM

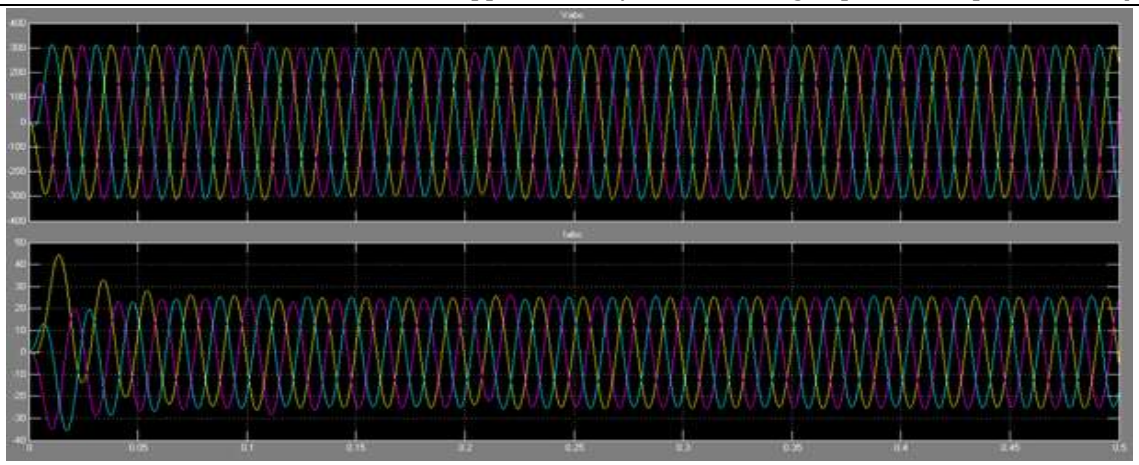

Fig (11b): Output voltage & current waveforms of 3-level SPWM multi-inverter

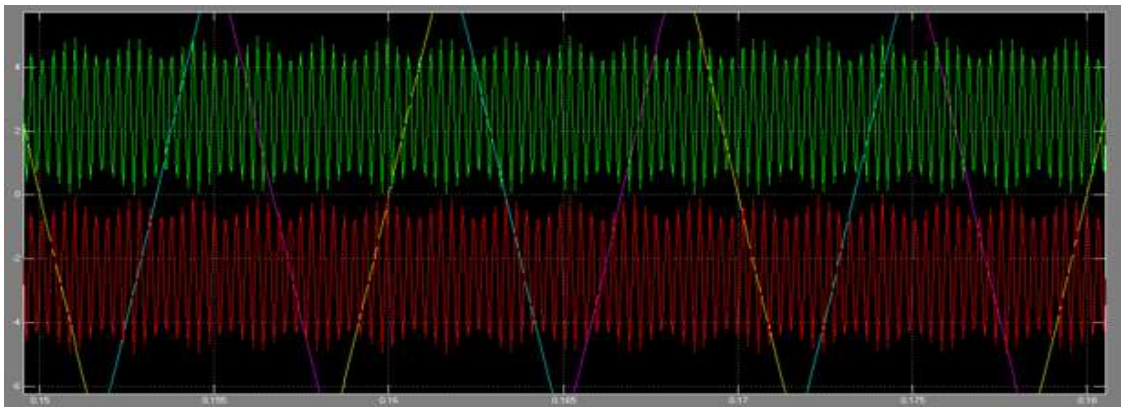

Fig (11c): Phase Disposition (PD) waveform for SPWM

Fig (10a) and Fig (10b) shows the output voltage and current waveforms of STATCOM and 3-level inverter for SVPWM method. The modulation index waveform for SVPWM is shown in fig (10c). SPWM output waveforms of voltage and current across STATCOM and 3-level inverter are shown in fig (11a) and fig (11b). Phase Disposition (PD) waveform for SPWM with carrier signal is shown in fig (11c).

V. Conclusion

This paper compares the SVPWM and SPWM techniques for 3-level multi inverter. By analyzing both the techniques it is evident that, in SVPWM the output voltage and current magnitudes are nearly identical to sinusoidal waveform and THD is negligible where as for SPWM the voltage waveform acquires nearly sinusoidal waveform but for current waveform THD is high at initial stage. Space vector Modulation Technique has become the most popular and important PWM technique for Three Phase Voltage Source Inverters for the control of AC Induction, Brushless DC, Switched Reluctance and Permanent Magnet Synchronous Motors. The Simulation study reveals that SVPWM gives lesser THD compared to SPWM. PWM strategies Sinusoidal PWM and SVPWM utilize a changing carrier frequency to spread the harmonics continuously to a wideband area so that the peak harmonics are reduced greatly.

Table (2): Comparison of SVPWM and SPWM

PARAMETER	SVPWM	SPWM
Designing	When going for higher level circuit complexity increases	Simple
THD	Less than 15%	For low levels THD is above 15% but if the levels increases THD will decrease and almost gives the same value of space vector modulation
Power Quality	High	For lower levels power quality is low
PWM switching frequency	Fixed	Fixed

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