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# A brief review of some pertinent oxidation and annealing effects on the oxide charge density and surface field-effect mobility in the SiC MOS and MOSFET devices

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***Abstract:*** *This article briefly reviews the oxidation and annealing effects on the flatband voltage of the SiC MOS device and the surface field-effect mobility of the MOSFET device. The oxide charge densities are calculated from the flatband voltages observed after processing in a MOS device. The oxide charges are found to be mainly near the $SiO_2$/SiC interface associated with the near-interface traps. NO annealing has been found to shift the flatband voltage in the p-type MOS device when Nitrogen gets incorporated only at the interface, but not in the n-type device, with both the samples having wet re-oxidised oxide. This however, does not change the slope of the Fowler-Nordheim plot in the MOS device as if only the metal-semiconductor work function difference has changed, and yields the same hole effective mass for the bulk oxide of 0.58m, with and without N at the interface. The MOS device on SiC is shown to contain near-interface traps in the oxide near the SiC conduction band associated with an E'centre that limits the channel mobility of the power MOSFET.*

***Keywords:*** *Oxidation, Annealing, Metal-Oxide-Semiconductor, Silicon Carbide.*

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## I. Introduction

Since the mid 1990s, increased impetus has been given to developing a reliable n-channel silicon carbide (SiC) power metal-oxide-semiconductor-field-effect-transistor (MOSFET). The electronic properties of SiC polytypes of 6H- and 4H- were found suitable for high power and high temperature applications. The MOSFET device was considered because the native oxide of SiC is $SiO_2$ and similarities could be found with the existing Si MOS technology. Starting with the characterization of a 6H-SiC/$SiO_2$ interface in 1994 by Brown et al., it was learnt that there are low $10^{12}$ order fixed charges and slow traps existing in the steam grown oxide and $SiO_2$/6H-SiC interface [1]. Shenoy et al. observed low oxide charge density of 9 x $10^{11}$/cm$^2$ when 6H-SiC epitaxial surface was wet oxidised at 750$^o$C with slow pull-out [2]. Lipkin and Palmour further devised the wet re-oxidation anneal at 950$^o$C for 3 hrs of the wet oxidised p-6H-SiC that reduced the fixed oxide charges and interface states to the minimum with 12 x $10^{11}$/cm$^2$ oxide charge density remaining after wet re-oxidation. They achieved a good quality oxide with a electrical breakdown strength of about 10 MV/cm [3]. This led to accepting the wet re-oxidation at 950$^o$C for 3 hrs as part of the standard oxidation procedure. In 1997, J. A. Cooper Jr. reviewed the advancement of the SiC MOS technology based on the work by M.K. Das, J.N. Shenoy and M.R. Melloch, L. A. Lipkin and J. R. Palmour and others, on 6H-SiC MOS devices [4]. The surface field-effect (FE) mobility in the 6H-SiC MOSFET has been determined to be in the range of 50-72cm$^2$/V-s with wet re-oxidised oxide having acceptor states mostly outside the 6H-SiC bandgap [3].

The Vanderbilt-Auburn research group [5-6] furthered the interface improvement, utilizing 4H-SiC MOS devices having wider bandgap of 3.23 eV than 6H-SiC having a bandgap of 3.03 eV, by introducing NO annealing at 1150-1175$^o$C for 2 hrs which passivated the Si and carbon dangling bond type interface states and reduced them to 6 x $10^{11}$/cm$^2$eV at $E_c$-0.2 eV [7-8]. It also passivated the interstitial carbon and carbon clusters with states near the conduction band (CB) and transferred them to near valence band (VB) by forming CN bonds [7]. It improved the surface FE mobility in the 4H-SiC MOSFET channel from single digit to about 25-35 cm$^2$/V-s [9]. By 2006, NO and NO+$H_2$ anneal improved the peak surface FE mobility in the MOSFET on (0001) oriented Si-face of 4H-SiC to 45cm$^2$/V-s and 55cm$^2$/V-s respectively [10]. Berens et al. have tried NO+$NH_3$ to incorporate Hydrogen, which improved mobility to 45cm$^2$/V-s but yielded reduced oxide reliability by increasing trapping at high electric fields [11]. Annealing in $NH_3$ incorporates Nitrogen throughout the oxide and removes oxygen thus changing the material to one like SiON with a lower bandgap. This increases the leakage current and lowers the electrical breakdown strength. Annealing in NO on the other hand, incorporates Nitrogen only at the interface [11-12]. $N_2$ annealing at high temperature improves peak mobility to 50cm$^2$/V-s as the best device and also yields high electrical breakdown strength of about 10 MV/cm [13]. $N_2$ is

environment-friendly gas but it requires a lot of energy to breakdown. It has high bond strength of 9.8 eV. A high density of border acceptor traps or near-interface traps in the oxide that lie within the 4H-SiC bandgap near the CB was found to limit the surface FE mobility improvements further in the 4H-SiC MOSFET device [8, 14-17]. The present article reviews some pertinent oxidation and annealing effects on the oxide charge density through the observation of flatband voltages on the 6H- and 4H-SiC MOS devices and correlates them to the surface FE mobility in the MOSFETs towards the end.

## II. Theory

In the early years of Si-MOS technology development, the interface states were called surface states and the formula used for finding the density of surface state charge was given as [18]:

$$\Delta V = Q_{ss} \frac{x_0}{K_0 \varepsilon_0} - \Phi_{MS} \quad (1).$$

Here, $Q_{ss}$ is the surface-state charge density per unit area, $\frac{K_0 \varepsilon_0}{x_0}$ is the oxide capacitance per unit area, and $\Phi_{MS}$ is the metal-semiconductor work function or barrier energy difference. Later on, the above formula was used to find the density of fixed charges $Q_f$ when it was updated after the standardized terminology for the oxide charges was introduced, as [19]:

$$V_{FB} = \Phi_{MS} - \frac{Q_f + Q_m + Q_{ot}}{C_o} \quad (2).$$

Here, $V_{FB}$ is the flatband voltage, $\Phi_{MS}$ is the metal-semiconductor work function difference, and the four types of charges in the oxide and the oxide/semiconductor interface are oxide fixed charge density $Q_f$, mobile ionic charge density $Q_m$, oxide trapped charge density $Q_{ot}$, and the interface trapped charge density $Q_{it}$. These charge densities are in Coulombs/cm$^2$. The oxide capacitance in Farads/cm$^2$ is represented by $C_o$. The interface states in the Si technology were passivated with a forming gas anneal at 450$^o$C for 30 min. This eliminated $Q_{it}$ from the formula, and the other oxide charges were determined unambiguously by different methods. The $Q_{it}$ will be part of the formula if they are high. Now, since 1992, near-interface trap or border trap charge density $Q_{bt}$ has been added [20]. These charges are different from the interface charges, which are at the interface. These are located in the oxide within 2-3 nm of the oxide/semiconductor interface. These are "slow" states and lie near the semiconductor conduction band. They are electrically active and communicate with the semiconductor CB. They are associated with E' centres in the oxide [20]. The near-interface trap or border trap charges are found in significant numbers as acceptor charges in the 4H-SiC MOS devices where the acceptor border traps lie within the 4H-SiC band gap. The trap states and pinned around 2.9 eV from the SiC VB in all polytypes. [21]. The border trap states in Si MOS device are at about 0.1 eV above the CB edge of silicon at flatband.

Oxidised silicon has mostly electrically active donor interface states in both lower and upper half of the silicon band gap [22-24]. Donor traps are positive when empty and neutral when filled while acceptor traps are neutral when empty and negative when filled. Therefore positive interface charge density for both n-type and p-type Si MOS devices are observed. Oxidised silicon carbide has donor interface states in the lower half and acceptor interface states in the upper half of the bandgap [21]. Therefore positive interface charge density is observed in the p-type SiC MOS device and negative interface charge density is observed in the n-type SiC MOS device, apart from the presence of electrically inactive fixed oxide charges in both device systems. The donor interface trap charge density at flatband in the Si/$SiO_2$ system is shown in Fig.3 of the study by Deal et al. on the oxidised n- and p-type Si<111> surface [18]. The figure shows the effect of oxidation temperature on the surface-state charge density as it was known earlier. The charge density is calculated by using equation (1). It can be observed that the p-type Si sample has a slightly higher charge density than the n-type sample at all oxidation temperatures with the difference getting larger at the lower oxidation temperatures. This is due to the difference in the $\Phi_{MS}$ value, which is -0.95 V for the Al-p-Si sample and -0.25 V for the Al-n-Si sample given the Si donor and acceptor doping is of the order of $10^{16}$/cm$^3$. The p-type Si MOS sample thus gives a slightly higher interface charge density.

## III. Results and Discussion

The development of a reliable n-channel power MOSFET on p-4H-SiC is a current worldwide objective. With this objective in view, many research groups have studied the effect of wet re-oxidation annealing at 950°C for 3 hrs on the oxides grown on p-4H-SiC and n-4H-SiC epitaxial layers. This wet re-oxidation procedure is part of the "standard" oxidation procedure for SiC MOS and MOSFET devices which is described in the study by Williams et al. [8]. The wet re-oxidation is performed on the oxides grown by dry or wet oxidation at high temperatures of 1100-1200°C followed by a 30 min inert anneal in Ar at the oxidising temperature. The effect of the wet re-oxidation on the flatband voltage is tabulated below from the studies of some of the research groups. NO annealing at 1150°C for 2 hrs is performed on the wet re-oxidised oxides, and its effect on the flatband voltage of the MOS device is also observed and analysed in terms of the oxide charge densities.

The first observation from the Table I below is that wet re-oxidation of the p-SiC/$SiO_2$ structure lowers the oxide charge density as shown by a lower flatband voltage. This has been observed before by Shenoy et al. and Lipkin and Palmour [2-3]. The second observation from column 7 and rows 3 to 6, that dry or wet oxidation in the 1100-1200°C temperature range followed by a 30 min. Ar inert anneal at the oxidising temperature finally gives the same flatband voltage of -4.3 V after performing wet re-oxidation at 950°C for 3 hrs on the p-4H-SiC/$SiO_2$ structure. That is, the final temperature and oxidising ambient decides the flatband voltage of the MOS device. This is a similar observation to that in the Si MOS technology [18]. This -4.3 V corresponds to 12 x $10^{11}$/cm$^2$ fixed positive charge density after the wet re-oxidation as calculated using equation (2), given that the metal-semiconductor work function difference between Mo gate and p-4H-SiC is 4.7-6.8 which equals -2.1 V. These charges are evidenced to be due to near-interface traps forming E' centre as Si-C-O-O with an unpaired electron [14-16]. The positive charge in the p-type device associated with the near-interface trap charge comes from the splitting of the neutral oxygen vacancy upon hole capture into the Si-C-O-O E' centre with an unpaired electron and the fixed positive charge. It is showing near the VB edge at $E_v$+0.1 eV. The calculated charge number density $Q_f/q$ from equation (2) is 12 x $10^{11}$/cm$^2$. The third observation is that the flatband voltage shift to lower voltage after wet re-oxidation is a parallel shift due to the removal of donor states whose density can be calculated by knowing the amount of parallel voltage shift.

**Table I.** The oxidation and annealing effects on the flatband voltage of the p-SiC MOS devices.

| S.No. | Reference | Oxidation condition (Ar anneal for 30min at the ox temp was common for all. | Oxide thickness (nm) | Flatband voltage after oxidation, $V_{fb}$ (V) | Wet Re-oxidation condition | Flatband voltage after wet reox. $V_{fb}$ (V) | NO annealing condition (for 2 hrs) | Flatband voltage after NO annealing, $V_{fb}$ (V) |
|---|---|---|---|---|---|---|---|---|
| 1. | Lipkin and Palmour, p-6H, [3] | Wet, 1100°C | 50 | -7.42 | 900°C for 1.5 hrs. | -5.8 | | |
| 2. | Lipkin and Palmour, p-6H, [3] | Wet, 1100°C | 50 | -7.42 | 950°C for 3 hrs. | -4.9 | | |
| 3. | Ekoue et al., p-4H, [25] | Wet, 1150°C | 50 | -9.95 | 950°C for 3 hrs. | -4.26 | | |
| 4. | Chung et al., p-4H, [7] | Wet, 1100°C | 40 | | 950°C for 3 hrs. | -4.2 | 1150 | -6.6 (Mo gate) |
| 5. | Okamoto et al., p-4H, [26] | Dry, 1200°C | 40 | -6.0 | 950°C for 3 hrs. | -4.8 (p-polySi gate) | | |
| 6. | Chung, Won, et al., p-4H, [27] | Wet, 1100°C | 40 | -6.5 | 950°C for 3 hrs. | -4.3 (Mo gate) | | |
| 7. | Chanana et al., p-4H, [5-6] | Wet, 1100°C | 40 | | 950°C for 3 hrs. | -4.3 (Should be) | 1150 | -6.0 (Au gate) |

The fourth observation is that the oxide charge density is about the same at 12 x $10^{11}$/cm$^2$ in both p-6H-SiC and p-4H-SiC MOS devices after wet re-oxidation at the lower temperature of 950°C for 3 hrs [3]. The oxide charge density observed by Shenoy et al. in the p-6H-SiC MOS device was also 23 x$10^{11}$/cm$^2$ after wet oxidation at high temperature of 1150°C and slow pull out of say 2 min. It reduced to 9 x $10^{11}$/cm$^2$ when wet oxidised at low temperature of 750°C, this being the lowest oxide charge density observed by them [2]. The fifth observation is that the flatband voltage after wet re-oxidation in the 4H-SiC MOS sample of the study by Chanana et al. [5-6] should be -4.3V although, a direct measurement after wet re-oxidation was not made. Therefore, after the NO annealing at 1150°C for 2 hrs, the flatband voltage in the p-MOS device shifts left to -6.6 V (Mo gate) [7] or -6 V (Au gate) [5-6]. These flatband voltages yield oxide charge density of 24 x $10^{11}$/cm$^2$ and 23 x $10^{11}$/cm$^2$ respectively, given that the work function of Mo is 4.7eV and that of Au is 5.1eV [5]. This

essentially means that the oxide charge density doubles after NO annealing in the p-4H-SiC MOS device when the Si-C-O-O E' centre is believed to be modified to Si-C-O-N by replacing 1O with 1N, where N has one less electron [14-16]. The study by Williams et al. [8] shows $D_{it}$ at $E_v$+3.1 eV after NO annealing as 24 x $10^{11}$/cm$^2$eV in Fig.4 of the reference representing the BTs density in the n-type device. The observed $D_{it}$ corroborates the calculated number charge density as $Q_{bt}/q$, meaning that the other types of charges become negligible after wet re-oxidation in the n-type device, as per the formulas given in equations (1) and (2) of the theory section. The interface trap density which is different from the near-interface trap density near the 4H-SiC conduction band however reduces by one order to about 6 x $10^{11}$/cm$^2$eV at $E_c$-0.2 eV after NO annealing represented by $Q_{it}/q$ [7-8, 14].

The positive charges due to donor states are present along with the 12 x $10^{11}$/cm$^2$ positive charges due to Si-C-O-O E' centres in the oxide of the p-4H-SiC MOS device after the high temperature oxidation as shown by the large negative flatband voltages. These are reduced after the wet re-oxidation as the higher negative flatband voltage shifts in parallel to lower flatband voltage of -4.3 V, and only the fixed positive charge centres remain as $Q_f/q$ . One can thus find out the number density of fixed positive charges from the parallel shift in the flatband voltage. The parallel shift is indicative of the fixed positive charges being reduced after wet re-oxidation. The author believes that there are no border traps or near-interface oxide traps near the valence band of the semiconductor/oxide interface because the displacement current in the p-type device represents the oxide displacement current only [28]. The pull out time of the wafers after high temperature oxidation is known to influence the oxide charge density with a slower pull out leading to higher charge density in Si-MOS technology [18]. The slower pull out in the SiC processing has shown a reduction in the oxide charge density [2]. This could be an important reason of higher and varied oxide charge density after high temperature oxidation as shown in Table I above in column 5.

There is contradictory evidence present in the research studies as to whether the flatband voltage shifts after NO annealing in the p-type 4H-SiC MOS device. Habersat et al. [29] pointed out that it does not shift and remains at -5 V before and after NO annealing without C-V plot to indicate and support his claim. Chung et al. [6] have claimed otherwise. Chung's study and the analysis by the author that the $N_f$ after NO annealing doubles, is a clear indication that the flatband voltage shifts left to higher negative voltages after NO annealing in the p-4H-SiC MOS device. The author in his previous article went along with the evidence of Habersat et al., but it now stands corrected [28]. The current-voltage curve through the MOS device will "adjust" according to the flatband voltage. Hole effective mass in the thermal $SiO_2$ has been determined from the p-4H-SiC MOS device to be 0.58m, m being the free electron mass by Chanana et al. [5-6] and reproduced by a Japanese research group, Nemoto et al. [30]. The SiC device has undergone the NO annealing incorporating Nitrogen at the interface and shifting the flatband voltage to the left by adding positive charges. This created doubt whether the hole effective mass in thermal silicon dioxide determined by Chanana et al. is correct or not [5-6]. Hole effective mass in thermal silicon dioxide of 0.58m, has also been determined by utilizing grounded and ungrounded n-channel MOSFETs by the author, which did not have any Nitrogen incorporated at the Si/$SiO_2$ interface [31-33]. This shows that Nitrogen which is incorporated only at the 2 nm interface in the p-4H-SiC MOS device does not affect the properties of the 40 nm thick bulk oxide. Therefore, adding Nitrogen only at the interface is like changing the metal-semiconductor work function difference only, by changing $Q_{it}/C_o$ in equation (2), with the other charges being negligibly small after wet re-oxidation and NO annealing. The slope of the Fowler-Nordheim (FN) plot will have a parallel shift as shown in the author's earlier study on p-type 4H-SiC MOS devices having Au and Mo gates [5]. The slope of the FN plot itself does not change, thus yielding the same hole effective mass of 0.58m in the oxide. A research study by Sometani et al. further convinces the author of the above analysis. The electron and hole leakage current versus gate voltage data in Fig.3of his study gives hole effective mass in the oxide as 0.58m for a hole barrier at the poly-Si anode of 4.6 eV, and for a electron effective mass in the oxide of 0.42m, the CB offset for the 4H-SiC/$SiO_2$ interface comes out to be 2.79 eV from the electron current data. The n-channel MOSFET in the study has the gate oxide grown in dry $O_2$ atmosphere at 1200$^o$C and does not have any NO annealing of the oxide [33a].

The n-type MOS device on both 6H-SiC and 4H-SiC exhibit a small positive flatband voltage of about 1 V in the 6H-device and about 2 to 2.5 V in the 4H-SiC MOS device [3, 34] after oxidation, and also after wet re-oxidation. This has also been shown by Lipkin and Palmour in Table II of their study on dry-wet $SiO_2$ at room temperature, where the net oxide charge is -10.8 x $10^{11}$/cm$^2$ in the n-6H-SiC MOS device and -26 x $10^{11}$/cm$^2$ in the n-4H-SiC MOS device [35]. The flatband voltages are attributed to the existing negative slow and deep acceptor traps [21, 34]. Since 4H-SiC has a wider band gap than the 6H-SiC, there are more acceptor states in the oxidised 4H-SiC MOS device near the conduction band [8-9], causing a larger positive flatband voltage than the MOS device on 6H-SiC. The n-type MOS device on 4H-SiC has exhibited a reproducible oxide charge density of -24 x $10^{11}$/cm$^2$ after wet re-oxidation at 950$^o$C for 3 hrs [27, 35] corresponding to a flatband voltage of 5.25 V, given that the metal-semiconductor work function difference for Mo and n-4H-SiC is 4.7-3.9 equalling 0.8 V. A flatband voltage of 5.4 V is exhibited in Fig.3a of another study by Chung et al.

[7]. The NO annealing at 1150°C for 2 hrs results in the negligible change in the flatband voltage in the n-type MOS device as shown in the Fig. 3a of the study by Chung et al [7]. Also, the author has determined the border trap density or the near-interface trap density in n-4H-SiC MOS device after NO annealing to be -24 x $10^{11}$/cm$^2$ eV by a new method based on the displacement current [14-16, 28, 36]. It is same as the oxide charge density calculated above from the flatband voltage indicating that the oxide charges are occupied BTs. It also shows negligible change in the flatband voltage after NO annealing in the n-type device. The charge density of -24 x $10^{11}$/cm$^2$ in the n-type MOS device is same in magnitude as that in the p-type device after NO annealing which led to the possibility of the charges coming from the splitting of a neutral oxygen vacancy upon hole capture into negative E' centre such as Si-C-O-N with an unpaired electron acting as BT and a positive charge trap acting as fixed positive charge in the p-type device [14-16]. The interstitial and carbon clusters acting as acceptor states in wet re-oxidised n-4H-SiC MOS device are shifted to near the VB upon NO annealing as CN bonds are formed [7].

It has been reported during the early stages of MOS technology development by Bruce E. Deal [37], that unambiguous determination of electrically inactive fixed oxide charges can be made only after minimizing the interface trap density. This is done in the Si MOS technology by annealing in forming gas at 450°C for 30 min. when the hydrogen passivates the interface states. In SiC technology, this passivation of the near-interface states has not yet been possible although the interface states have been reduced by Nitrogen from the NO annealing. Therefore, the fixed charge density can be determined unambiguously by observing the parallel voltage shift after wet re-oxidation as described above. However, from the oxide charge data of the study by Chung et al. [27], it is found that the charge density after the high temperature oxidation is 24 x $10^{11}$/cm$^2$ which reduces to 12 x $10^{11}$/cm$^2$ after wet re-oxidation. Thus the reduced fixed oxide charge density must be 12 x $10^{11}$/cm$^2$. The Table II below, in its revised form from the author's previous study [15-16] tries to give a plausible scene of charges during the oxide processing in 4H-SiC MOS devices with the study by Chung [27] and Chanana [16] in view. The total $Q_f$ after high temperature oxidation may vary, but the Si-C-O-O E'related fixed positive charge density remains the same at 12 x $10^{11}$/cm$^2$ after the wet re-oxidation. This density doubles to 24 x $10^{11}$/cm$^2$ after NO annealing due to the possible formation of Si-C-O-N E'charges as near-interface charges when replacement of 1O by 1N has one less electron.

**Table II**. Processing effects on the wet oxidised 4H-SiC Si-face (0001) oriented surface.

| Device type | $N_f$ in p-type MOS (x $10^{11}$/cm$^2$) | $N_f$ in n-type MOS (x $10^{11}$/cm$^2$) |
|---|---|---|
| High temperature (1100°C) wet oxidation followed by Ar inert anneal | 24 (12 from (Si-C-O-O) E' positive charges + 12 from donor states in the lower half of the bandgap | -12 from (Si-C-O-O) E' negative charges, |
| Wet re-oxidation at 950°C for 3 hrs | 12 (fixed positive charges from (Si-C-O-O) E' centres + reduced donor states | -12 from carbon acceptor traps plus -12 (Si-C-O-O) E' acceptor centres giving a total of -24 acceptor states |
| After NO annealing at 1150°C for 2 hrs causing fresh oxidation at the interface | N replaces O to add a positive charge doubling the density of fixed positive charges to 24 by forming Si-C-O-N (E' centres) or Si-N-N-N bonds at the interface. | N doubles the density of E' centres having an unpaired electron to 24and makes them neutral with even number of electrons, and carbon acceptor states are passivated with N to form states near the VB. |

Summarising the above results and analysis points to the fact that the oxide charge density in both n-type and p-type 4H-SiC MOS device having undergone NO annealing is -24 x $10^{11}$/cm$^2$ and 24 x $10^{11}$/cm$^2$ [14]. They are equal in magnitude suggesting the association of E'centre from a neutral trap. The E' molecule suggested is Si-C-O-N bonded molecule with an unpaired electron in the n-type device and Si-C-O-N bonded positive charge from the same trap upon hole capture in the p-type device. Before NO annealing, Si-C-O-O bonded E' centres exist as a near-interface traps in the n-type device and the associated fixed positive charges exists in the p-type device, both having a density of 12 x $10^{11}$/cm$^2$. Here O is present in place of N with one extra electron causing the charge density to be half of that after NO annealing. This further correlates to the interface state charge density in Si<111> MOS device with Si<111> having almost the same planar density of atoms as the (0001) oriented surface of 6H- and 4H-SiC [14]. The interface state charge density in the above Si MOS device is determined to be 4 x $10^{11}$/cm$^2$ in both n- and p-type wet or dry oxidised Si<111> surface with 920°C as the final wet oxidation temperature [18]. The border trap density in Si MOS is also determined to be 4 x $10^{11}$/cm$^2$ eV where the Si is oxidised at 1000-1200°C [38]. This is close to the 950°C wet re-oxidation temperature in the SiC MOS device processing described above. Si-O-O-O E' centre with an unpaired electron is formed as the near-interface trap in the Si-MOS from the neutral oxygen vacancy upon hole capture. This does not have Carbon but Oxygen with two extra electrons, reducing the oxide charge density three times to 4 x $10^{11}$/cm$^2$. The 6H-SiC MOS device is found to behave similarly with the oxide charge density after wet re-oxidation to be 12 x $10^{11}$/cm$^2$. The total oxide charge density is the sum of interface trap charge density and the near-interface trap charge density. These add up to give a charge density of 30 x $10^{11}$/cm$^2$ in the 4H-SiC MOS

device. This minimum oxide charge density of 30 x $10^{11}/cm^2$ as border acceptor traps and interface traps after NO annealing limits the surface FE mobility in the n-channel 4H-SiC power MOSFET to about 35 to 45 $cm^2$/V-s as discussed in the author's earlier studies [9-10, 16]. The author is not too hopeful that it can be increased further to any substantial amount as this is the minimum oxide charge density achievable after wet re-oxidation and NO annealing.

The Table III below highlights another aspect of the $SiO_2$/SiC interface. The oxide charges have been found to be located mainly near the SiC/$SiO_2$ interface where there could be Si-C-O bonds apart from the Carbon and Si dangling bonds as interface traps. When the n-doping is 5-8 x $10^{15}/cm^3$ in the 6H-SiC epi-layers, the flatband will occur at $E_v$ +2.8 eV which is the position of the Fermi level. Equation (2) will then yield -10.8 x $10^{11}/cm^2$ charge density at the interface of the n-type device [8, 35]. But the border traps (BT) in the oxide are pinned at 2.9 eV which is 0.13 eV inside the 6H-SiC CB and above the Fermi level. Their density is about double to that at $E_v$ + 2.8 eV. It is -24 x $10^{11}/cm^2$ at $E_v$ + 2.9 eV [8, 21]. In the p-type 6H-SiC MOS device also, the net oxide charge density calculated by using equation (2) is shown to double for the heavily Boron doped sample doped at 1 x $10^{17}/cm^3$, when the flatband will be at 0.13 eV inside the VB (the position of Fermi level) opposite to $E_v$ + 2.9 eV [3]. The fixed positive charge part of the E' centre due to BTs in the oxide seems to have been added to the p-type device near the VB. This is similar to the doubling of the positive charge in the p-4H-SiC MOS device upon NO annealing as shown in the Table III below. The author was with the Auburn-Vanderbilt group where n-epilayers on 4H-SiC having a bandgap of 3.23 eV were doped with 8-9 x $10^{16}/cm^3$ giving the position of the Fermi level 0.134 eV inside the 4H-SiC CB at $E_v$ + 3.1 eV at flatband. The calculated oxide charge density using equation (2) and the $D_{it}$ characterization by the high-low C-V method yielded the BT density of 24 x $10^{11}/cm^2$ as the BTs are pinned at 2.9 eV which is below the Fermi level. The NO annealed 4H-SiC MOS samples in the Table III below have wet oxidised/wet re-oxidised oxide that showed doubling of the positive oxide charge density [8, 14, 27]. Semiconductor bulk defects such as $EH_5$ and $Z_{1/2}$ also manifest themselves as interface states in the 4H-SiC MOS device at about $E_v$ + 2.2 eV and $E_v$ + 2.6 eV respectively [8]. These have also been found in the 6H-SiC MOS device. Their defect densities on the oxidised SiC surfaces are reduced after NO annealing [8].

The surface FE mobility in the 6H-SiC MOSFET device is influenced by the larger density of slow border traps and is calculated to be 35$cm^2$/V-s at high oxide fields by Lipkin and Palmour [35]. There is therefore no significant improvement in mobility of the MOSFETs on 6H-SiC as compared to those on 4H-SiC. The border trap density near the CB of 24 x $10^{11}/cm^2$ in both the polytypes of SiC thus limits the surface FE mobility in the MOSFETs to 35-45$cm^2$/V-s as discussed above. The 4H-SiC MOS device is found to respond better to NO annealing than the 6H-SiC MOS device. From the previous study by the author [16], it is proposed that, with the knowledge of the correct surface FE mobility of one MOSFET device and the total interface state density of the corresponding MOS device, the mobility in any MOSFET device on any semiconductor can be determined solely from the study of a MOS device on a semiconductor because mobility is inversely proportional to the total interface state density in the MOS device, given that the mobility is limited by Coulomb scattering. This conclusion led the author to give a close estimate of the surface FE mobility of a GaN MOSFET device as 45$cm^2$/V-s [16].

**Table III.** The oxide charge density and mobility in the 6H- and 4H-SiC MOS devices after processing.

| References for oxide charge density | Device | Oxide charge density in p-6H-SiC MOS device (x $10^{11}/cm^2$) | Oxide charge density in n-6H-SiC MOS device (x $10^{11}/cm^2$) | Field-effect Mobility in the MOSFET[reference] ($cm^2$/V-s) |
|---|---|---|---|---|
| [3, 35] | Wet re-oxidised | 6.9, 10.0 | -10.8 | Best 50-70 [3]<br>35 at gate voltage of 5V above threshold [35] |
| [8] | NO annealed | - | -10.8 at $E_v$ + 2.8 eV<br>-24 at $E_v$ + 2.9 eV (BTs) | |
| | Device | Oxide charge density in p-4H-SiC MOS device (x $10^{11}/cm^2$) | Oxide charge density in n-4H-SiC MOS device (x $10^{11}/cm^2$) | |
| [27, 35, present study] | Wet re-oxidised | 12 | -24, -26 (BTs) | |
| [8, 14, 17] | NO annealed | 23.6 (doubles) | -23.5 | 25-35 [9] |
| | | Mainly $Q_f$ from fixed positive charges | Mainly $Q_{bt}$ + $Q_{it}$ from BTs and Interface traps | |
| | | Flatband voltage changes in p-type device after NO annealing in the 1100-1200°C range for 1 to 2 hrs. | Flatband voltage does not change in n-type device after NO annealing in the 1100-1200°C range for 1 to 2 hrs. | |

The limitation on mobility in the MOSFET device due to border traps after Nitrogen incorporation at the $SiC/SiO_2$ interface can be removed by reducing the border traps which are within 3 nm of the interface in the oxide. So having 1 nm oxide grown by rapid thermal process which reduces the border trap density, followed by atomic layer deposited $Al_2O_3$ is a possible solution, when the surface FE mobility can be increased to well above $100cm^2/V$-s in the MOSFET on (0001) oriented Si-face of 4H-SiC [39-40]. However, the leakage current would increase and the electrical breakdown strength of the dielectric will go down due to the use of lower bandgap $Al_2O_3$ as discussed earlier by the author [36]. The justification of the use of $Al_2O_3$ lies in the fact that the maximum oxide field in the MOSFET has to be 2 MV/cm ideally in the on-state, which is quite low and so one can think of substituting the thick $SiO_2$ by 1nm $SiO_2/Al_2O_3$ stack [41-42]. It is worth mentioning that it does not do much good to completely remove the $SiO_2$ as the peak FE mobility obtained is $52cm^2/V$-s which is a small improvement over mobility in the MOSFET having NO annealed oxide of $35\text{-}45cm^2/V$-s [43]. The author thinks that a 1 nm oxide for a device meant to be operated at high temperatures of above $150^oC$ is a delicate and unreliable proposition.

## IV. Conclusions

The following conclusions are made from the review. First, the wet re-oxidation lowers the oxide charge density in both the 6H- and 4H-SiC MOS devices. Second, the final oxidation temperature and ambient decides the obtained flatband voltage. Third, the oxide charges are mainly near the interface of the n-type and p-type silicon carbide MOS devices in the form of border traps or near-interface traps associated with an E' centre and a positive charge trap, split from a neutral oxygen vacancy upon hole capture. Fourth, the density of border trap charges is $-24 \times 10^{11}/cm^2$ in the n-type device and the associated fixed positive charge density of $24 \times 10^{11}/cm^2$ in the p-type device after NO annealing of the wet re-oxidised oxide on Si-face of the 6H- and 4H-SiC (0001) oriented surface. Fifth, the border trap density is correlated to charge density in Si MOS device processed at about the same final oxidation temperature and ambient by a factor of 3 in the charge densities before NO annealing. The interface trap density after NO annealing is $6 \times 10^{11}/cm^2$ at $E_c$-0.2 eV in the 4H-SiC MOS device. These limit the surface FE mobility in the n-channel SiC power MOSFETs. Sixth, a possibility of using an alternative dielectric such as $Al_2O_3$ exists to improve mobility beyond $100cm^2/V$-s in the power MOSFET fabricated on (0001) oriented Si-face of SiC epi-surface. Finally, it is concluded that the study of a MOS device is powerful enough to give a close estimate of surface FE mobility in a MOSFET device fabricated on any semiconductor.

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