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A new symmetrical multilevel inverter topology for solar photovoltaic system

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Abstract:*In this paper a new symmetrical seven level multilevel inverter is proposed. The input source for the multilevel inverter is a series combination of three PV arrays. In this paper we compare the outputs of three phase bridge inverter and seven level multilevel inverter for input of a PV system. Here two cases are considered. In first case, PV module output is applied to three phase full bridge inverter. In second case, PV module output is applied to symmetrical seven level inverter. The more the number of PV modules the more the number of voltage levels, the more faithful is the output sinusoidal waveform. In the proposed topology, both voltage pulse width and height are modulated and precalculated by using a pulse width and height modulation so as to reduce the number of switching states and the Total Harmonic Distortion (THD). In the proposed model the total harmonic distortion is very much reduced compared to the three phase bridge inverter. The efficiency and power quality is greatly improved by the use of proposed symmetrical seven level inverter.*

Keywords*: Symmetrical seven level inverter, PV module, pulse width modulation (PWM), three phase bridge inverter, total harmonic distortion (THD), power quality, multilevel inverter (MLI).*

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I. Introduction

There has been increase in demand for electrical energy all over the world. With increase in population, industrialization and globalization, the per capita consumption of electrical energy demand is more. To meet the increased demand, there is increase in requirement for installation of alternative energy sources. Therefore renewable energy sources (RES) have been in demand and installed at distribution level in the power system to support supply-demand balance equation. Solar power plant is widely used nowadays to support the power system. But the main issue is the dynamic nature of input for RES[1]. In prime mover based generators, turbines are rotated at constant speed to maintain constant frequency. The frequency mismatch is the main challengewhen solar power plant is installed and connected to grid[2]. Rated frequency can be obtained by designing a proper inverter[3]. Photo voltaic (PV) module is modelled and the output is provided to inverters.Conventional inverters produce two levels in the output voltage which has high harmoniccontent. There evolves the concept of production of multilevels in the output of the inverter. There are many multilevel inverters in usage but they are operating at high switching frequency. Therefore a new symmetrical multilevel inverter is designed to operate at line frequency of 50Hz so that switching losses are reduced[4,5].The pulse width modulation (PWM) technique is used in which 'phase and level shifted reference modulation' technique is applied. The THD content in the current waveform for single phase loads is greatly reduced and the power quality is improved by the proposed multilevel inverter [6, 7, 8].

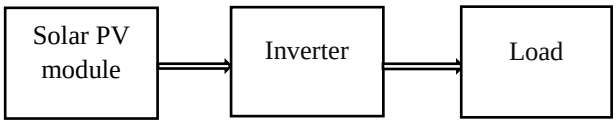

Fig1: Basic block diagram of this paper

II. Solar energy system

An ideal solar cell can be considered as a current source. The current produced by it is proportional to solar irradiation intensity falling on it. The recombination losses are represented by the diode connected parallel to the current source but in the reverse direction. The ohmic losses in the cell occur due to the series and shunt resistances denoted by R_s and R_p respectively.

Equivalent circuit of PV cell

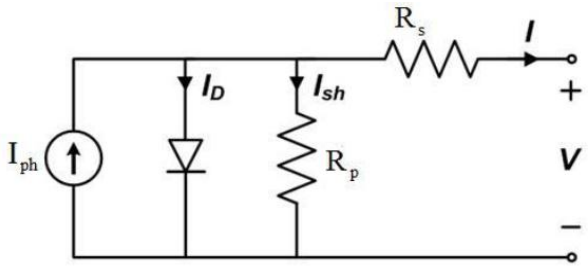

Fig2: Electrical equivalent of PV cell

Where,

$$I_{ph} = photon\ current$$
$$I_D = diode\ current$$
$$I_{sh} = shunt\ current$$
$$R_p = parallel\ resistance$$
$$R_s = series\ resistance$$

PV array modelling

N_sModules are connected in series to produce array voltage V.
N_pModules are connected in parallel to produce array current I.

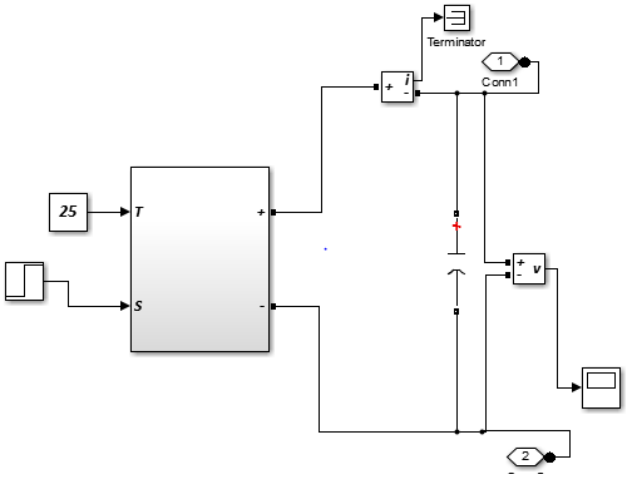

Fig3: PV main system modelling

Data sheet values

Short circuit current (I_{sc})=8.65A
Open circuit voltage(V_{oc})=44.1V
Short circuit current temperature coefficient (K_i)=0.067
Open circuit voltage temperature coefficient (K_v) =-0.33
Number of modules in series (N_s)=5
Number of modules in parallel (N_p)=10
Nominal operating cell temperature (NOCT) =T_c=T=47^0C
Ambient Temperature (T_r)=25^0C
Diode ideality factor (a)=1.2
Boltzmann's constant (k)=1.3806× 10^{-23} J/K
Electron charge (q) =1.6× $10^{-19}C$
Series resistance (R_s) =0.2Ω
Shunt resistance (R_p)=1000Ω
Capacitance=3300× $10^{-6}F$

Subsystem modelling:
Thermal voltage(V_t)equation

$$V_t=\frac{N_s\times k\times T_c}{q} \quad (1)$$

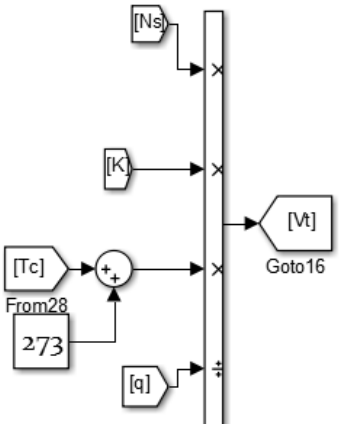

Fig4: Thermal voltage modelling

Panel shunt resistance current (I_p) equation

$$I_p=\frac{V+IR_s}{R_p} \quad (2)$$

V=array voltage
I=array current

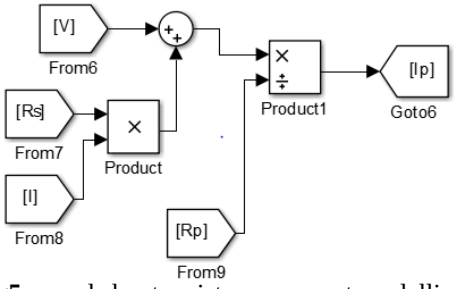

Fig5: panel shunt resistance current modelling

Diode current(I_D) equation

$$I_D=I_{rs}\left(exp\left(\frac{V+IR_s}{aV_T}\right)-1\right) \quad (3)$$

Where $I_{rs}=N_p\left[\frac{NOCT+k_i(T-T_r)}{\exp\left(\frac{V_{oc}+k_v(T-T_r)}{aV_t}\right)-1}\right]$ (4)

I_{rs}=reverse saturation current

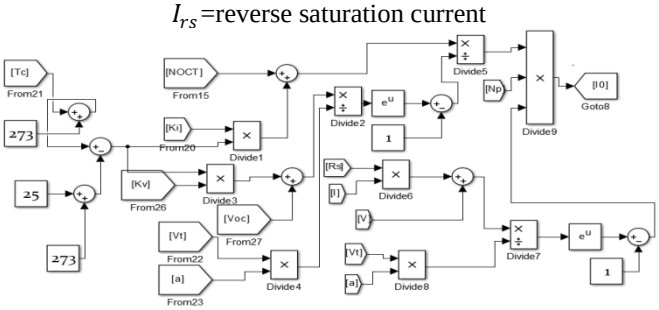

Fig6: Diode current modelling

Panel current (I_{pv}) equation

$$I_{pv}=N_p\times I_{ph} \quad (5)$$

Where $I_{ph}=I_{sc}+k_i\times$ (T-T_r)G(6)
Where G=S/1000
S=1000w/m2
S=solar irradiation

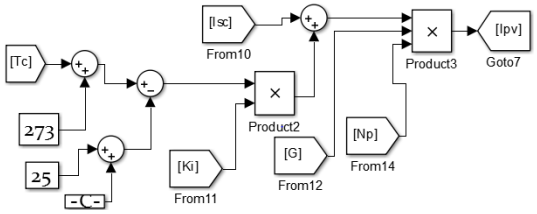

Fig7: panel current modelling

Pv array current(I) equation

$$I=I_{pv}-I_D-I_p \quad (7)$$

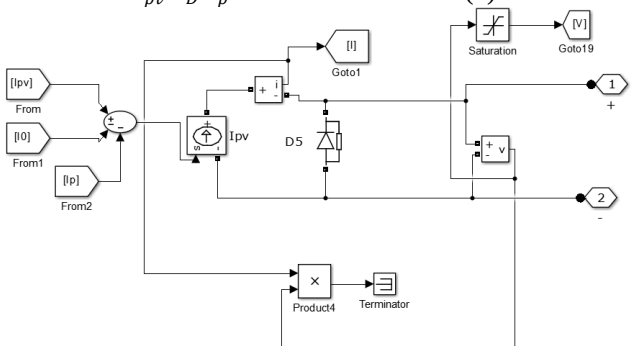

Fig8: pv array current modelling

Three such PV arrays are connected in series to produce the rated voltage of 132.3V.This voltage is given as input to the inverter.

III. Inverter modelling

In this section design of two kinds of inverters is mentioned. The first one is universal bridge inverter taken from the simulink library browser.The second one is proposed multilevel inverter designed specifically to improve the power quality to a greater extent. The same input voltage is given to both inverters.

Universal bridge inverter modelling

The series combination of three PV modules modelled in section 2 is connected to the input dc terminal of the universal bridge inverter. The universal bridge topology is considered from the simulink library.

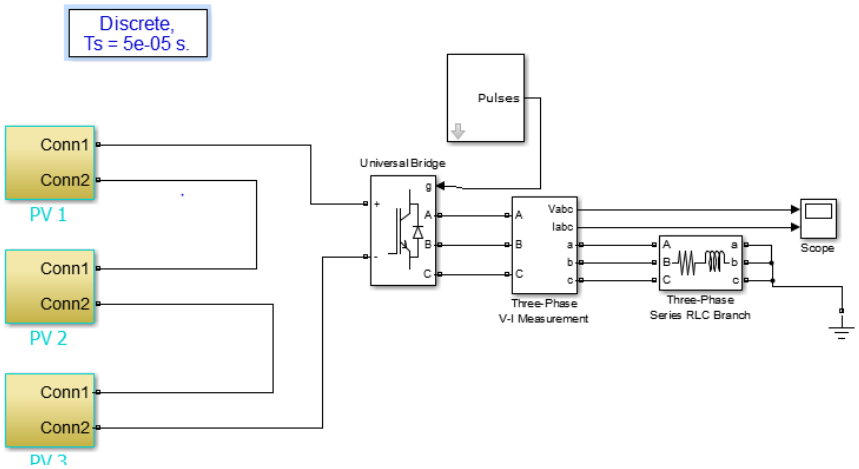

Fig9: modelling of photo voltaic driven universal bridge inverter

The inverter is named after the switching combination used for its operation. There can be many switching configurations used for universal bridge inverter. In this paper the anti parallel combination of IGBT and diode is used as a switch. The protection components called as snubber circuit parameters connected across the switch are

Snubber resistance(rs)=1e5Ω

Snubber capacitance(cs)=inf

Onstate resistance(ron)=1e-3Ω

Pulse width modulation

Discrete pwm generator block is considered from the library browser.One referencewave(sinusoidal) and one carrier wave(triangular) is considered in this 'sinusoidal pulse width modulation' technique.

Table no 1: parameter table

Parameter	Value
Generator mode	3 arm bridge(6 pulses)
Carrier frequency	2000Hz
Modulation index	0.4
Frequency	50Hz

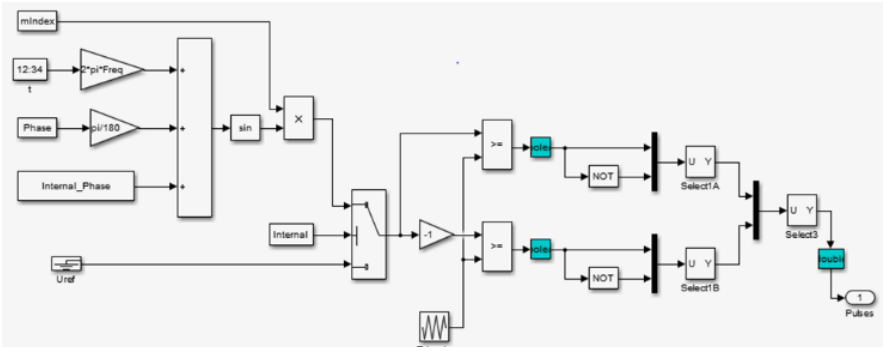

Fig10: modelling of pwm for universal bridge inverter

The pulses are given to drive the gate circuit of the bridge inverter.

The operation of this universal brige inverter is compared with the proposed multilevel inverterdesigned in the following topic.

Multilevel inverter modelling

There are many inverters designed to produce more than two levels in the output voltage in the process of improving power quality[9]. The main purpose of designing the inverter to produce multilevels is to eliminate the harmonic content in the output voltage. Some of the multilevel inverters include diode clamped MLI,flying capacitor MLI and hybrid MLI. The multilevels are produced in such inverters based on the pwm technique used. Pwm technique differs on the basis of conduction period of the switch used. The maximum conduction period of a switch in an half cycle is 180^0. So ultimately the inverter is designed based on the unique pwm technique used.The input voltage to both universal bridge and multilevel inverters is same.

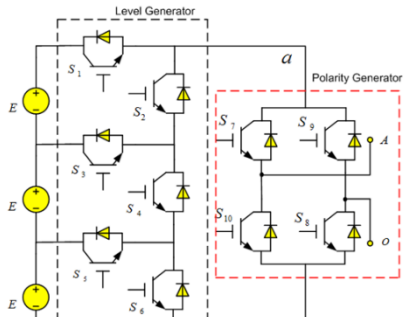

Fig11: The electrical equivalent circuit of symmetrical seven level inverter

E is equal to voltage of each pv unit. The positive terminals of three pv sources are connected to collector terminals of S1,S3 and S5.

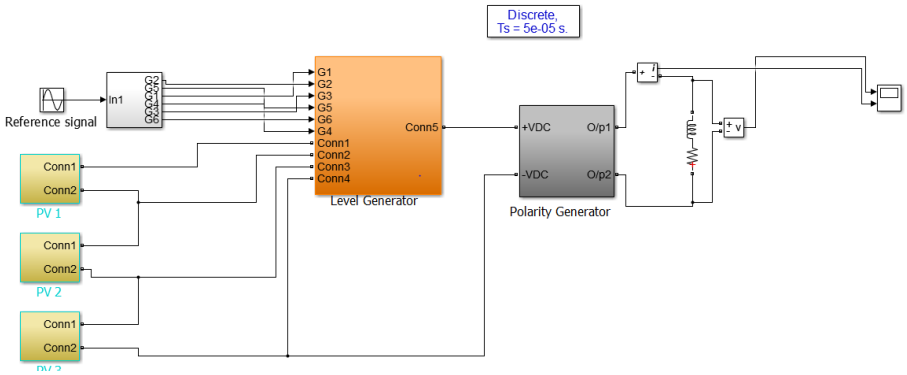

Fig12:multilevel inverter complete block diagram

Level generation

The stable voltages generated in the output are E,2E,3E,0,-3E,-2E and –E.Out of which there are four different levels of voltage which are 0,E,2Eand 3E.The switches used to produce these four voltage levels are S1,S2,S3,S4,S5 and S6.

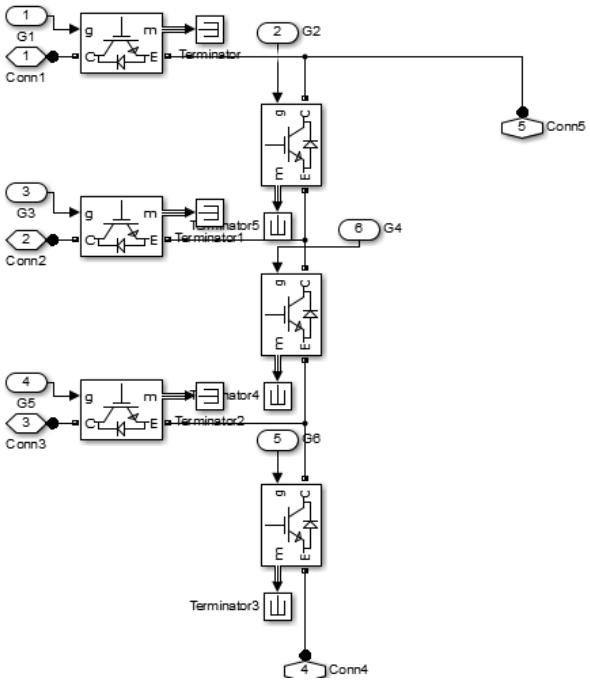

Fig13:level generator modelling

Polarity generation

The polarity of the output voltage is positive when S7 and S8 are on and negative when S9 and S10 are on.

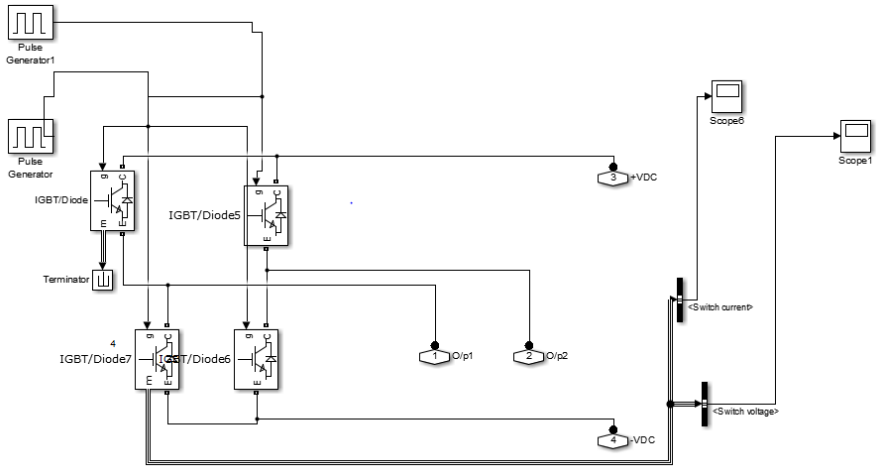

Fig14:polarity generator modelling

Table no2:Switching state table

Voltage value	Level generation switches in on state	Polarity generation switches in on state
E	S2,S4,S5	S7,S8
2E	S2,S3	S7,S8
3E	S1	S7,S8
0	S2,S4,S6	Not required
-E	S2,S4,S5	S9,S10
-2E	S2,S3	S9,S10
-3E	S1	S9,S10

The objective of this section is to produce the voltage levels mentioned in the above table by designing the logic equation for the switches S1 to S10.

Pulse width modulation

In this technique the reference signal used is sinusoidal and the carrier signal used is triangular. Three reference signals with different levels and phases and one carrier signal is used to meet the requirement.

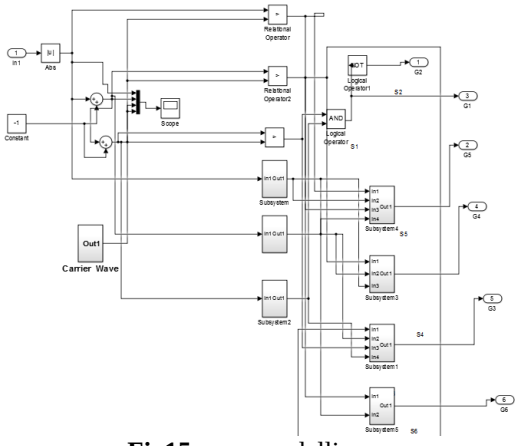

Fig15:pwm modelling

Pwm switching signal generation

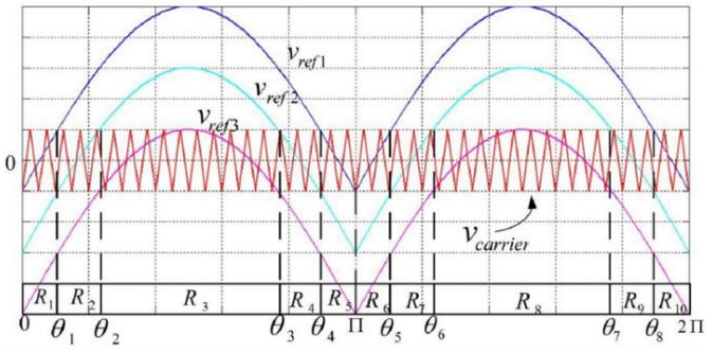

Fig16: pwm technique

State1: $0<\omega t<\theta 1$ and $\theta 4<\omega t<\pi$
State2: $\theta 1<\omega t<\theta 2$ and $\theta 3<\omega t<\theta 4$
State3: $\theta 2<\omega t<\theta 3$
$Modulation\ index(M_a)= (V_m/3V_{cr})$
V_m = amplitude of reference signal
V_{cr} = amplitude of carrier signal
$V_{cr} = V_m \sin\theta 1$ therefore $\theta 1 = sin^{-1}(V_{cr}/V_m)$ and same as $\theta 5$.

$$\theta 2=\theta 6= sin^{-1}(V_{cr}/V_m)$$
$$\theta 3= \pi-\theta 2$$
$$\theta 4= \pi-\theta 1$$
$$\theta 7=2\pi-\theta 6$$
$$\theta 8=2\pi-\theta 5$$

Pwm modelling

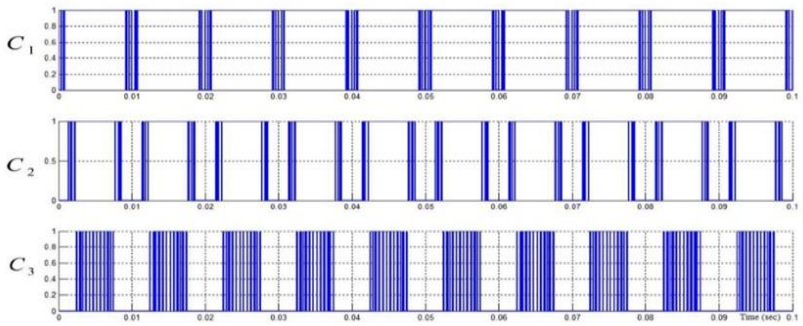

Fig17: The output levels of three comparators C1,C2 and C3

R1 to R10 are the regions.The interaction of each reference signal with carrier signal is considered a separate region.In an half cycle of the reference wave, there are five such regions. The logic equation for level generated switches S1 to S6 depend on the output of level of three comparators and intersection region of reference and carrier signals.

$$S_1= C_3 * R_3$$
$$S_2= \bar{S}_1$$
$$S_3=C_2*[R_2+R_4]+\bar{C}_3*R_3$$
$$S_4=\bar{C}_2*[R_1+R_2+R_4+R_5]$$
$$S_5= C_1*[R_1+R_5]+\bar{C}_2*[R_2+R_4]$$
$$S_6= \bar{C}_1*[R_1+R_5]$$

The gate logic signals for switches S1 to S10

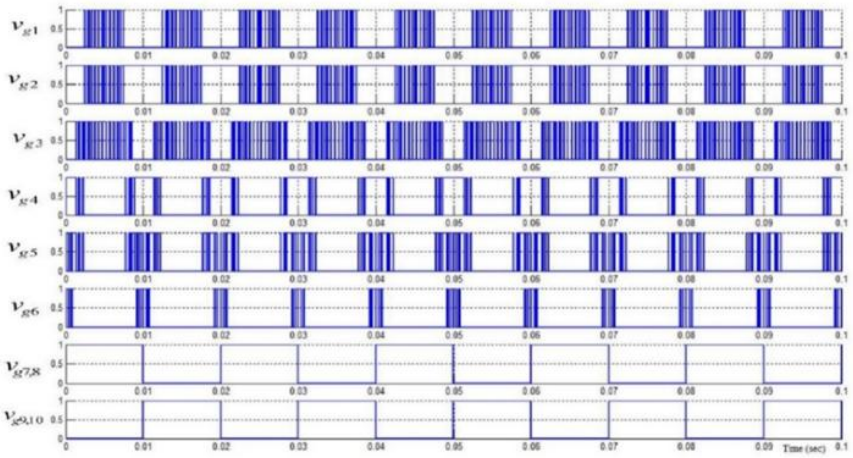

Fig18: complete gate signals

The level generated switches S1 to S6 operate at high frequency while the polarity generated switches S7 to S10 operate at line frequency 50Hz. This is the advantage of proposed switching configuration in which the less operating frequency leading to reduction in switching losses improving the efficiency of the inverter [10].These switches are operated accordingly to generate seven levels in the output voltage which is the objective of the paper.

IV. Simulation results

The output voltage of one PV aray is 44.1V. Three such identical PV arrays are connected in series to produce 132.3 V. This dc voltage is given as input to two types of inverters. The output of inverter is alternating in nature which drives the load.

First case: For three phase bridge inverter

The universal bridge inverter is considered from the Simulink library browser in which "IGBT in anti parallel with diode" combination is used as switch.Three arm and six pulse bridge configuration is used

For three phase resistive load

R=16.66Ω

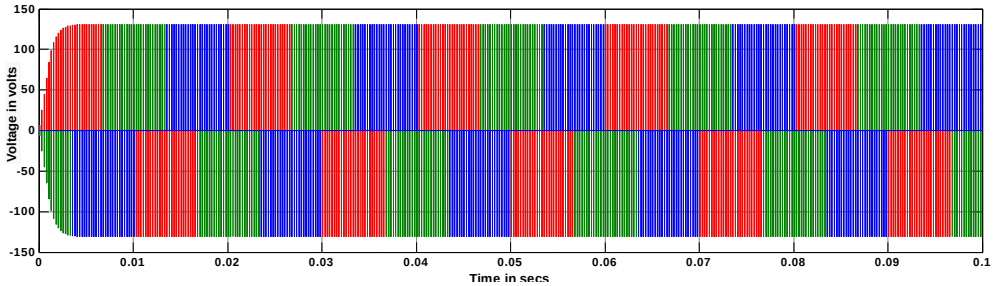

Fig19: Three phase line voltage for R load

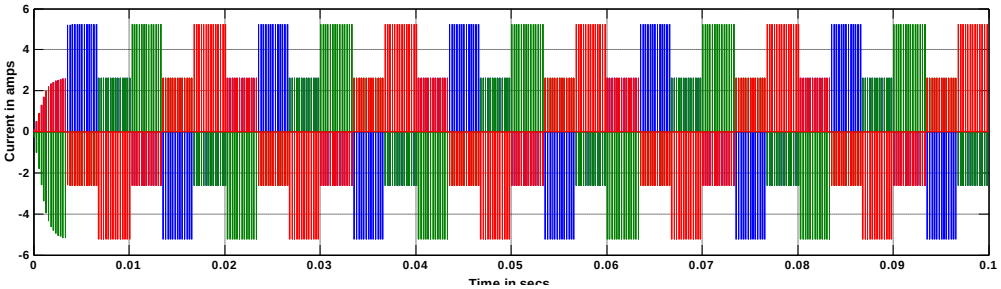

Fig20: Three phase phase current for R load

The peak value of output line voltage is 132.3V.The peak value of load current is 4.584A. Two levels are produced in the output voltage waveform.

For three phase RL load
R=16.66Ω
L=0.01H

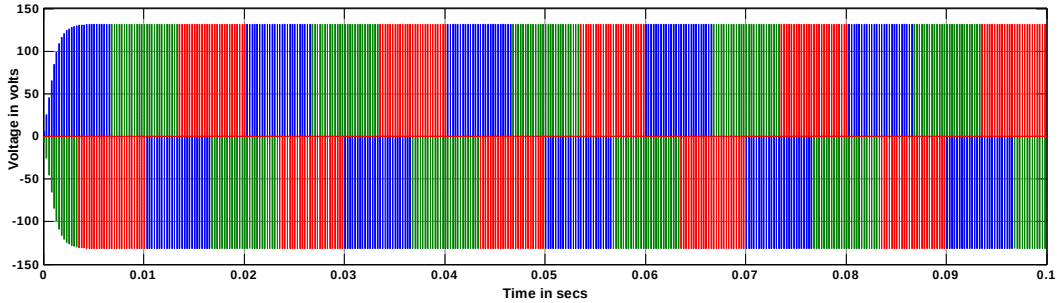

Fig21: Three phase line voltage for RL load

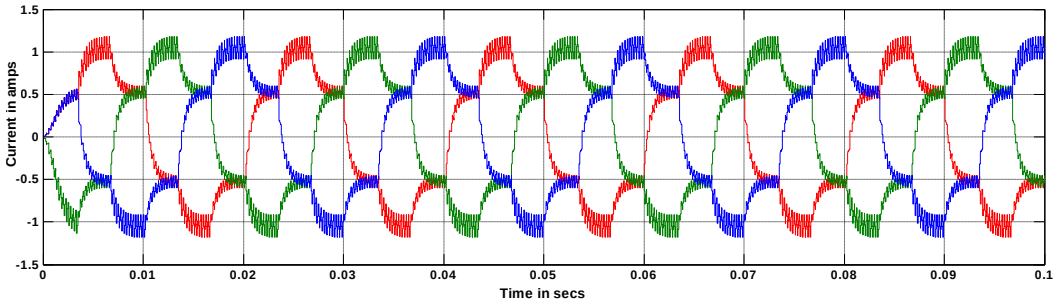

Fig22: Three phase current for RL load

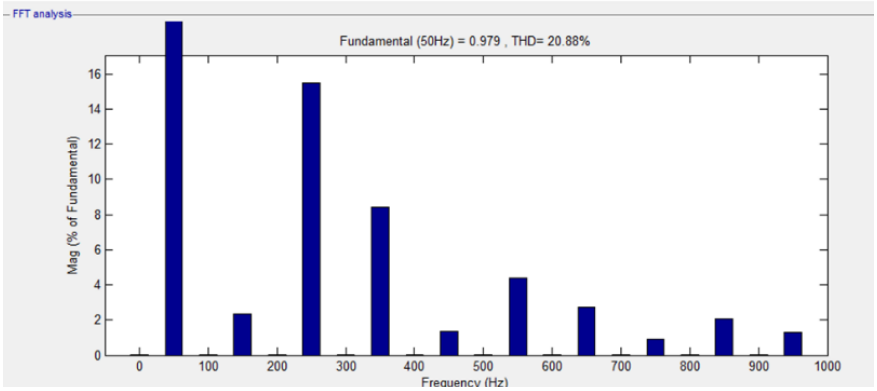

Fig23:%THD of output current waveform of three phase bridge inverter feeding RL load

The above graph represents the total harmonic content that exists in the current waveform which can be obtained by using FFT analysis.The voltage waveform remains same and current waveform varies when compared to resistive load. THD in current waveform=20.88%.The peak value of load current is 1.2A.

Second case:For Multilevel inverter
This symmetrical multilevel inverter is designed by Using 10 Switches and 10 diodes only but in remaining topologies more number switches are required.
For single phase R load
R=50Ω

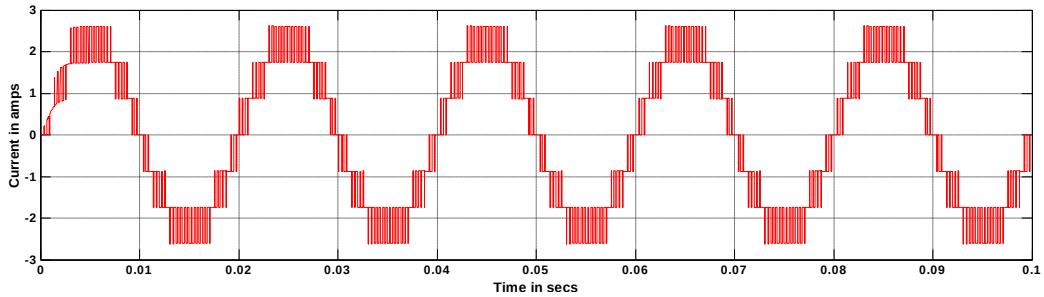

Fig24: single phase voltage waveform for R load

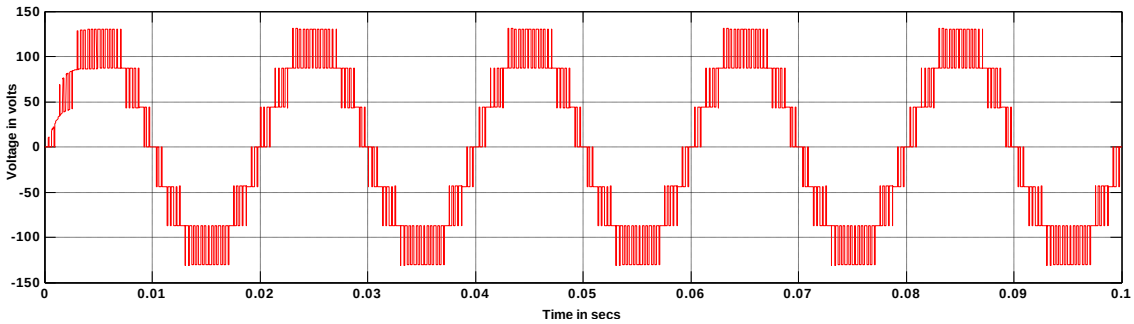

Fig25: single phase current waveform for R load

The line voltage and phase current waveforms are observed.The peak voltage is observed to be 132.3V.The peak current is 2.646A.Seven levels are produced in the output voltage waveform.

For single phase RL load

R=50Ω

L=0.03H

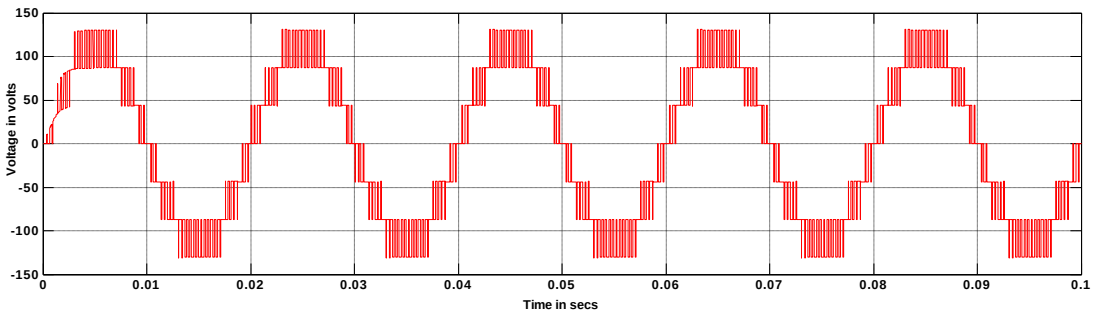

Fig26:single phase voltage waveform for RL load

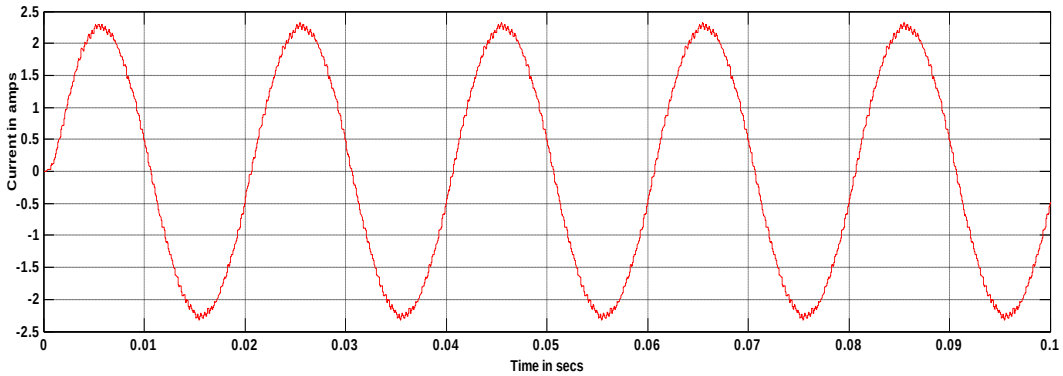

Fig27: single phase current waveform for RL load

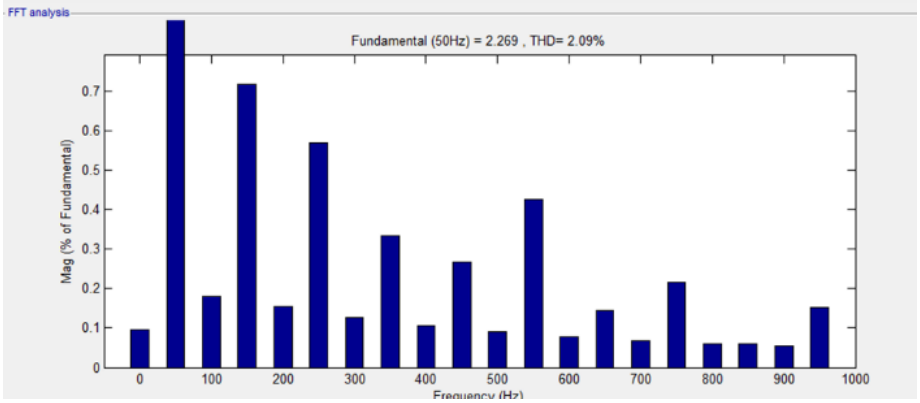

Fig28:%THD of output current waveform of the multilevel inverter feeding RL load

The above graph represents the total harmonic content that exists in the current waveform which can be obtained by using FFT analysis.
The peak voltage remains same.The peak current is 2.45A.THD obvserved in current waveform is 2.09%**.**

Result analysis

The voltage remains same in all the cases. The current waveform follows the voltage for resistive loads and changes for RL loads.

Total harmonic distortion observed in current waveform of RL load in three phase bridge inverter is 20.88% whereas in proposed MLI it is 2.09%. so THD is greatly reduced in proposed symmetrical multilevel inverter.

In universal bridge inverter for RL load 15^{th} harmonic is least in magnitude. Least harmonic content(LHC) is equal to 0.9229% of fundamental component. In the output current waveform only odd harmonics are present.In multilevel inverter for RL load 19^{th}harmonic component is least. Least harmonic component(LHC) is 0.05415% of fundamental component.

Though even harmonics are present along with odd harmonics the harmonic content of each component is greatly reduced by the use of multilevel inverter.So the proposed multilevel inverter enabled reduction in harmonic content to a great extent improving the power quality.

V. Conclusion

In this proposed model, source is three PV arrays which are connected in series where the voltage and current of PV arrays is maintained at standard operating conditions. The output of the PV module is given to the symmetrical multilevel inverter.The output voltage of the proposed multilevel inverter is symmetrical and has seven levels. The harmonic content is greatly reduced from three phase bridge inverter to multilevel inverter. For proposed symmetrical multilevel inverter there are less number of switches compared to other topologies.As the switching speed of the multilevel inverter is less, switching losses are reduced . The low frequency switching reduces the inverter power losses leading to a better efficiency of the proposed topology. Total harmonic distortion is reduced to a great extentby the use of proposed multilevel inverter.Thus power quality is improved by the proposed seven level inverter.The proposed MLI topology can be a good solution to feed microgrids from RESs.

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