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Notes on Interface traps in 4H-Silicon Carbide Metal-Oxide-Semiconductor devices

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Abstract: *Two observations and their analysis are performed in this short communication. One, the bulk defects $Z_{1/2}$ and EH_5 in the 4H-SiC epitaxial layers manifest themselves as SiO_2/4H-SiC interface states in the MOS device fabricated on them due to their high volume density. Two, there is new evidence suggesting formation of silicon nitride at the oxide/SiC interface after nitric oxide annealing of the oxidised 4H-SiC epitaxial surface resulting in K^0 defects that act as E' centres. The formation of either C-O-N bonds or N-N-N bonds at the interface keeps the fixed charge and near-interface trap density the same due to equal number of electrons in the bonds. Also, the charge correlation with Si<111>/SiO_2 structure remains unaffected due to the formation of either type of bonds at the SiO_2/4H-SiC (0001) interface.*
Keywords: *Defects, metal-oxide-semiconductor, Silicon Carbide, Silicon, NO annealing.*

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I. Introduction

Defects could be present in the bulk of a material such as a semiconductor or an insulator or it could be present at the semiconductor/insulator interface or metal/semiconductor interface. In semiconductors crystals, point defects are zero-dimensional defects. They can physically be a vacancy (Schottky defect), an interstitial, a vacancy-interstitial pair (Frenkel), extrinsic point defect as an impurity atom, or a split interstitial defect. In a compound semiconductor such as GaAs, the presence of two types of atoms opens the possibility of having a Ga atom in place of an As atom. This type of defect is called a Ga antisite defect. There could also be complexes of this defect with other native or extrinsic point defects such as a antisite-vacancy complex. Point defects are electrically active defects as they can be in more than one charge state as a donor or acceptor defect. As a donor, the defect is neutral when occupied by the electron and is positive after donating an electron. In the same way, the acceptor is negative when occupied by electron and becomes neutral when empty. Thus, the point defects can be classified as shallow level defects with their energy levels close to the CB or VB, or deep level defects with their energy levels away from the CB or VB edges. An understanding of point defect physics can be gained by combining theory and experiment [1]. Just like point defects, there are line defects such as dislocations, surface defects such as grain boundaries and volume defects such as precipitates and clusters. All these crystallographic defects in a semiconductor sample produce energy levels in the band gap and affect the device characteristics through generation and recombination currents. The trap close to the intrinsic Fermi level is the most effective generation-recombination centre. In a p^+n-junction and a metal-semiconductor Schottky diode, generation current via defects dominate in the reverse bias and the recombination current via defects dominate the diode current-voltage characteristics in forward bias. Defects can be good for the diode as a switch because the generation-recombination current reduces the carrier lifetime and thus turns on and off the switch faster. Defects can be bad for the diode as a detector, because the generation-recombination current increases the reverse biased leakage current in the diode and the change in current due to radiation is reduced.

II. Theory

There are many spectroscopic techniques to characterize bulk defects in the semiconductors such as Photoluminescence (PL), Deep Level Transient Spectroscopy (DLTS), Electrically Detected Magnetic Resonance (EDMR), and Electron Paramagnetic Resonance (EPR) [1]. Metal/semiconductor barrier height can be determined by current-voltage and/or capacitance-voltage method [2]. The semiconductor/insulator interface can be characterized for interface trap density determination using MIS device in depletion by techniques such as the Terman method, Conductance technique, Low frequency C-V technique, High frequency C-V technique, Combined High-Low frequency C-V technique and others [3]. Semiconductor/insulator band offsets can be determined using photoelectron spectroscopic techniques such as X-Ray Photoelectron Spectroscopy (XPS), Ultra-Violet Photoelectron Spectroscopy-Inverse Photoelectron Spectroscopy (UPS-IPES) and others. Elemental analysis technique such as Electron Energy Loss Spectroscopy (EELS) is used to characterize

elements present in a material or semiconductor/insulator interface, particularly for low atomic number elements such as carbon, oxygen, nitrogen, silicon and others.

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III. Results and Discussion

Two observations are brought to light in this short communication. First, the bulk defects in a semiconductor such as 4H-SiC show up as interface states in a metal-oxide-semiconductor (MOS) device fabricated on it. The terminated epitaxial surface is oxidised to form the MOS device after metallization of the oxidised surface. The semiconductor/oxide interface is further characterised by techniques such as the high-low capacitance-voltage measurement technique, to determine the interface trap density versus semiconductor bandgap energy plot. The plot clearly shows these defects at the right energy levels in the 4H-SiC bandgap. Second, the near-interface traps in the oxide of the 4H-SiC MOS device near the conduction band (CB) become neutral upon NO annealing, causing the fixed oxide charge density in the n-type 4H-SiC MOS device to become negligible. The EPR and EDMR signal from the unpaired electron also become very small after NO annealing because it cannot detect neutral traps. The neutral trap density is however determined by a new method of observing the low field leakage current in an n-type MOS device in accumulation.

Many studies on bulk defects in 4H-SiC have been performed. The author has selected three of them to enlighten the first observation [4-6]. Defects studies by Mannan et al. [4, 5] points to three bulk defects in 4H-SiC at E_c-0.67 eV named as $Z_{1/2}$, at E_c-1.04 eV named as EH_5, and at E_c-1.60 eV named as $EH_{6/7}$, all three having high density in the range of 10^{12} to $10^{13}/cm^3$. Defects study by Negoro et al. [6] indicates the energy position of two main stable defects, $Z_{1/2}$ and $EH_{6/7}$ at E_c-0.59 eV and E_c-1.66 eV, with the epitaxial layer grown at low C/Si ratio of less than 0.7. Their densities decrease by one order after very high temperature annealing at 1700^oC or 1800^oC. The energy position of the defects $Z_{1/2}$ and EH_5 in 4H-SiC are at about E_v + 2.6 eV and E_v + 2.2 eV given that the experimental bandgap of 4H-SiC is 3.23 eV. These defects, because of their high density are visible as humps in the interface trap density (D_{it}) versus bandgap energy plot in Fig.2 of the study by Williams et al. on the wet-oxidised/wet re-oxidised 4H-SiC MOS devices [7]. The near-interface traps in the 4H-SiC MOS device are different from the above bulk traps and are known to be pinned at 2.9 eV from the 4H-, 6H- or 15R-SiC valence band (VB) [8]. Since the 2.9 eV position from the 4H-SiC VB is 5.83 eV from the SiO_2 VB, therefore these acceptor traps are indicative of being the E' centres in the SiO_2 which have this energy location in the SiO_2. $Z_{1/2}$ and $EH_{6/7}$ are the two thermally most stable traps [4] which act as recombination centres and reduce the carrier generation lifetime in 4H-SiC in the range of 1ns to 1µsec [9]. Out of these two defects, $Z_{1/2}$ is believed to be the dominant carrier lifetime reducing defect because the intrinsic Fermi level is at E_c-0.97 eV [10] and this trap is the closest to the intrinsic Fermi level thus acting as the most efficient recombination centre [11, 12]. The structure of all the bulk traps is not clear yet but is believed to be due to displacement of carbon atom in the SiC lattice [4, 5].

The second observation is considered next. It has been analysed and explained before by the author (an attempt was made) that dry or wet oxidation with or without wet re-oxidation at 950^oC for 3 hrs, results in the SiO_2/4H-SiC interface having Si-C-O-O like bonds which form the E' centres with an associated positive charge trap that manifests itself as fixed oxide charge in the p-type device. The density has been shown to be 12 x $10^{11}/cm^2$ and there are 22 electrons associated with C-O-O bonds based on the atomic numbers of carbon and oxygen. The NO annealing for 2 hrs at 1150^oC or 1175^oC is thought to replace one O with one N and form C-O-N bonds giving the total number of electrons as 21. This means that there is one less electron as compared to C-O-O and so the positive charge density doubles to 23.5 x $10^{11}/cm^2$ in the p-type device. The corresponding E' centre in the n-type device which has another unpaired electron before NO annealing becomes neutral due to replacement of one O with one N that adds a positive charge [13]. There is new evidence from a study in Japan to suggest that after NO annealing Si_3N_4 is formed at the interface that has about 2 x $10^{14}/ cm^2$ nitrogen atom density which for a 2 nm interface becomes about $10^{21}/cm^3$ volume density. Silicon nitride based K^0 defect centres have been observed which are characteristic of Silicon nitride [14]. Earlier in 2017, a workshop at the University of Maryland, USA, Taillon and co-researchers also showed silicon nitride like bonding at the SiO_2/SiC interface after NO annealing through EELS measurements. A comparative study of defects in silicon nitride and SiO_2 suggests that the K^0 centre in silicon nitride is similar to the E' centre in SiO_2 with the energy level predicted to be near midgap of the nitride. Two K^0 defects can produce a set of positive and negative centres [15]. Since N-N-N bonds in Si-N-N-N also has 21 electrons based on the atomic number of Nitrogen, therefore the fixed oxide charge density in the p-type device will also be 23.5 x $10^{11}/cm^2$ and in the n-type device with an additional unpaired electron will be neutral and have negligible fixed oxide charge density as observed and explained earlier [13]. The unpaired electron will make the number of electrons even to 22 causing neutral K^0 centre in the n-type device [13]. Essentially, the entire analysis made earlier [13] with consideration of Si-C-O-N formation after NO annealing remains the same for consideration of Si-N-N-N formation because the number of electrons in C-O-N and N-N-N are the same at 21 based on the atomic number of carbon, oxygen and nitrogen. Further, the EDMR and EPR studies have shown that after NO annealing, the

EPR or EDMR signal becomes very small because they cannot detect neutral molecule unless there is an unpaired electron. This means that the small signal present is due to some non-stoichiometric silicon nitride as SiN_x or it could be due to some SiON present [14, 16-17]. However, a new method of finding the near-interface trap density in the n-type MOS device in accumulation is applied, that is based on the observation of low-field leakage current and compared with the displacement current in the oxide at a ramp rate of 0.1 V/s to determine the near-interface trap capacitance from which the near-interface trap density is obtained [18]. Two articles written about the correlation of fixed charge density and border trap density between Si<111>/SiO_2 interface and 4H-SiC(0001)Si/SiO_2 interface have the analysis applicable to Si-N-N-N formation after NO annealing for the same oxidizing ambient with similar processing temperatures [19-20]. Another evidence of the silicon nitride formation at the SiO_2/SiC interface is that the humps appearing due to bulk defects after wet re-oxidation at 950^{o}C for 3 hrs disappear after NO annealing as shown in Fig.2 and Fig.3 of the study by Williams et al. [7]. It is to be kept in mind that nitride defect formation at the SiO_2/SiC interface after NO annealing is another possible outcome of NO annealing. The characterization of the interface is an ongoing research problem. In the end, the author in summary finds that Nitrogen at the SiO_2/SiC interface passivates P_b and P_{bC} traps of one type and introduces near-interface or border traps of another type. Since the overall field-effect mobility is increased after N at the interface when compared to mobility in the as-oxidised MOSFET, therefore N at the interface is necessary. The charge correlation studies by the author shows that mobility cannot be increased any further in 4H-SiC power MOSFET due to the minimum high density of border traps at the interface of low 10^{12}/cm^{2}eV order.

IV. Conclusions

Bulk defects in 4H-SiC semiconductor material epitaxial layer named as $Z_{1/2}$ and EH_5 manifest themselves as interface states in the MOS device fabricated by wet oxidizing the semiconductor followed by metallization, particularly when their volume densities are high or the order of 10^{12} to 10^{13}/cm^3 in the semiconductor material. After NO annealing, they disappear due to possible silicon nitride formation at the SiO_2/4H-SiC interface. Fixed charge and border trap density determined with consideration of formation of Si-C-O-N bonds in the oxide and at the oxide/SiC interface does not change with consideration of formation of Si-N-N-N bonds because the number of electrons in the C-O-N and N-N-N bonds remain the same at 21, given the atomic number of carbon, oxygen and nitrogen as 6, 8, and 7. The analysis of the correlation of charges in 4H-SiC (0001) MOS device and the Si<111> MOS device also remains unaffected. Nitrogen at the SiO_2/4H-SiC interface passivates the P_b and P_{bC} traps of one type but creates border traps of another type limiting the surface field-effect mobility in the 4H-SiC n-channel power MOSFET.

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