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Decoupling capacitors optimization in a Power Distribution Network

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Abstract:*The design of a Power Distribution Network (PDN) for high performance integrated circuits (IC) has been demanding ever more strict requirements, due to the increased information transmission speed. This article proposes a methodology that allows through a genetic algorithm optimization technique to minimize the number of decoupling capacitors in a PDN in order to satisfy a target impedance (Ztarget) in a frequency range. The work shows the possibility to find a solution that meets the target impedance design criteria Ztarget of a specific IC with a time of around 30 to 40 seconds. The results show sufficient reliability for the starting point of the minimum number of decoupling capacitors in pre-layout of a PDN.*

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I. Introduction

Nowadays, high-speed digital designs have surpassed the barrier of 10 Gb / s of real information exchange (bits switching). Thus, designers must provide special care with a Signal Integrity (SI) and Power Integrity (PI) system. Increased system speed requires more ingenuity design, especially in relation to the strictest requirements of strength and power that are provided for high-performance devices. The PI and SI are factors that guarantee the signal transmission between the transmitter and receiver.

The PI problems are associated with the impedance of the power distribution network (PDN), which comprises the entire path from the output of the power supply to the integrated circuit (IC). Some requirements of the PDN must be guaranteed so that the devices connected to it work correctly. One of these requirements is that the PDN must work as a source of low impedance across the entire bandwidth (from DC up to a certain frequency). This impedance must be lower than the requested maximum impedance for the PDN, called target impedance (Z_{target}). Thus, given the transient current consumption of the device, the impedance level must ensure that the supply voltage of the IC is kept in an acceptable range of ripple. This article proposes a methodology based on genetic algorithms to minimize the number of capacitors in a PDN, in order to meet a target impedance within a certain frequency band.

The PDN and the Decoupling Capacitors: The impedance characterization of the PDN can be represented by three regions, as shown in Fig. 1. The low frequency range is comprised between the level of zero to a few hundred kilo-hertz. In this frequency range the impedance is defined mainly by the return characteristics of the energy converter. The average frequency range reaches up to a few hundred mega-hertz and the impedance is associated with the inductance and capacitance of the PCB circuit (decoupling capacitors, ferrites, resistors) in this band of frequency. The high frequency range contemplates the impedance of the load elements (encapsulation, pathways) and part of the impedance of the PCB.

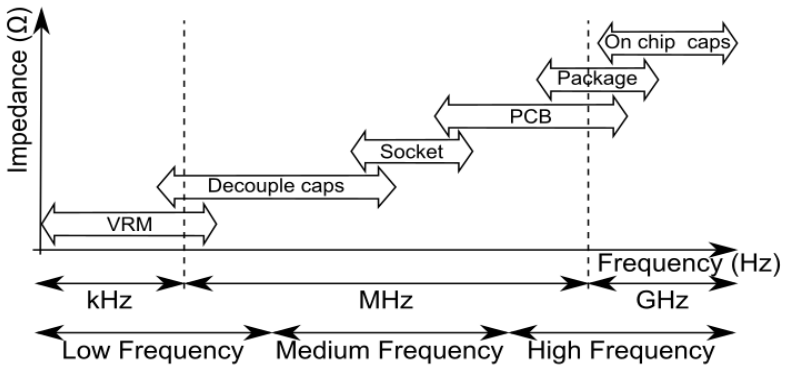

Fig. 1 Ranges of performance of each part that composes the PDN considering impedances in the frequencies.

Fizesan and Pitica[1] provided a simulation of a four-layer PCB with power and feedback plans to evaluate the effectiveness and importance of decoupling capacitors. A powerful simulation program allows the user to identify problems in the PDN even before the layout and thus check if the decoupling strategy is working.

Tripathim et al. [2] presented a method known as simulated annealing to reduce the noise of the power supply in a PDN. The method is a metaheuristic solution to approach global optimization in a large search space for an optimization problem. The cumulative PDN impedance is reduced by using a smaller number of decoupling capacitors compared to the intuitive placement of decoupling capacitors.

Piersantiet al. [3] used an algorithm to optimize the placement of decoupling capacitors in a Multichip PDN. The cost function is based on the evaluation of the impedance of the PDN and its comparison with a predefined mask. The work demonstrates that the Nature Inspired Algorithm (NIA) can be used for the placement of capacitance considering the geometric constraints of the PDN.

Koo et al. [4] presented a fast capacitor assignment algorithm capable of minimizing the number of decoupling capacitors in a PDN. The work allows finding, with a semi-arbitrary manner, a decoupling solution with a minimal number of components that meets the predefined target impedance. The solution takes a time interval that can go from a few seconds to an hour for a given PDN, depending on its complexity.

Different from these related works, this article presents a methodology that provides a minimum quantity of decoupling capacitors to be used in a PDN pre-layout stage. The minimum quantity of decoupling capacitors is provided in a few seconds indifferent of the PDN complexity. It is relevant because only the voltage and transient current demanded by the IC is required.

II. Material And Methods

The design of a PDN must be performed to meet the impedance threshold in a given frequency range. In addition, the PDN project must take into account other aspects, such as the footprint on the PCB and the cost of its components. Fig. 2 shows methodology proposed to optimize the number of capacitors used in the PDN design.

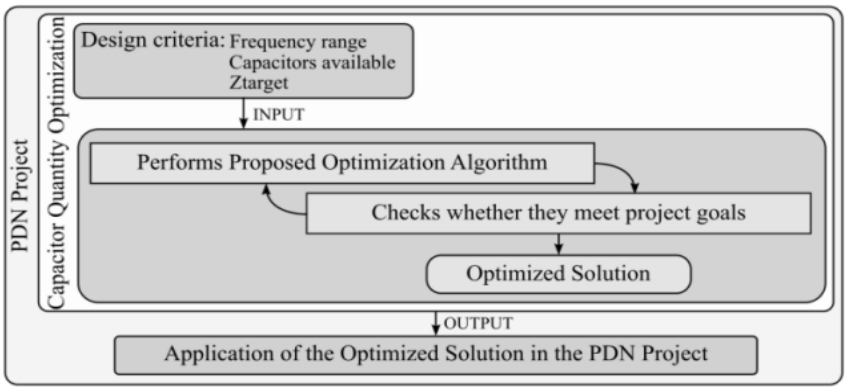

Fig. 2 Methodology to design the PDN decoupling capacitors.

Thus, this methodology allows to evaluate and size the capacitors to meet the impedance required by the IC and also to minimize the number of capacitors to be used. This brings benefits during the design stage. One of these benefits is that the designer has a starting point for the number of decoupling capacitors to be used in the PDN, because many IC manufacturers do not provide as many or which capacitors must be used. Another benefit is the reduction of the number of decoupling capacitors, avoiding oversizing and thus reducing the layout space and manufacturing cost of the product. This work was developed using a problem solving toolbox, which is based on the Genetic Algorithm (GA) solution method, available in MatLab® software.

Optimization of Capacitor Quantity by Genetic Algorithm:

The objective of the PDN project is maintain its impedance below a certain limit in order to reduce the number of capacitors. So, an optimization algorithm for capacitor allocation was elaborated. The GA optimization method was used to solve the problem. This method of optimization is based on the evolutionary biology of living beings to solve problems that have the characteristic of being non-linear.

In the evaluation of the proposed method, 14 different capacitors values were chosen to represent the range of available capacitors for the PDN project. The capacitors used in the study are manufactured by SAMSUNG® and belong to the family of multi-layer ceramic capacitors CL05A. The values of each capacitor used are C1=1nF, C2=10nF, C3=22nF, C4=47nF, C5=100nF, C6=220nF, C7=470nF, C8=1µF, C9=2,2µF, C10=4,7µF, C11=10µF, C12=22µF, C13=47µF, C14=100µF. To check the behaviour of the impedance was

downloaded the data containing the Z parameters of each capacitor. The data is available on the manufacturer's site (http://weblib.samsungsem.com/mlcc/mlcc-ec.do). All these data were imported into MatLab® software, which was used to determine the resulting impedance of the PDN project.

The PDN for a specific IC must have an impedance of less than 0.533 mΩ in a frequency range that lies between 300 kHz and 100 MHz. This design requirement becomes a constraint for the resolution of the optimization problem. Therefore, the problem to be solved is represented by equations (1) and (2), where Z_{Total} is the maximum impedance resulting from the association of the capacitors in the specified frequency range and Z_{Target} is the maximum impedance that the PDN must have in the specified frequency range.

$$MinL(x) = \sum Capacitors\ in\ the\ PDN \quad (1)$$

Subjected to

$$Z_{Total} \leq Z_{Target} \quad (2)$$

The problem was treated through the perspective of integer optimization because of the impossibility to allocate a fraction of capacitor to the PDN Therefore, the problem was structured and the objective function was defined, considering the appropriate restrictions established for the problem in question. After that the parameters of the genetic algorithm were modelled in order to obtain the best solution to the problem. During the analysis, the algorithm obtained a good performance when using a population of 60 individuals and mutation rate of 4%.

III. Result

In order to evaluate the performance of the GA, an analysis was performed to verify the behaviour of the population of individuals throughout the generations. The algorithm was executed according to the previous description, and for each generation was identified the worst and best individual corresponding to the respective objective function of the problem. It was calculated the mean of the generation too. These values allowed to verify the behaviour of the genetic algorithm. Fig. 3 shows the graph containing the values of the worst and best individual and the average capacitors used in the solution set (population) over the generations required for the GA to determine the final solution to the problem.

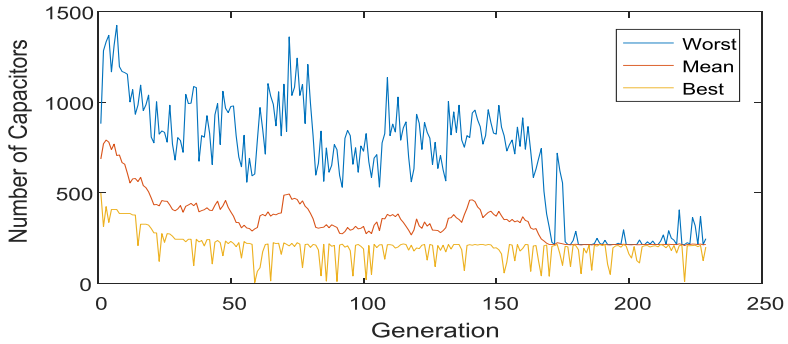

Fig. 3 Worst and best individual and the average capacitors used in the solution set (population) over the generations.

Fig. 3 shows that the first generations have a high variation along and a high average. Throughout the generations the average begins to decrease until, after the 180th generation, the population converges to the point corresponding to the solution to the problem. The population remains for many generations with few variations, indicating that the solution found corresponds to the global minimum solution of the problem. The variations around the mean in these generations are caused by the mutation of the individuals present in the population. Often is found a solution that has a quantity of capacitors much smaller than the final solution. However, these values do not correspond to a valid solution because the resulting impedance is higher than the Z_{Target} .

Fig. 4 shows the graph containing the best solution over the generations, which meets all constraints. Initially there was a large drop in the number of capacitors. From the 130th generation the best solution to the problem is found. The comparison of graphs in Fig. 3 and Fig. 4 shows that the average of the individuals of the population converges precisely to the value corresponding to the best solution for the problem.

The result found by the proposed methodology has a total of 215 capacitors. The quantity of each capacitor according to the answer given by the methodology is C1=1, C2=54, C3=8, C4=5, C5=1, C6=2, C7=0, C8=4, C9=10, C10=39, C11=18, C12=71, C13=2, C14=0.

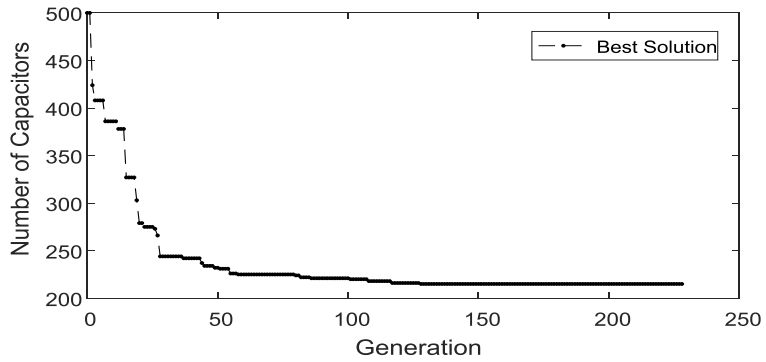

Fig. 4 Best solution over the generations.

Fig. 5 demonstrates the final response impedance found by the algorithm. The figure shows the individual impedance of each capacitor available and the Z_{Target} impedance in the respective desired frequency range. The response obtained meets the requirements and objectives. The resulting impedance obtained in the 300 kHz and 100 MHz range was lower than the maximum impedance determined in the design. The algorithm takes a time between 30 and 40 seconds of simulation to obtain a result for the problem. The algorithm runs on a computer with a 2.4 GHz 2-core Pentium Core i7® processor and 8 GB of RAM.

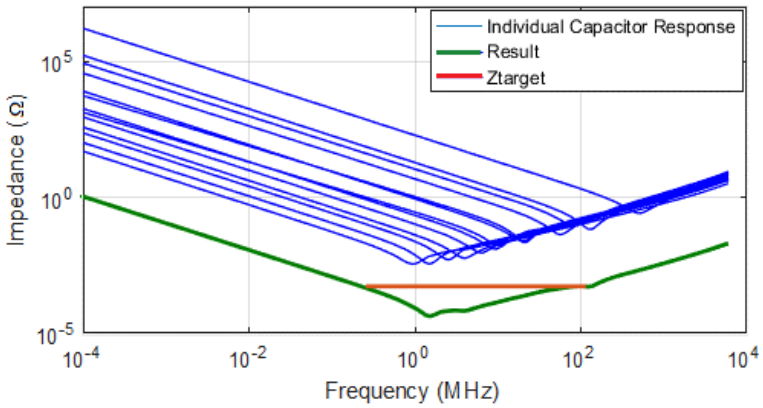

Fig. 5 Frequency response of each capacitor and the association of the resulting capacitors the GA response

IV. Conclusion

The dimensioning of decoupling capacitances in a PDN can become complex in high performance electronic designs. This work presented a methodology that provides a starting point for scaling the minimum quantity of decoupling capacitors in a PDN for high performance ICs. The methodology uses only the electrical requirements of voltage, power noise, transient current of the IC and optimization by Genetic Algorithm to determine the solution. The result prevents oversizing of the capacitance in the PDN, reduces the layout space and the manufacturing cost of the product. The methodology allowed to meet the target impedance Z_{Target} design criteria of a specific IC in a very low time, around 30 to 40 seconds, with sufficient reliability for the starting point in the minimum number of capacitors of decoupling of the PDN.

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