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Static and Dynamic Characterization of GaN HEMT Power Semiconductor Devices

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Abstract: *Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs) have demonstrated their capabilities to be an excellent candidate for high voltage, high temperature, high-power, and high-frequency power electronic applications.*
In this paper, a simplified LTspice model of the GaN HEMT device is proposed. The current GaN HEMT from GaN System Inc. is evaluated including static and dynamic characteristics for different gate resistances, different load currents and at various temperatures.In addition, a simple mathematical model is derived to estimate the optimal external gate resistance required to obtain lower feasible switching losses, while ensuring that the oscillation in the gate-source voltage is reduced sufficiently. The results showed that the model is effectively simulating the static and dynamic behavior of GaN device. Furthermore, the actual power losses of this device can be easily calculated.
Keywords: *GaN HEMT, LTspice model, Optimal gate resistance, Power loss, Static and dynamic characterization.*

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I. Introduction

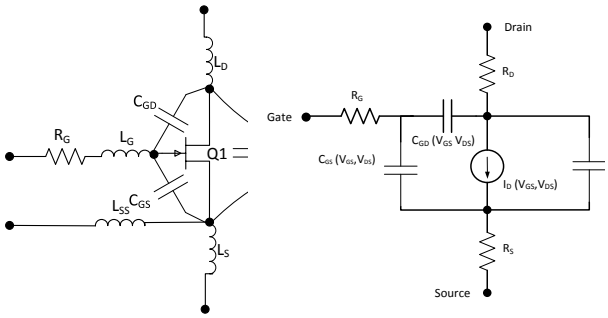
For the last few decades, silicon-based power switches were considered to be the primary solutionfor power electronics applications. However, Si-based devices are approaching some of theirinherent material limits, including those related to operating temperature, switching frequency, andblocking voltage. Recently, wide bandgap (WBG) semiconductors such as gallium nitride (GaN) and silicon carbide (SiC) have attracted the focus of a great deal of research and development[1, 2].GaN devices have approximately three times as large a bandgap (3.4 eV) as silicon-based (Si) devices (1.12 eV). Large bandgaps result in much lower leakage currents and higher operating temperatures. Furthermore, the higher breakdown field of the WBG semiconductors allows for a higher doping concentration with thinner blocking layers than those achievable with Si devices. As a consequence, the drift region may be designed to be much thinner, allowing a lower on-state resistance for a given breakdown voltage. Additionally, WBG devices are superior in terms of thermal conductivity, which in turn improves the size of the cooling system[3]. All of these features make WBG devices attractive for use in a high-frequency and high-power application[4–7].Further, the fast switching, though, is associated with oscillation phenomena that occur during the dynamic switching process. The switching is more sensitive to the circuit parasitic elements, such as inductance and capacitance in gate and power loops. The main drawback of GaN HEMTs is that they are mostly available in lower current ratings. Therefore, in many cases, GaN HEMTs still need to be paralleled to increase the current capability. Current sharing among parallel devices has always been an important issue, since an unequal loss- and temperature distribution may occur which could even exceed the safe operation area (SOA) of devices [8].

Therefore, an accurate model is needed to optimize and predict the static and dynamic switching behavior of the GaN HEMT devices and hence to determine their limitation factors, e.g. thermal and switching frequency limits, at different operating conditions.The physics-based and analytical models of GaN are discussed in[9–14]. In most cases, they require large computational effort and are difficult to use for circuit simulation. For simplicity, assumptions are made to obtain results at a fast simulation speed at the expense of accuracy. Therefore, the trade-off between model accuracy and computational effort is an important factor when special effects occurring in GaN are included.

In this paper, GaNPX packaged, 650 V, 60 A GaN HEMT developed by GaN System Inc. is simulated and investigated. The static characteristics, such as on-state resistance (*Ron*) in the first and third quadrant are derived. In addition, the temperature dependence of the threshold voltage and the transconductance are investigated. In order to evaluate the dynamic switching of the devices, double pulse tests (DPT) with inductive load are conducted, and the effects of different gate resistances, varying the load current and the temperature operating points are analyzed.

Static Characterization

The simulation model is built by LTSpice-IV, where the model of GS66516B is applied in the simulation. The equivalent gate circuit of GaN HEMT is shown in Fig. 1.The key parameters of this device are presented in Table-I. The forward output characteristics of the 650 V/ 60 A GaN HEMT are simulated with different gate-source voltages (V_{gs}) of up to 6 V and over wide operating case temperatures (T_c) of up to 150 °C. The measured I-V characteristics are depicted in Fig. 2.In order to avoid any self-heating, the turn-on pulse is limited < 4 µs. As shown, the slope of the I-V characteristics decreases with increasing temperature, indicating the decreasing channel conductivity. This is due to the lower channel carrier mobility under higher operating temperature.



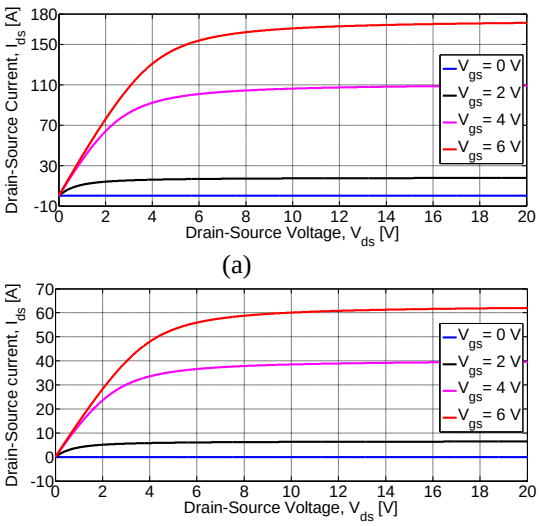
(a) (b)

Fig. 1: Equivalent circuit of (a) GaN HEMT GS66516B and (b) GaN transistor model in [15].

Table-I: DEVICE UNDER TEST (DUT) SPECIFICATIONS

Drain-Source voltage (V_{ds})	650 V
Gate-Source Voltage (V_{gs})	-10 V to + 7 V
Internal Gate Resistance ($R_{gInternal}$)	340 mΩ
Drain Current (I_{ds}) at 25 °C /100 °C	60 A / 47 A
On-Sate Resistance (R_{on}) at 25°C/150°C	25 mΩ / 65 mΩ

Further, *Ron* is then calculated based on the slope of the output characteristics. Fig. 3gives the temperature-dependency of *Ron* applying the rated gate-source voltage of 6 V. As shown, at I_{ds}= 40 A, the simulated on-resistance of GaN HEMT increases from 26mΩ to 78mΩ, as device junction temperature rises from 25 °C to 150 °C. This shows that this device has a very low *Ron*which makes it suitable for high power applications. The positive temperature coefficient (PTC) is expected for self-balancing. This feature is potentially beneficial to the short circuit ruggedness by limiting the saturation current and improving the device paralleling behavior.



(a)

(b)

Fig. 2: Temperature-dependent output characteristics of DUT at (a) T_c= 25 °C and (b) T_c = 150 °C.

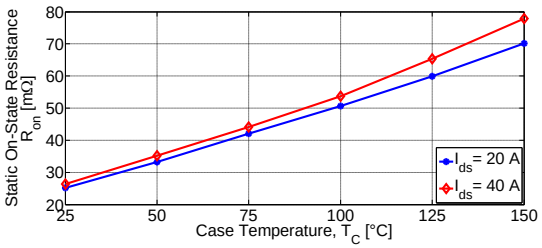


Fig. **3**Temperature-dependent on-state resistance at I_{ds}= 20 A and 40 A.

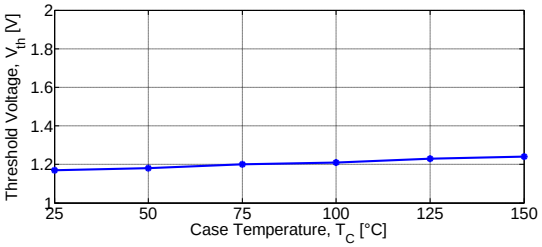


Fig.4: Threshold voltage versus case temperature.

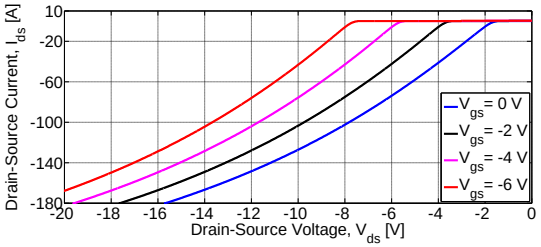
Further, the threshold voltage (V_{th}) of GaN HEMTs at different temperatures is simulated as shown in Fig.4. In this work, the threshold voltage is defined as the minimum voltage required to produce 5 mA drain-source current when the drain and gate terminals are shorted. Different from SiC MOSFET [8], the threshold voltage of GaN HEMTs is almost constant as a function of junction temperature. A lower V_{th} leads to a false turn-on, also generates a higher switching current which means more losses. Therefore, to prevent any false turn-on switching, the GaN devices are recommended to be driven by a negative gate-source voltage.

On the other hand, GaN transistors can also conduct in the reverse direction when the drain-source voltage is higher than the biasing voltage by at least the threshold voltage. The reverse characteristic of GaN is similar to that of a diode, but it is greatly affected by the gate-source voltage. It worth to mention that the GaN HEMT doesn't have a body diode anti-parallel to the device. This results no reverse recovery losses which is a great advantage over SiC MOSFETs.

Fig.5 depicts the reverse static characteristics of DUT applying different biasing voltage. As shown, if a negative biasing voltage is applied, the forward drop will increase proportionately. For example, using 0 V biasing, V_{sd} is reduced by more than 77% compared with the case of using -6 V gate-source voltage.

Furthermore, the transfer characteristic is evaluated applying V_{ds} = 10 V. The results are shown in Fig. 6. In addition, the average transconductance (g_{fs}) as a function of case temperature is shown in Fig. 7, calculating using the average slope of the curves in Fig. 6 between 3 V and 6 V.

As shown, one notable feature of this device is that the transconductance drops significantly as the junction temperature increases. This feature is potentially beneficial to the switching loss that will be explained in the next section.



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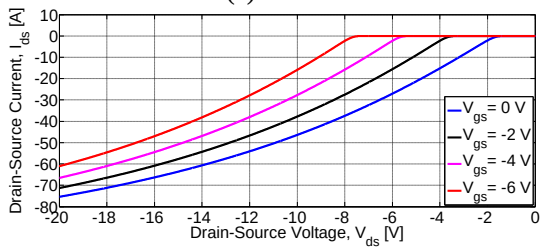


(b)

Fig.5: Static reverse characteristics of DUT at (a) T_c = 25 °C and (b) T_c = 150 °C.

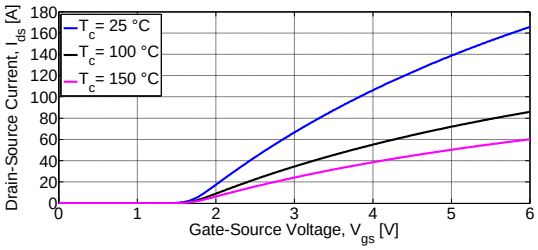


Fig. 6: Transfer characteristic over increasing junction temperature, V_{ds} = 10 V

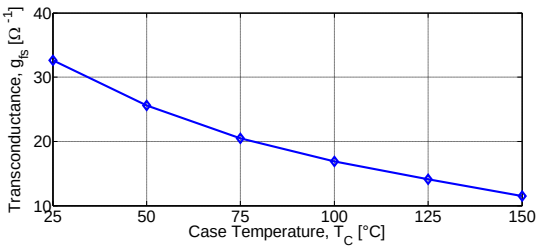
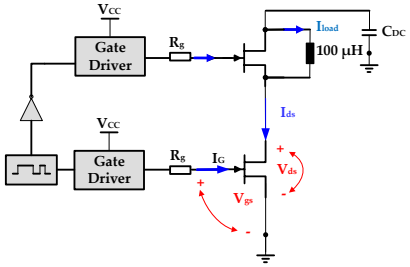


Fig. 7: Transconductance at different case temperatures.

Dynamic Characterization:

GaN devices exhibit fast switching, accompanied by an undesirable current and voltage ringing during the turn-on and –off processes. Thus, to achieve optimal utilization of GaN transistors, it is necessary to fully understand the switching behavior and the dominating factors in both the turn-on and turn–off dynamic processes.

The standard double-pulse tester (DPT) circuit with inductive load is used to evaluate the switching performance of the transistors. The dynamic characterization is done at different DC link voltages (V_{dc}), load currents (I_o), external gate resistances, and temperatures. The schematic of the DPT circuit, as well the typical switching waveforms, are depicted in Fig. 8. The gate-source voltage (V_{gs}), drain-source voltage (V_{ds}), and the drain-source current (I_{ds}) at the end of the first pulse and at the beginning of the second pulse are recorded. This gives the dynamic turn-off and turn-on processes, respectively.



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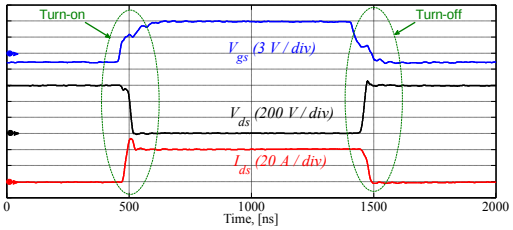


(b)

Fig. 8: DPT circuit: (a) schematic of DPT and (b) typical waveforms.

The switching experiments are conducted up to 400 V varying the load current from 5 A to 60 A. The switching speed is adjusted by using different gate resistances in the range 1 Ω to 40 Ω.

The Effect of Different External Gate Resistance

The impact of the gate resistance on the switching is analyzed in Fig. 9. Fig. 9-a demonstratesthe turn-on switching waveforms, while Fig. 9-b shows turn-off behavior. As shown, if a small gate resistance is used, the fast switching speed generates a high ringing in the gate waveforms which may cause unintentional turn-on or turn-off of the device. Therefore, the external gate resistance should be selected to ensure that the ringing at the gate drive signal is sufficiently damped.

The switching losses are calculated directly from the simulation according to (1) and are plotted in Fig. 10.

(1)

$$E = \int_t v_{ds}(t) i_{ds}(t)\, dt$$

Analyzing Fig. 9 and Fig. 10, it is obvious that with increasing switching speed a significant reduction of power losses can be achieved at the cost of higher ringing, higher current overshoot at turn-on and voltage overshot at turn-off. The evaluation also shows that in order to make full use of the transistor's switching capability, the gate resistance should be further reduced.

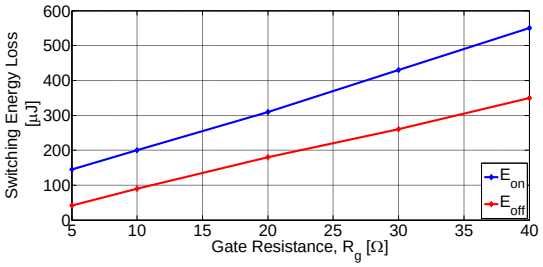
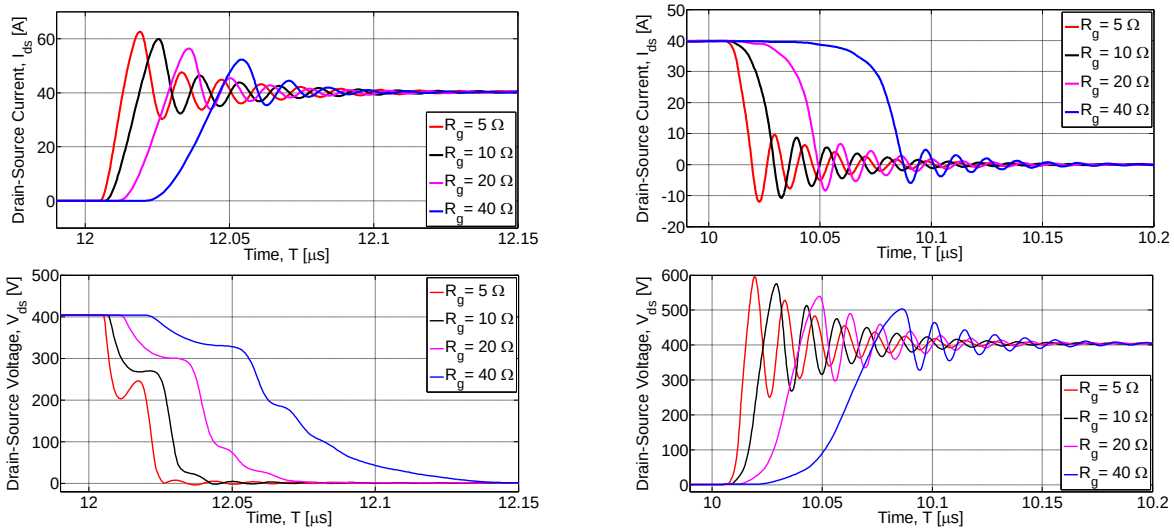


Fig. 10: Switching energy using different gate resistors at 400V, 40A and T_c= 25 °C



(a) (b)

Fig. 9: Switching behavior of GaN device at 400 V, 40 A, with different gate resistors. Time scale 50ns/div.

Optimal Selection of the External Gate Resistance

The fast switching capability of GaN often generates overshoot and switching oscillation. Using a large external gate resistance (R_g) leads to a reduction in the overshoot, but increases switching losses (see Fig. 9). In this, the external gate resistance should be carefully selected to ensure that the gate pulse is sufficiently dampened. In this work, the optimal $R_g$is calculated based on the trade-off between the fast switching time and the gate-source overshoot voltage. The DPT showed in Fig. 11-a is used to derive the analytical expression of the optimal R_g. The optimal $R_g$is derived considering the turn-on process, see Fig. 11-b.

The equivalent circuit of the charging input capacitance (C_{iss}) sub-interval during a turn-on transition is depicted inFig. 11-b. When the gate pulse voltage (V_{pulse}) is applied, the gate current (i_g) charges the gate-source equivalent input capacitance ($C_{iss} = C_{gs} + C_{gd}$). In this case, the circuit equations can be expressed as follows:

(2)

$$V_{Pulse} = (L_G + L_S)\frac{di_g}{dt} + R_G i_g(t) + V_{gs}(t)$$

(3)
$$i_g = C_{iss}\frac{dv_{gs}}{dt}$$

Here,$R_G$includes the internal ($R_{ginternal}$) and external (R_g) gate resistances, ($R_G = R_{ginternal} + R_g$), L_G and L_s are the gate and source parasitic inductances respectively.

To solve these differential equations, the Laplace transformation is applied:

(4)
$$V_{gs}(s) = \frac{1}{s}\frac{V_{Pulse}}{L_{eq} + C_{iss}s^2 + R_G C_{iss}s + 1}$$

Generally, the gate-source voltage behavior is underdamped. Therefore, the characteristic equation has complex conjugate roots.

(5)
$$0 = s^2 + \frac{R_G}{L_{eq}}s + \frac{1}{L_{eq}C_{iss}}$$

According to control theory, the damping ratio (ζ), which represents the transient response, is expressed as follows:

(6)
$$\zeta = \frac{R_G}{2}\sqrt{C_{iss}/L_{eq}}$$

Finally, rearranging(6), the optimal external gate resistance (R_g) can be calculated as the following:

(7)
$$R_g = 2\zeta\sqrt{L_{eq}/C_{iss}} - R_{g\,Internal}$$

According to the datasheet, C_{iss}= 520 pF, $R_{gInternal}$= 340 mΩ and the $L_{eq}\left(=\frac{L_s L_D}{L_s+L_D} + L_G\right)$assumed to be 20 nH, then the optimal R_g is calculated using (7) to be 10.8 Ω. In this work, a 10 Ω is used as anexternal gate resistance.

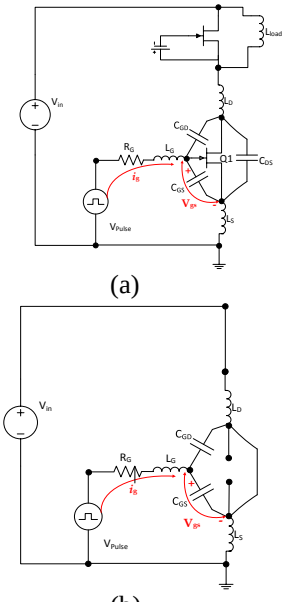
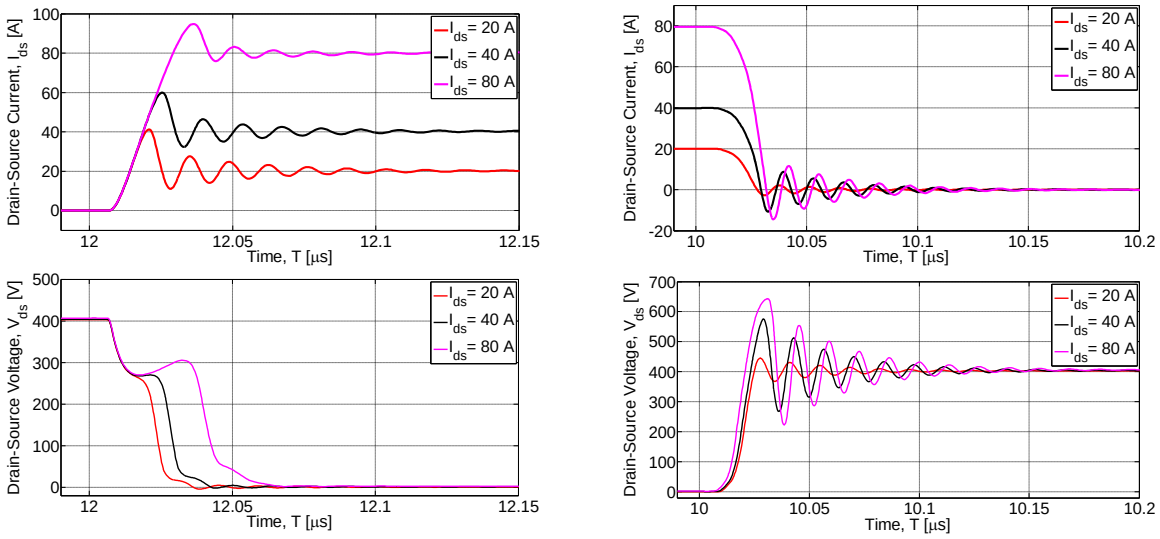


Fig. 11: (a) DPT circuit and b) charging input capacitance during the turn-on process.



(a) (b)

Fig. 12: Switching behavior of GaN device at 400 V, R_g= 10 Ω and different load current. Time scale 50ns/div.

The Effect of DifferentLoad Current

Further, the impact of the load current is analyzed applying a gate resistance of R_g=10 Ω, see Fig. 12. Both, the on and off switching losses increase with the load current, but the turn-off losses do not increase as fast as the turn-on losses because of the reduction in the turn-off time, see Fig. 13. This behavior is due to the fact that a higher drain current leads to a higher plateau voltage ($V_{plateau} = g_{fs}^{-1} I_{ds}$) in the gate signal during turn-off which in turn increases the gate discharge current and hence reduces the turn-off time [3].

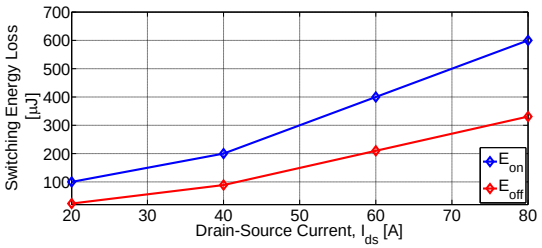


Fig. 13: Switching energy loss under the effect of different load currents at V_{ds}= 400 V, R_g= 10 Ω, and T_c= 25 °C

The Effect of Different Case Temperature

Further, another advantage of GaN devices is high-temperature capability. Fig. 14depicts the simulated waveforms at different case temperatures. Additionally, the switching energy loss as a function of temperature is calculated and plotted in Fig. 15.

As shown, turn-on loss increased with temperature, because of the reduced transconductance (see Fig. 6 and Fig. 7). Hence, the plateau voltage $V_{plateau}$($V_{plateau} = g_{fs}^{-1} I_{ds}$) will increase for given load current, and a lower dv/dt during the turn-on transient is achieved. In contrast, the turn-off loss did not show a strong correlation with temperature.

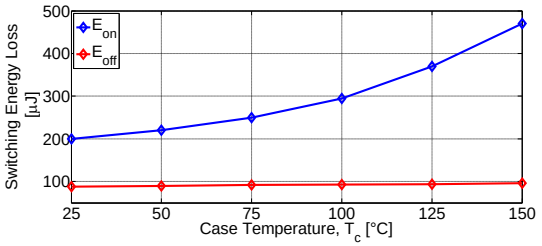


Fig. 15: Switching energy under different case temperatures at V_{ds}= 400 V, R_g= 10 Ω, and I_{ds}= 40A.

II. Conclusion

An extensive static and dynamic characterizations of the up-to-date GaN HEMT developed by GaN System Inc. are evaluated, showing its superior switching performances at different operatingconditions.The simulation approach is used to predict the power loss of GaN devices, which can achieve relatively fast simulation speed and accurate prediction in the LTspice simulation platform. The investigated device has a very low on-resistance and a good switching performance even at high temperatures.The results showed that the model is effectively simulating the static and dynamic behavior of GaN device. Further, the actual power losses of this device can be easily calculated. Further, a simple mathematical model is derived to estimate the optimal external gate resistance. The optimal gate resistance calculated based on the trade-off between the fast switching time and the gate-source overshoot voltage

Based on the derived simulation results, the next step in the work is to derive a full analytical power loss modelwhich identifies the switching waveform subintervals and develops the analytical equations to predictthe loss behavior of semiconductors in the switching process.

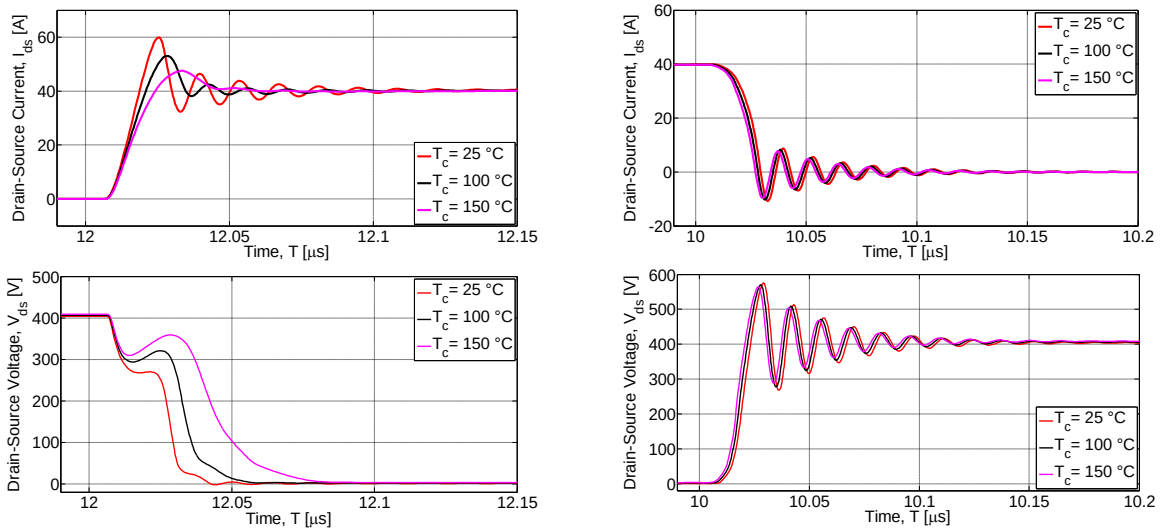


Fig. 14 Switching behavior of GaN device atV_{ds}= 400 V, R_g= 10 Ω, I_{ds}= 40 A and different case temperatures. Time scale 50ns/div.

References

[1]. T. Kimoto and J. A. Cooper, Fundamentals of Silicon Carbide Technology. Singapore: John Wiley & Sons Singapore Pte. Ltd, 2014.

[2]. I. Omura, W. Saito, T. Domon, and K. Tsuda, "Gallium Nitride power HEMT for high switching frequency power electronics," in International Workshop on Physics of Semiconductor Devices, 2007: IWPSD 2007 ; 16-20 Dec. 2007 ; held at the Indian Institute of Technology, Bombay, Mumbai, India, 2007,.

[3]. A. E. Awwad, P. Birgel, and S. Dieckerhoff, "Investigation of 1.2 kV SiC MOSFETs for hard- and soft-switching converters," in 2014 16th European Conference on Power Electronics and Applications, Lappeenranta, Finland, Aug. 2014 - Aug. 2014.

[4]. A. E. Awwad, N. Badawi, and S. Dieckerhoff, "Efficiency analysis of a high frequency PS-ZVS isolated unidirectional full-bridge DC-DC converter based on SiC MOSFETs," in 2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe): 5-9 Sept. 2016, Karlsruhe, 2016, pp. 1–10.

[5]. A. E. Awwad and S. Dieckerhoff, "Operation of planar and trench SiC MOSFETs in a 10kW DC/DC-converter analyzing the impact of the body diode," in ECCE 2017: IEEE Energy Conversion Congress & Expo: Cincinnati, Ohio, October 1-5, Cincinnati, OH, 2017, pp. 917–924.

[6]. A. Stillwell and R. C. N. Pilawa-Podgurski, "A resonant switched-capacitor converter with GaN transistors for series-stacked processors with 99.8% power delivery efficiency," in 2015 IEEE Energy Conversion Congress and Exposition (ECCE): 20-24 Sept. 2015, Montreal, Quebec, Canada, Montreal, QC, Canada, 2015.

[7]. Y. Wang, B. Chen, Y. Hou, Z. Meng, and Y. Yang, "Analysis and Design of a 1MHz Bi-directional Multi-CLLC Resonant DC-DC Converter with GaN Devices," IEEE Trans. Ind. Electron., p. 1, 2019.

[8]. A. Eial Awwad, "On the perspectives of SiC MOSFETs in high-frequency and high-power isolated DC/DC converters," PhD diss., Technische Universität Berlin, 2018.

[9]. B. Syamal et al., "GaN HEMT compact model for circuit simulation," in Proceedings of the 2015 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC): 1-4 June 2015, Singapore, Singapore, Singapore, 2015, pp. 535–538.

[10]. S. Khandelwal, Y. S. Chauhan, and T. A. Fjeldly, "Analytical Modeling of Surface-Potential and Intrinsic Charges in AlGaN/GaN HEMT Devices," IEEE Trans. Electron Devices, vol. 59, no. 10, pp. 2856–2860, 2012.

[11]. D. Cucak et al., "Physical modeling and optimization of a GaN HEMT design with a field plate structure for high frequency application," in IEEE Energy Conversion Congress and Exposition (ECCE) 2014: 14-18 Sept. 2014, Pittsburgh, PA, USA, Pittsburgh, PA, USA, 2014, pp. 2857–2864.

[12]. R. M. Kotecha et al., "An accurate compact model for gallium nitride gate injection transistor for next generation of power electronics design," in 2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL): Stanford University, Stanford, California, USA, July 9-12, 2017, Stanford, CA, USA, 2017, pp. 1–6.
[13]. R. M. Kotecha et al., "A physics-based compact gallium nitride power semiconductor device model for advanced power electronics design," in APEC 2017: Thirty Second Annual IEEE Applied Power Electronics Conference and Exposition: March 26-30, 2017, Tampa, Florida, Tampa, FL, USA, 2017.
[14]. X. Cheng, M. Li, and Y. Wang, "Physics-Based Compact Model for AlGaN/GaN MODFETs With Close-Formed I–V and C–V Characteristics," IEEE Trans. Electron Devices, vol. 56, no. 12, pp. 2881–2887, 2009.
[15]. Appl. Note AN005, "Circuit Simulations Using Device Models," https://epc-co.com/epc/Portals/0/epc/documents/product-training/Circuit_Simulations_Using_Device_Models.pdf.

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