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Performance Evaluations of Interleaved ZCS Boost DC-DC Converters Using Quasi-Resonant Switch Blocks for PV Interface

Khairy Sayed [1], Emad El-Zohri [2], Farid Naguib [3], and Hedra Mahfouz [2]
[1] *Department of Electrical Engineering, Sohag University, Sohag, Egypt*
[2] *Electricity Department, Sohag University, Sohag, Egypt*
[3] *Department of Electrical Engineering, Assiut University, Assiut, Egypt*

Abstract: *This paper presents a novel circuit topology of voltage source multi resonant ZCS interleaved boost DC-DC converter with auxiliary quasi-resonant lossless inductor snubbers and capacitor snubbers. It uses two feedback loops, similar to current mode control, one for slow outer loop and the other for faster inner PWM control loop. To improve the transient response of the 2-cell converter system, a coupled inductors of energy storage inductors is used. This integrated magnetic design structure reduces size and improves the converter performance, both steady-state and transient. The effectiveness of the proposed control scheme is demonstrated through PSIM simulations.*

Keywords: *Photovoltaic system, Interleaved boost converter, Ripple reduction, Coupled inductor.*

I. Introduction

In recent years, there has been a huge increase in the demand for power due to rapid industrial growth, along with an increase in residential loads. As it is necessary to meet these increasing power demands, and since non-renewable energy resources such as fossil fuels are quickly being depleted, alternative, renewable energy resources such as wind energy, solar energy, hydroelectric energy, and bio-mass energy have become major areas of research. Solar energy is one of the most reliable sustainable energy sources and does not require waste management nor pollute the environment. In order to boost the voltage output from PV panels, a boost converter is employed [1-3]. The conventional boost converter, when interfaced with an PV panel, has a high ripple in the voltage and current waveforms on both the input and output sides [4]. When interleaved boost DC-DC converter is used, the ripple is reduced.

Multiple boost converters connected in parallel form the interleaved boost DC-DC converter circuit [5]. Due to variations in environmental conditions, the insolation level varies; hence, the power output from the panel varies. For instance, in shaded conditions as PV power decreases, just a few converters are sufficient to transfer the power whereas under high-light conditions when PV power goes high, additional converters are employed to share the power. When the inductors of the interleaved boost DC-DC converter are mutually coupled, there is a greater reduction in the ripple content than in cases where they are left uncoupled [6]. The current through the converter gets divided among the parallel branches; hence, there is reduction in the stress on the power electronic devices employed as well as a reduction in losses. The only disadvantage is the rise in cost. However, this rise is not significant since lower rating devices may be employed as the current is divided between the parallel branches.

Interleaving technique was also investigated in the early days for the smaller power spacecraft, satellite or avionic applications, and was introduced as unconventional SMPS power stage architecture [7-9]. In such applications, one major concern is the input and output filters rely almost exclusively on tantalum capacitors due to the highest available energy-storage-to-volume ratio at that time. However, the ESR of this filter capacitor causes high level thermal stress from the high switching pulsed current. The input and output filter capacitance is usually determined by the required number of capacitors sufficient to handle the dissipation losses due to the ripple current. Interleaving multiple converters can significantly reduce the switching pulsed current go through the filter capacitor. By properly choosing the channel number with considering the duty cycle, the ripple current may be reduced to zero. Furthermore, interleaving increases the ripple frequency to be n (n is the total channel number) times the individual switching frequency.

The ESR of the tantalum capacitors is inversely proportional to the frequency. Interleaving technique can effectively reduce the filter capacitor size and weight. Another concern of this application is packaging. Due to the thermal management issues, the power loss of non-interleaved converter exceeds the typical dissipation capability of a slot mount circuit packaging card. In addition, the substantial bulky converter usually requires a custom designed mainframe. Interleaving technique can divide the power transfer into multiple modules, lighter and smaller parts can be mounted on the printed circuit card. Each module has limited power loss which the slot mounted cards can conduct away. The third concerns of such application lies in the necessity to redesign virtually the entire power supply in the event that higher power levels are required than initially specified at start

of the design. With the interleaving architecture, increased output power may be supplied by adding additional identical modules. The interleaved converter was designed and developed which can well demonstrate the benefits on input/output filter, packaging, and modularity. Interleaving technique has been studied and investigated in varieties of applications and systems, as reflected in the references [1-16]. Among these studies, the multi-channel interleaved boost converter for PV Interface application has been intensively studied and thoroughly explored [12-16].

This paper describes a two novel circuit topology of voltage source multi resonant ZCS interleaved boost DC-DC converter with auxiliary quasi-resonant lossless inductor snubbers and capacitor snubbers, which additionally includes practical outstanding features. The effectiveness of the proposed converter is demonstrated against line and load variations. PSIM is used to implement the closed loop converter system. The control strategy is discussed. Steady state response analysis and other simulation studies are discussed. Studies were also made to improve the dynamic performance of the converter by incorporating the coupling between three cells of the converter. This coupling inductance M will not only gives a compact magnetic design, but also results in an improved converter performance. Among two possible coupling structures, direct and inverse coupling, the inverse coupling results in better performance. This is because with inverse coupling the common-mode inductance is high. As a result the steady state current ripple is low, and hence the corresponding power loss is also low.

II. Interleaved High Power ZCS Boost DC-DC Converter

2.1 Circuit Configuration

This voltage-fed ZCS PWM DC-DC converter circuit consists of two main switches of reverse conducting IGBTs $Q_1(SW_1/D_1)$ and $Q_2(SW_2/D_2)$. One ZCS-assisted lossless inductor snubbers L_{S1} connected in series with the main switches Q_1 and Q_2, An auxiliary quasi-resonant snubber capacitor C_r in parallel with Q_1 and L_{S1}, DC smoothing capacitor Co output filter is connected in parallel with the DC load that used to smooth out the DC output voltage. The proposed voltage source ZCS-PWM DC-DC converter is configured by a few circuit components and power semiconductor devices as two switches are used as shown in Fig. 1.

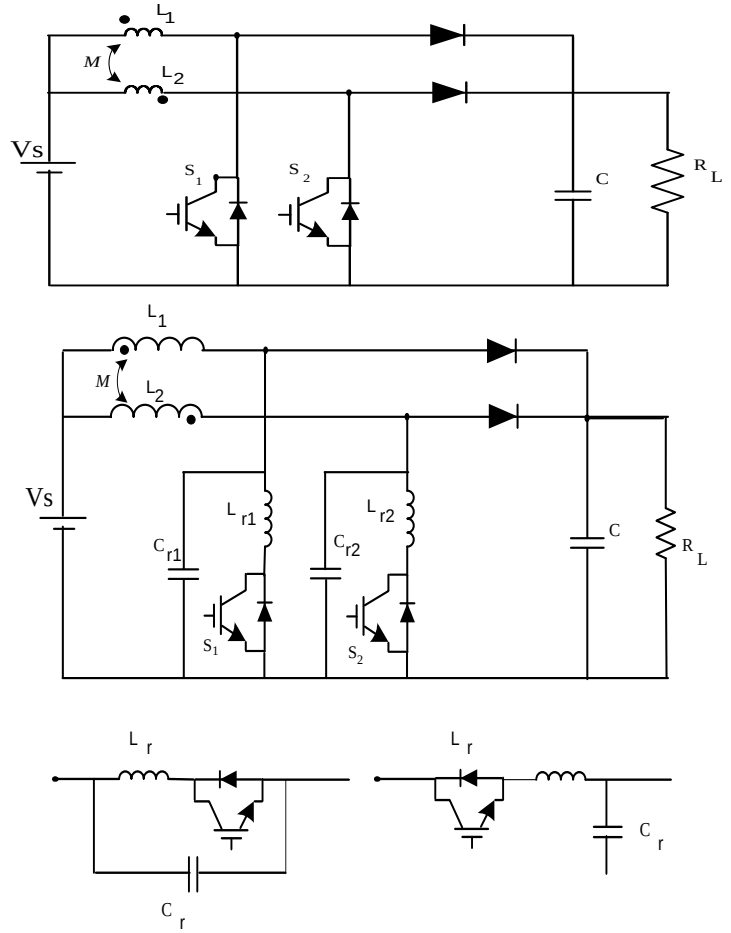

Fig. 1. (a) Hard-switching interleaved Boost DC-DC converter. (b) Soft-switching interleaved Boost DC-DC converter using ZCS PFM cell. (C) ZCS resonant switch cell.

However, the steady-state ripple, both in the load voltage and current, has reduced. This is mainly because of the coupling present between the two channels. a control signal, depending on the error signal, to the PWM generator, while the inner voltage loop comparator generates the PWM sequence to the switching devices. The load voltage is used as the PWM ramp signal and is fed to the PWM generator. Whenever, a change in the supply then it automatically reflects slope of the load voltage. Since the load voltage is used as the PWM ramp, the corresponding duty ratio changes (either increase or decrease) accordingly to maintain the load voltage almost constant. On the similar lines changes in the load affects the load voltage, which in turn changes the pulse width of the PWM output to maintain the load regulation. The indirect coupling is better suited to pairs of inductors; flux cancellation is advantage in this case.

2.2 Gate Pulse Sequence Pattern

The output power of the proposed ZCS DC-DC converter circuit, can be continuously regulated by a constant frequency asymmetrical PWM (duty cycle) control scheme under a condition of zero current soft switching commutation mode. The proposed gate voltage pulse timing PWM sequences for the active power switches Q_1 and Q_2, are shown schematically in Fig. 2. Consider operation of an N -cell parallel converter system. If all of the cells are clocked synchronously, as illustrated in Fig. 2(a) for a two-cell system, then the system behaves exactly as a single large converter. However, it can be shown that if the cells are clocked independently (and hence operate at slightly different frequencies) as shown in Fig. 2(b), the rms input and output current ripples will be reduced by a factor of due to the passive ripple cancellation which occurs among cells. Active ripple cancellation methods can yield even higher performance benefits. The active method of *interleaving*, illustrated in Fig. 2(c), is well known.

Interleaving N parallel (or series) connected converter cells requires that the cells be operated at the same switching frequency but phase displaced with respect to one another by $2\pi / N$ radians. This is conventionally achieved by using a centralized control circuit to supply properly phased clock or synchronization pulses to the individual cells. Comparisons are made between synchronized clocking, independent clocking and interleaved clocking of the converter cells

In the interleaving method, cells are operated at the same switching frequency with their switching waveforms displaced in phase over a switching period. The benefits of this technique are due to harmonic cancellation among the cells, and include low ripple amplitude and high ripple frequency in the aggregate input and output waveforms. For a broad class of topologies, interleaved operation of N cells yields an N-fold increase in fundamental current ripple frequency, and a reduction in peak ripple magnitude by a factor of N or more compared to synchronous operation.

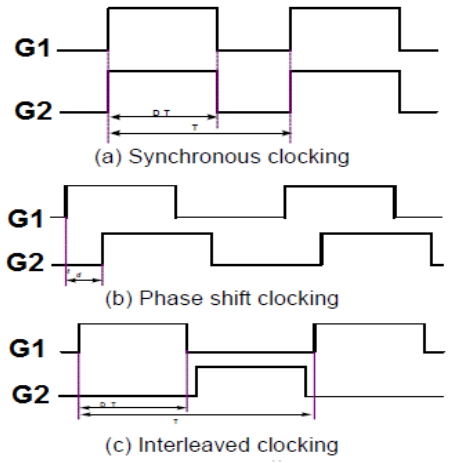

Fig. 2. Gate pulse sequence pattern.

2.3 Principle of Operation

The proposed converter considered as a zero-current-switched quasi-resonant converter (ZCS-QRC). A resonant switch represents a sub circuit consisting of semiconductor switch S1 and resonant elements L_{r1}, and C_{r1}. For a ZC resonant switch, as shown in Fig. 3, inductor *L*, is in series with switch *S*, to achieve zero-current switching. If the ideal switch *S*, is implemented by a unidirectional switch; the resonant switch is confined to operate in a half-wave mode, in the sense that the switch current is permitted to resonate only in the positive half cycle. The switch current can flow bidirectionally and the resonant switch now operates in full-wave mode.

In essence, the resonant *LC* circuit is used to shape the current waveform through switch S. At turn-on, the device voltage Vc_r can be driven into saturation before the current slowly rises. Because of the resonance between *L*, and *C*, current through switch S1 will oscillate, thus, allowing switch S1 to be naturally commutated. For simplicity of analysis, we will consider one cell, as in Fig. 3.

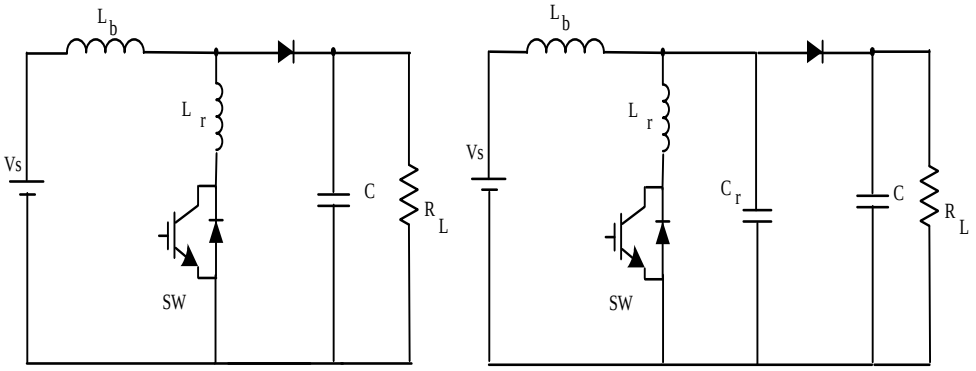

Fig. 3. One unit of ZCS DC-DC converter.

The concept of a resonant switch can be directly applied to a large number of conventional PWM converters. Simply replacing the power switch of a PWM converter with the ZC resonant switch, a new family of ZCS-QRCs can be derived.

A boost quasi-resonant converter is employed to describe the principle of operation. To analyze the steady-state circuit behavior, the following assumptions are made:

- *Lo >> L*
- Output filter L_o - C_o and the load are treated as a constant current sink.
- Semiconductor switches are ideal, i.e., no forward voltage drop in the on-state, no leakage current in the off-state, and no time delay at both turn-on and turn-Off.
- Reactive elements of the resonant tank circuit are ideal.

The following variables are defined:

Characteristics impedance $Z_n = \sqrt{L_r / C_r}$

Resonant angular frequency $\omega_o = 1/\sqrt{L_r C_r}$

Resonant frequency $f_n = \omega_o / 2\pi$.

A switching cycle can be divided into four stages; the operating waveforms are shown in Fig. 4, their equivalent circuits are shown in Fig. 5. Before S1 is turned on, diode D_o carries the output current Io, and resonant capacitor voltage V_{cr} , is clamped at Vo.

Mode 1: At the beginning of a switching cycle, t = *to*, SW is switched on. Input current i_L, rises linearly,

Mode 2: At t2 the capacitor Cr current changes it direction and the capacitor now charging.

Mode 3: The switch is turned of at ZVS, the reverse conducting diode start conducting, the voltage across the resonant capacitor C_r increasing until it reaches Vo at the end of this mode.

Mode 4: At t4, the reverse conducting diode commutates, the output diode start conducting, and the output capacitor start charging.

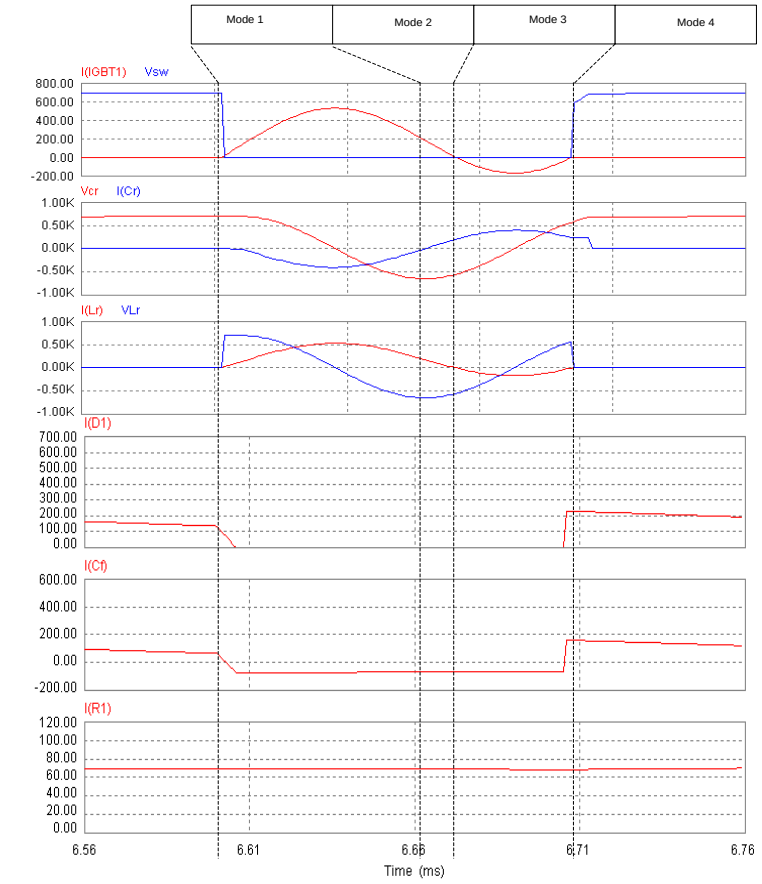

Fig. 4. Operating waveforms.

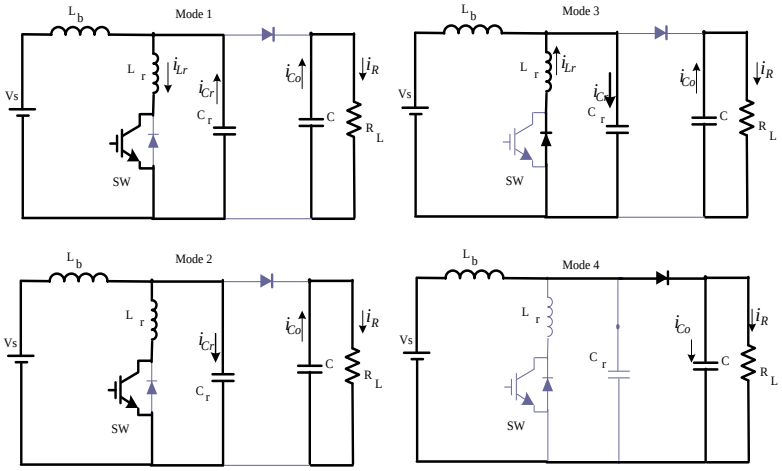

Fig. 5. Boost quasi-resonant operation modes equivalent circuits.

III. Feedback Control Scheme

There are several commercial ICs to drive multiphase converter with 2 to 4 phases. Some of them were designed to work in parallel with others extending the number of phases that can be driven. However, for a very high number of phases this solution is not cost-effective. Moreover, the use of these circuits forces to include a current loop in each phase to equal the DC currents.

Our proposal is to use a digital device such as a FPGA or CPLD, being very easy to generate many shifted driving signals with a very good accuracy. It has been demonstrated previously that with a good design, it is possible to remove the current loop of each phase and being the output voltage the lonely magnitude to control. This duty ratio is controlled by means of a PWM generator, obtained from the controller. The proposed controller based scheme is evaluated through PSIM simulations. The dual loop average current mode control is a better solution. In the dual loop structure, the outer loop is voltage loop, which provide the current reference for

the inner loop. This control requires the sampling of two variables: output voltage, inductor current. Both the inner current loop and the outer voltage loop use a PI controller.

IV. Simulation Results and Discussions

The proposed interleaved boost converter system is shown in Fig. 1. Simulation for prototype converter system was done to study the power regulation and soft-switching ranges of the proposed DC-DC converter. The converter circuit parameters are given in Table 1. In order to maintain the load voltage constant against the line and load disturbances, the converter duty ratio should be changed. Fig. 6, depicts the PSIM model of the proposed DC-DC converter and its feedback control circuit. The output voltage for open loop converter circuit, the output current and the input current with synchronous clocking is shown in Fig. 7.

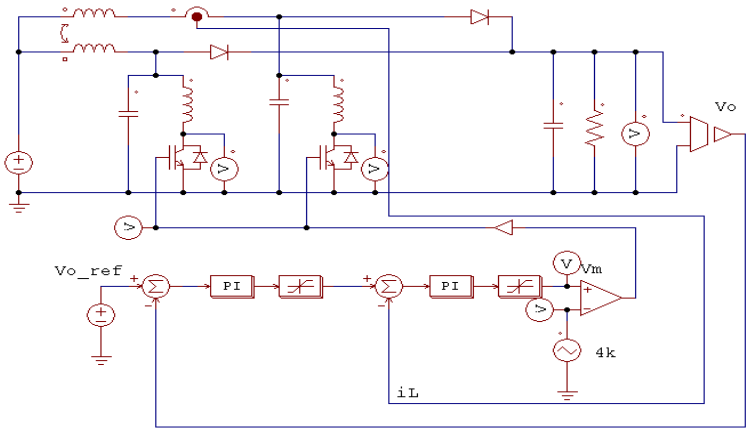

Fig. 6. PSIM model with feedback control.

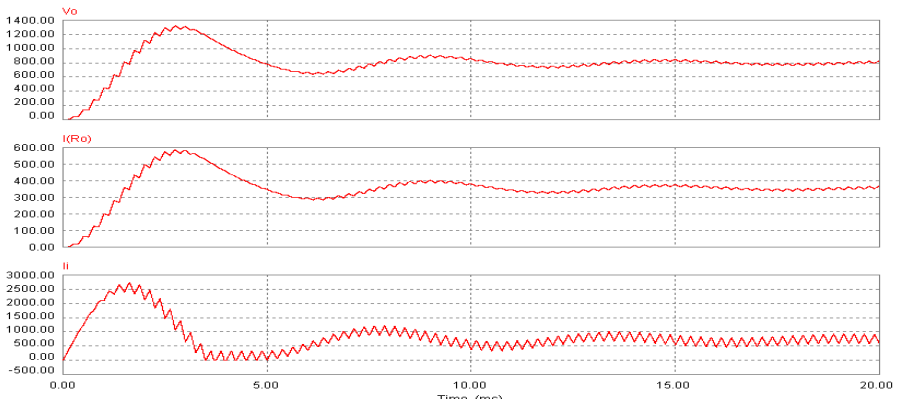

Fig. 7. Input and output waveforms with open loop conditions for synchronous clocking pulse pattern.

Figure 8, depicts the ZCS soft-switching condition for IGBT current and voltage waveforms. After using the feedback control system shown in Fig. 6, the feedback control signal Vm is modulated to obtain the gating signal; output voltage and current waveform are shown in Fig. 9.

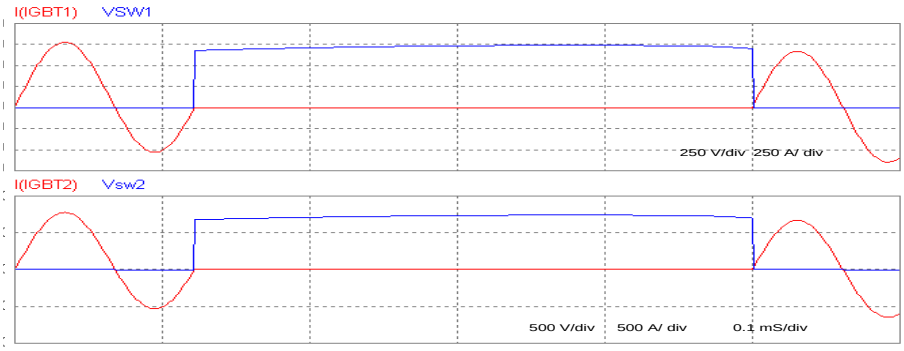

Fig. 8. IGBT current and voltage waveforms and gating signal.

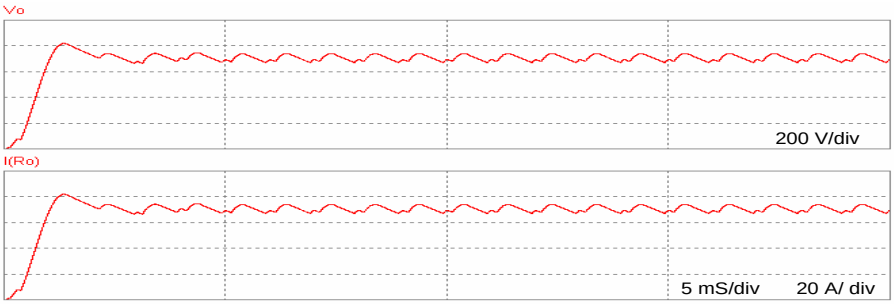

Fig. 9. Output voltage, current waveforms with feedback control.

V. Experiment Circuit Setup

The experimental DC-DC converter circuit setup treated here is shown in Fig. 10. In the DC-DC converter setup implementation. The IGBT power modules CM900CU-24NF are each IGBT with reverse conducting diode in the 6in1 IGBT power modules is used for switches $Q_1(S_1/D_1)$ and $Q_2(S_2/D_2)$ and the upper IGBT with reverse conducting diode in the 6in1 IGBT modules is used ad diode while two IGBT are not in use.

The whole appearance of experimental setup is presented in Fig. 11. The design specifications and circuit parameters are described in Table 1. Fig. 12, shows the Exterior appearance of two phase coupled inductor in the proposed soft switching PWM DC-DC converter. The IGBT power modules are mounted on the heat sink and connected to the output capacitors C_o and directly connected in parallel with the load resistors. The measured voltage and current switching waveforms of Inductor currents and gating signals with interleaved clocking are shown in Fig. 13, Inductor currents and gating signals with synchronous clocking are shown in Fig. 14.

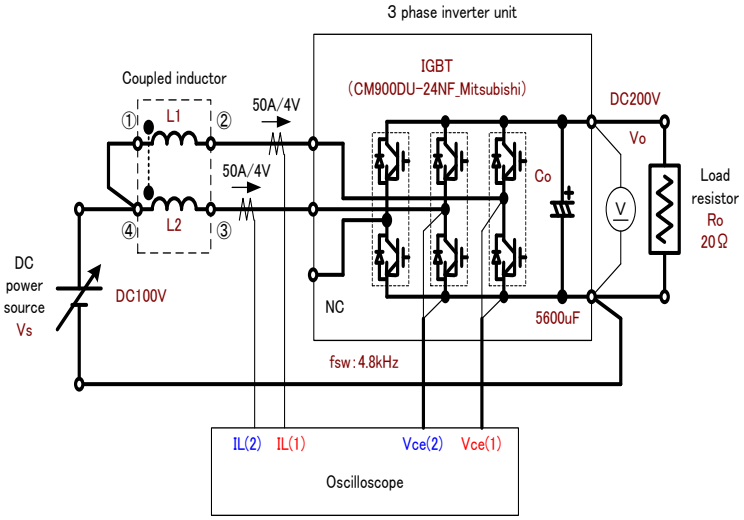

Fig. 10. Experiment circuit diagram.

Fig. 11. Picture of experimental lab setup.

Table 1. Experimental Circuit Parameters.

Item	*Symbol*	*Value*
Voltage Source	*Vs*	*100 V*
Switching Frequency	*fsw*	*4800 Hz*
Load Resistance	*Ro*	*20 Ω*
Load Voltage	*Vo*	*200 V*
Filter Capacitor	*Co*	*5600 μF*
Self Inductance of Coupled Inductor Branch 1	*L11*	*419 μH*
Mutual Inductance between Branch 1 and 2	*L12*	*351 μH*
Self Inductance of Coupled Inductor Branch 2	*L22*	*419 μH*
Coupling Coefficient	*k*	*0.84*

Fig. 12. Two phase coupled inductors.

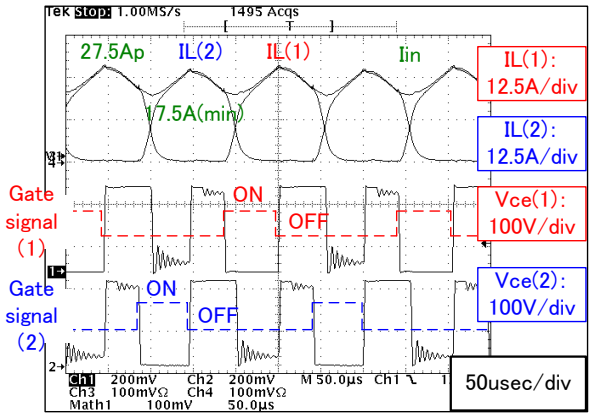

Fig. 13. Inductor currents and gating signals with interleaved clocking.

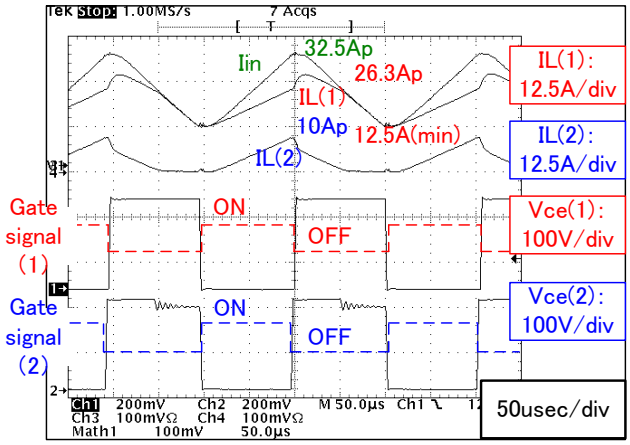

Fig. 14. Inductor currents and gating signals with synchronous clocking.

VI. Conclusion

In this paper, a novel circuit topology of voltage source multi resonant ZCS DC-DC converter with constant frequency PWM control strategy using active auxiliary quasi-resonant lossless inductor sunbbers and capacitor snubber is newly proposed, which additionally includes practical outstanding features. The operating principle of the proposed DC-DC converter topology incorporating ZCS-PWM control scheme is illustrated and evaluated on the basis of simulation results and the effectiveness of this proposed DC-DC high frequency ZCS inverter using IGBTs is substantially proved. The proposed ZCS with PWM control scheme can be able to regulate its output power under constant frequency PWM control strategy.

The use of coupled inductors could reduce the number of magnetic cores and magnetic material used and exhibits lower switch stress and lower conduction losses both in the switching device and filter capacitor on account of the smaller current ripple, and improves the converter efficiency compared to the non-coupled case. Increasing the coupling coefficient reduces the output current ripple which in turn reduces the inductor core losses. Another advantage of using coupled inductors will be reduction of size and cost.

The using of interleaved clocking has advantage of reducing the output ripple and increase the output voltage for the same circuit conditions. The fundamental characteristics of the zero-current and zero-voltage-switching techniques and the basic structure of the zero-voltage-switched circuit are discussed in this paper. Through the establishment of the zero-current switching technique and the proposed basic circuit structures, a large family of ZCS-QRCs has been derived.

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