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A Theoretical Novel Approach of High Durable Super Battery

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Abstract: *This paper focuses on the effects, energy and power storing strategy of Super Battery which is presented along with the theoretical calculations and proper justifications. Super Battery is such a device which can charge itself during a very short time, and with a long life discharging time.This battery is very crucial device in the present upgrading nanoelectronic industries. The most fundamental things of this device are charging, discharging cycle/time, energy and power has purely calculated with proper equations theoretically. Mainly concentrates on the power storage in different manners with proper analyses. This paper will contribute a very new information to the present nanotechnology science.*

Keywords: *Super battery, Nanocapacitor tray, Nanobattery device, High durable battery.*

I. Introduction

Batteries have been the most popular energy storage device since 1800 AD when the first voltaic pile was discovered. But with acceleration in technology and need for cleaner energy it is necessary to look for more efficient and environmental friendly energy storage. Along with the discovery of super capacitors one term should be most common i.e. Super Battery. It is such a device which behaves as a very fast charging device. The predictable charging time is too much less of this device and with comparison of that the discharging efficiency is very high. All the charging/discharging cycles are discussed broadly. It needs an external power supply for charging, but when it starts to discharge it can give a long durability [1] - [3]. The internal arrangement of the capacitors are in such a way that those can store a huge amount of energy within the capacitor trays.

The basic concept of the circuit connectivity of capacitors is directly used here. When the capacitors are in parallel way then the summation value of capacitances is taken and serially equivalent is taken. For the high durability operation the author selected the parallel connection [4], [5]. All the values of energy, power and the duration of the battery is calculated theoretically. The result of the paper will survive a new technical information to the modern nanotechnology science.

II. Motivation

In case of the series and parallel connections the equivalent capacitances are written as,

$C_{eq} = \frac{C1*C2}{C1+C2}$ and $C_{eq} = C_1 + C_2$ respectively.

$C = \frac{I\,tc}{V}$

$t_c = \frac{VC}{I} = \frac{C}{I/V}$

In this case t_c is the charging time constant which is directly related with the applied charge Q and voltage V. The time constant t_c can also be written as t_c = CR (R is the resistance of the capacitors). As far the resistance can be increased the time of charging would be increased [6]. On other hand, by placing a resistance regulator at the output terminal discharging time t_d can be sated as higher than charging time [7], [8]. For that the time/cycle of discharge would be increased for any output load and the device would provide a high efficiency.

III. Energy Calculation

Severally the capacitance of any capacitor is indicated by,

$C = \frac{\varepsilon A}{d}$

$U = \frac{1}{2}(\varepsilon Ad)E^2$ ($V = E \cdot d$, U is the energy stored in the parallel plate capacitor and d refers the distance between two parallel plates of capacitor)

$= \frac{1}{2d}(\varepsilon A)V^2$ …. (1)

According to the charging time concept t_c = CR due to small value of input resistance t_c become very less. When the output is taken from the output terminal the regulator increases the terminal resistance or when load is

connected then automatically the resistance increases. Hence t_d become high and the device would be gained long discharging time.

Assuming there are having same numbers of capacitors (Cn) in row and column on a tray then from the classical mathematics the total number of capacitors $C_t = Cn^2$ (here n numbers of capacitors are used) [9].

Hence the equation (1) is reformulated as,

$U = \frac{1}{2}(C_n{}^2 \cdot V^2) = \frac{1}{2}(V \cdot C_n)^2 \ldots.$ (2)

Again, the internal energy of the capacitor tray is given by in another from as follows,

$$U = \frac{1}{2d}(\varepsilon A)V^2$$
$$= \frac{1}{2d}(\varepsilon A)(IR)^2$$
$$= \frac{R}{2d}(\varepsilon A)I^2R$$
$$= \frac{R}{2d}(\varepsilon A \cdot P)$$
$$\langle P\rangle = \left(\frac{2U\varepsilon Ad}{R}\right)$$
$$= C_n{}^2\left(\frac{2Ud^2}{R}\right)$$
$$= C_n{}^2\left(\frac{1}{\frac{1}{2U}\frac{R}{d^2}}\right) \quad \ldots. (3)$$

After simplification of this power (average) with unit distance between two parallel plates of capacitor$(d = 1$ unit.

$\langle P\rangle = 2C_n{}^2\left(\frac{U}{R}\right)$

Hence, this power is varying with mainly two factors. Firstly the internal energy and secondly the resistance of the device. From table 1, the variation of internal energy has concluded previously. But one more new term is the device resistance R, which is reciprocally related with the device power. This point can be concluded as, as much the resistance would be low at the output terminal the power dissipation would be less and vice versa. For long durability operation the resistance always to be taken with a low value.

IV. Capacitance And Power Calculation

Now considering the capacitors row wise and column wise respectively if having $n[n = 1,2,3,4,5,6,7,8 \ldots\ldots\ldots]$numbers of capacitors and suppose the values of the permittivity's are $\epsilon_1, \epsilon_2, \epsilon_3 \ldots. \epsilon_n$, respectively, assuming all the capacitors are with different ε values primarily.

The capacitances are written as,

So, $C_1 = \left(\epsilon_1 \cdot A/_d\right)$, $C_2 = \left(\epsilon_2 \cdot A/_d\right)$, $C_3 = \left(\epsilon_3 \cdot A/_d\right) \ldots.$ $C_n = \left(\epsilon_n \cdot A/_d\right)$.

While assuming in row wise then the capacitance is equal toC_{n_r}.

The addictive value is $C_{n_r} = C_1 + C_2 + C_3 + \ldots\ldots + C_n$

$$C_{n_r} = \left(\epsilon_1 \cdot A/_d\right) + \left(\epsilon_2 \cdot A/_d\right) + \left(\epsilon_3 \cdot A/_d\right) + \ldots\ldots\ldots + \left(\epsilon_n \cdot A/_d\right).$$
$$= (\epsilon_1 + \epsilon_2 + \epsilon_3 + \ldots\ldots + \epsilon_n)\left(A/_d\right)$$

Taking, $\epsilon_1 = \epsilon_2 = \epsilon_3 = \ldots. = \epsilon_n$

$C_{n_r} = \left[n\epsilon_1 \left(A/_d\right).\right]$

Similarly column wise calculation also provides the value of C_{n_c} .

$C_{n_c} = \left[n\epsilon_1 \left(A/_d\right).\right]$

Next, from the previous statement which was discussed in section III, the total capacitors C_t assumed as a 2D capacitor matrix grid, with n numbers of capacitors is given by,

$C_t = (C_{n_r} \cdot C_{n_c}) = C_{n_r}{}^2 = C_{n_c}{}^2, [C_{n_r} = C_{n_c}]$

$C_t = \left(n\epsilon_1 \left(A/_d\right)\right)^2$

In previous section III equation 3, shows that

$\langle P\rangle = C_n{}^2\left(\frac{2Ud^2}{R}\right)$

$\langle P\rangle = \left(n\epsilon_1 \left({}^{A}/_{d}\right)\right)^2 \left(\frac{2Ud^2}{R}\right)$

$=2n^2 \left(U \frac{(\varepsilon A)^2}{R}\right)$ [Assuming $\epsilon_1 = \varepsilon$] …. (4)

From here it is to be written as $\langle P\rangle \alpha {}^{U}/_{R}$. [Where $2n^2(\varepsilon * A)^2$ is taken as a constant]

As discussed in the section II, the power of this device and the charging/discharging cycle depends upon the resistance applied at the output terminal [10]-[12]. Here the equation (4) denoted the same thing about the resistance. Hence with increasing of the resistance using one resistance regulator it would be possible to have long discharging time for sufficient loads.

Now apart from one tray there should to be more connected capacitor plates/trays for high efficiency purpose. Considering all the values of the capacitance there would have a huge condensation of the capacitance that can store a huge energy inside itself. It is justified by the following calculations.

Taking n numbers of trays and each tray contains the capacitances are $C_{n_1}{}^2, C_{n_2}{}^2, C_{n_3}{}^2, \ldots C_{n_n}{}^2$, respectively. According to the total capacitance of the total n trays the net capacitance is given by [13], [14]

$C_t' = C_{n_1}{}^2 + C_{n_2}{}^2 + C_{n_3}{}^2 + \ldots + C_{n_n}{}^2$.

$C_t' = nC_n{}^2$. $\left[\text{If } C_n{}^2 = C_{n_1}{}^2 = C_{n_2}{}^2 = C_{n_3}{}^2 = \cdots = C_{n_n}{}^2\right]$

$\langle P\rangle = C_t' \left(\frac{2Ud^2}{R}\right)$

$= nC_n{}^2 \left(\frac{2Ud^2}{R}\right)$

$= n\left(n\epsilon_1 \left({}^{A}/_{d}\right)\right)^2 \left(\frac{2Ud^2}{R}\right)$

$= 2n^3 \left(U \frac{(\varepsilon A)^2}{R}\right)$ [$n = 1,2,3,4,5,6,7,8 \ldots\ldots\ldots$] …. (5)

The charge is stored inside a capacitor is given by,

$Q = C_t' V$

$= nC_n{}^2 V$

$= n\left(n\epsilon_1 \left({}^{A}/_{d}\right)\right)^2 V$

$= n^3 \left(V \frac{(\varepsilon A)^2}{d^2}\right)$

Now for the unequal numbers, means the number of trays are not equal to the number of capacitances. That means taking the number of trays are m and number of capacitance are n. [where $n \neq m$]

Then this total charge is written as $Q = mn^2 \left(V \frac{(\varepsilon A)^2}{d^2}\right)$

The total charge of the device could be evaluated broadly with the m and n.

And the total power condensation is according to the equation (5),

$\langle P\rangle = 2mn^2 \left(U \frac{(\varepsilon A)^2}{R}\right)$…. (6)

V. Table

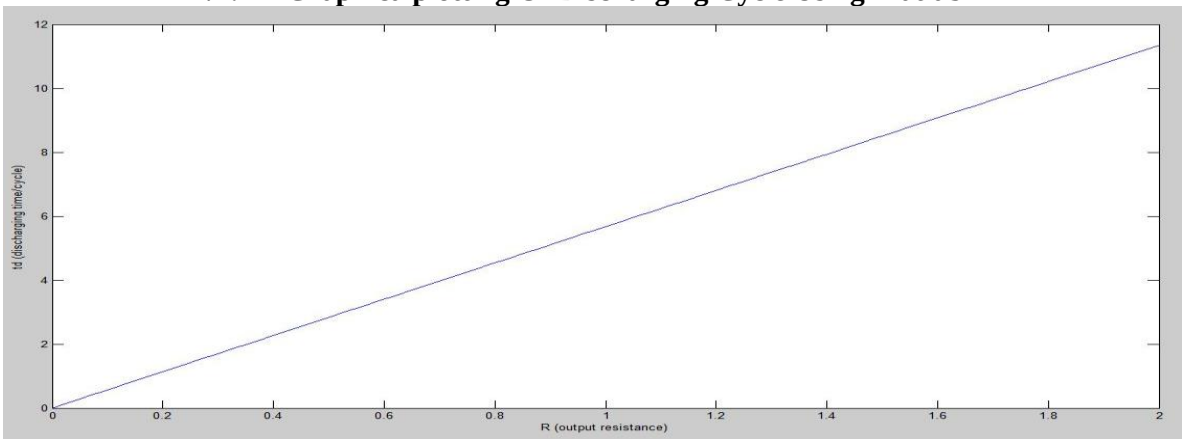
Table 1: Internal Energy Condensation Due To Applied Voltage [All Values Are Calculated By Equation 2, Section Iii]

V	C_t	U
9	50	101250
10	50	125000
11	50	151250

All the values of potential/voltage, capacitance have taken arbitrarily for the creation of above table.

It is seen that from above table, if C_t, the total number of capacitors are taken as fixed for a particular operation, then according to the applied voltage/potential the internal energies are calculated serially (in Jules unit). From above table it is clear to understand that increasing with 1V potential the internal energy raise with a high amount and device become more efficient.

VI. Graphicalplotting Of Discharging Cycle Using Matlab



This graph follows the equation t_d = CR, as mentioned in section II. Hence this plotting has justified the cycle of the discharging t_d with respect to the output resistance R. To generate this plot the capacitance C has taken at a fixed value is 10 unit and the resistance is varied from zero to 2 unit. Correspondingly the discharging time is showed in graph on Y-axis. It is successfully proved that the discharging time become higher with increasing of the output resistance.

VII. Conclusion

By the calculation of the previous sections it is clearly proved that, these kinds of capacitor structure/arrangement which is discussed in this paper, can store a huge amount of energy than other capacitor technologies. One of the most important fact of this paper is discussed in section III, i.e. in case of the simple capacitor designing the internal energy is always taken as $\frac{1}{2}$ CV^2. But here all the previous calculations are justified that the amount of internal energy is $\frac{1}{2}$ $(CV)^2$. The condensation of internal energy become more and more high and for this reason the power would be developed accordance with the internal energy. As much the internal energy and the power would be developed the discharging time would get very much high. With reference of this, the device efficiency will get high and the main motivation, discharging cycle would be increased.

References

[1]. Li. Zhang, Jin-Yan Song, Ji-Yan Zou, Ning Wan, High Voltage Super-Capacitor for Energy Storage Devices Applications, proc. 14th Symposium on Electromagnetic Launch Technology, Victoria, BC, 2008. ISBN 978-1-4244-1832-9

[2]. Al-Janad, A. Omar, R. Rasheed, M. Amhed, Comparative study of super capacitor and battery as storage energy in three phase system, proc. IEEE Conference on Clean Energy and Technology (CEAT), Lankgkwi, 2013 ISBN 978-1-4799-3237-5

[3]. Bin Wu, Fang Jhuo, Fei Long, Weiwei Gu, A Management strategy for solar pannel- battery- super capaitor hybrid energy system solar car, proc. IEEE 8th Internationla Conference on Power Electronics and ECCE, Asia (ICPE & ECCE), 2011, ISBN 978-1-612884-956-0

[4]. Sathikumar , R. Kollimalla, S.K. Mishra, M.K, Dyanamic Energy management of micre grids using battery super capaitor combined storage, proc. Annula IEEE India Conference, INDICON, Kochi, 2012 ISBN 978-1-4673-2270-6

[5]. Musolino,V, Tironi, E, A comparison of super capacitor and high power lithium batteries , proc. Electrical Systems for Aircraft on Railway ans Ship Propulation (ESARS), Bolgona, 2010, ISBN 978-1-4244-9092-9

[6]. Sheng Chen, Chih-Chen-Chen, Chen-Chain-Hwu, Shao-Hua Chen, Super Capacitor applications on series lithium batteries for robot power management, proc. 7th Asia-Pacific International Conference on Lighting (APL), Chengdu, 2011, ISBN 978-1-4577-1467-2

[7]. Aarahi, A.R, Jayan, M.V, Grid connected photovoltic system with super capacitor energy storage and STATCOM for power system stability enhancement, proc. IEEE International Conference on Advances in green energy (ICAGE), Thiruvananthapuram, 2014, ISBN 978-1-4799-8049-9

[8]. Das, S.Dey, A. Biswas, A.Mohanty, A novel design of Super-capacitor used to enhance solar energy restoration of photovoltaic cells, proc. 1st International Conference on Non-Conventional Energy (ICONCE), , Kalyani, 2014, ISBN 978-1-4799-3339-6

[9]. Zou Ji-yan, Zhang Li, Song Jin-yan, Development of 40 V hybrid super-capacitor unit, proc. 12th Symposium on Electromagnetic Launch Technology, 2004, ISBN 0-7803-8290-0

[10]. Nan Li, Jiancheng, Yun Zhong, A novel charging control scheme for super capacitor energy storage in photovoltic generation system, proc. 3rd International Conference on Electric Utility Deregulation and Restructuring and Power Technologies, DRPT 2008, Nanjuing, 2008, ISBN 978-7-900714-13-8

[11]. Soori, P.K. Shety, S.C.Chacko, S, Application of super capacitor energy storage in microgrid system, proc. GCC Conference and Exhibition (GCC), Dubai, 2011, ISBN 978-1-61248-118-2

[12]. Gazwi, Sarath, Modelling of Super Capacitor Modules and Parameters Extraction, proc. UPEC,46th International Conference, Soest, Germany, 2011, ISBN 978-3-8007-3402-3

[13]. Kaiser, Cletus J., The capacitor handbook: A comprehensive guide for correct component selection in all circuit applications, (C J Publishing, Olathe, Kansas, U.S.A., 1995).

[14]. Ben G. Streetman & Sanjay Kumar Banerjee, Solid state electronic devices (PHI Learning Private Ltd., New Delhi-110001, 2011).