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High Efficiency MOS Charge Pumps for Low-Voltage Operation Using Threshold-Voltage Cancellation Techniques for RFID and Sensor Network Applications

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Abstract: *A threshold-voltage cancellation technique is employed in a conventional Dickson charge pump to increase the pumping efficiency and cause transfer switches to be completely turned on and off in low-voltage CMOS process. A novel enhanced gate boostingtechnique is added to the resulted charge pump in order to havefurther efficiency improvement, turning transfer switches completely on and off consequently. The simulation results show that the improved charge pump has higher efficiency and provides higher output voltages.*

Key words: *charge pump, gate boosting technique, none volatile memory RFID and sensor networks.*

I. Introduction

Charge pump circuits are the key circuitsin the integrated devices when some DC voltages higher than available supplies is required; for example,programming floating gate devices and nonvolatile memories, such as EEPROM and Flash memories, requires low-voltage designs to improve the performance of the circuits [1], [2].Conversion efficiency of low voltage charge pumps such as those are used in RFID, Sensor Networks and implantable biomedical devices are highly degraded by low harvested power supply voltage, so low voltage design techniques for such charge pumps are highly demanded.Conventional CMOS charge pumps use diode-connected MOSFETs as charge transfer devices, named Dickson charge pump circuit. The DC output voltage of a positive Dickson charge pump with n stages can be approximated by the following equation [3]:

$$V_{out} = V_{dd} + n\left(V_{dd}\frac{C_p}{C_p + C_{par}} - \frac{I_{out}}{f(C_p + C_{par})} - R_{on}I_{out}\right) \qquad (1)$$

While Vddis the supply voltage, Cp is pumping capacitor of each stage, Cpar is parasitic capacitances, f is the pumping frequency, Iout is the output current, and Ron is the resistance of transfer switches when they are turned on. Some optimized design strategies for the charge pumps have been presented in [4], [5] which eliminate Ron, assuming that the transfer switches are turning on completely and have small resistance at the conducting state. This approximation degradestheaccuracy in deep-submicron CMOS integrated circuits as the transistor threshold-voltage (Vth) can not scale down proportionally to supply voltage. So the last term in equation (1) grows up and becomes considerable. Increasing the size of transistors reduces the Ron but it also increases the total parasitic capacitance and overall silicon area which reduces the total power efficiency thatcould be approximated as below[4]:

$$\eta_p = \frac{I_{out}V_{out}}{I_{Power}V_{dd}} = \frac{K}{n+1+\alpha\frac{n^2}{n+1-K}} \qquad (2)$$

In which, Ipower is the average current consumed from the supply voltage source; K is the ratio of output voltage to the input voltage (pumping gain), and α is the ratio of parasitic capacitance to pumping capacitor value.

Although considering the Ron in the analytic calculations for power optimization strategies, results in complicated and useless equations.It is clear that reducing the Ron will increase the Vout with constant number of stages which improve the pumping efficiency while the previous optimization strategies still keep their validity.

So many techniques where found in the literature which try to decrease the Vth of transistors in charge pump circuits for low-voltage operation and preventing the Vth augmentation of the transistors due to body effect, specially in NMOS charge pumps. Using the internal boosted voltage to backward control the charge transfer switch of the previous stage and applying a dynamic control to the charge transfer switches in order to eliminate the reverse charge sharing phenomenon are proposed in [2] which are suitable for the low-voltage operations.Using dynamic adjustment of the body voltage with removing the back bias effect, proposed in [6] the Vth of the transfer switches are kept constant. High efficiency MOS charge pumps are introduced in

[7],utilizing an exponential-gain structure and pumping gain increase circuits, which solve the Vth problem of the MOSFET used as a transfer switch. In [8] two symmetrical charge pumps, controlled by two out-of-phase pumping signal, are used which offer out-of-phase node voltages to control the switches of the opposite charge pump instead of internal boosted voltage. Using a four-phase clocking system to boost the gate-source voltage of transfer switches and updating the body voltage of transistors is proposed in [9] for low-voltage operation. An effective boosting of control signals of the transfer switches is employed in [10] to enhance driving capability while keep the impact of the parasitic elements to as low as possible. A charge pump circuit with two pumping branches is proposed in [1] and it is mentioned that, as the transfer switches can be completely turned on and off, its pumping efficiency is higher than traditional designs. Although it is clear thatthese charge pumps will fail to operate in low-voltage operations.

Equations (1) and (2) implies that havingthe constant output voltage and constant load current with highest pumping efficiency, needs to reduce the number of stages, parasitic element, and amount of Ron of transfer switches as much as possible. A new threshold-voltage-cancellation technique is employed in this paper to completely turn on the small sized transfer switches in the low-voltage operation. The resulted charge pumps has high pumping gain and efficiency while it has small parasitic elements which use single phase clocking, and work properly in low-voltage operations. Another enhancement technique is employedin the resulted charge pump to under-drive the transfer switches in off-state and also reduces the reverse charge sharing phenomenon effectively in order to have further overdrive of each switches in on-state.

The second part of this paper will introduce the proposed charge pump and the enhanced one. The third part will discuss the simulation results, and the conclusion is coming in the last part.

Proposed Charge Pumps:

The idea of external Vth cancellation technique is employed in [11] for a high-sensitivity rectifier circuit to operate with small RF signal amplitudes. We use a similar technique in the low-voltage charge pump circuits in order to reduce the Vth of transfer switches to turn them on completely in on-state. It is mentioned that using Vth below 100 mV is not suitable; because MOS transistor's absolute variation of ±100 mV generally make thetwo following transfer switches to be attheir on-state simultaneously and off-leaks will occur [11]. Fig. 1 shows the schematic of an eight-stage NMOS charge pump in which the gate terminal of each transfer switches is boosted to voltages as high as Vb so the switches turned on completely even with low voltage input clock signals. In the other word, the Vth of the transistors are reduced by the value of Vb. Although it increases the off-leak ofthe switches, charge pump circuit can operate with low-voltage input clock and generates the desired high output voltage. Also, size of the switches can be kept low enough to reduce the parasitic elements and increase the pumping efficiency at high output currentswhich the overdrive is sufficient to drive the output resistive load or fast charging of the capacitive loads.

Fig. 2 shows the implementation of the employed technique. A diode-connected NMOS transistor is biased to generate the reference voltage for Vb. The boosting capacitor cbi holds the boosting voltage between gate-source of the transfer-switch MOS, while the flying capacitor cfi updates its voltage to the value of Vb in each clock period. The value of cbi should be selected higher than the gate-source parasitic capacitance of each switches,in order to keep its voltages constant in the both clock phases effectively. The Vb distributor can work with lower clock frequencies, but working with the same clock frequency ofcharge pump, causes no significant increase in dynamic power consumption because the power consumption of the Vb distributor network is limited to the leakages of the gate-source parasitic of switches.

Although the Vth cancellation techniques works well for the completely turn on transfer switches, it increases the off-leakage because of reductionof the Vth of the switches, so they can not become completely turned off.The off-state of switches is worse than a charge pump circuits without using the cancellation technique. Another drawback of the employed Vth cancellation technique is that the value of gate-boosting Vb is limited to 100 mV lower than theVth of the transistors. So the Vthcan not be canceled completely in the on-state. To solve this problem, an enhancement switching technique is added to the proposed charge pump which under-drives the gate voltage in the off-state and over-drives it effectively in the on-state. Fig. 3 shows this enhancement technique. The boosting voltage of Vb is applied to the gate of the each on-state switches and an under-drive voltage of -Vb is applied to off-state in the first phase of the clock. The applied boosting voltage inverts in second phase of the clock as the on-state switches turn off, and the off-state switches turn on in the second clock phase. In this manner when a switch turns on the Vb is applied to its gate-source and when it turns off the applied voltage changes to -Vb, so the Vb can be higher than the Vth of the transistor to overdrive the transistor effectively and increase its drive capability even with small sizes. Increasing the Vb no longer has the drawbacks of off-leakage in the off-state because the gate-source is under-drived by the same overdrive value and resultsfurther reductionin the off-leakage.

Fig. 4 shows the implementation of the enhancement technique in the proposed charge pumps. The boosting capacitor cbi is connected to gate-source of the transfer switch trougha direct and crossed switches which conducts according to the state of the transfer switch and connects the boosting capacitor cbidirect or inverted to the gate-source. The flying capacitor cfi updates the cbi with the Vb in each clock period. Then the value of the Vb is set to Vdd. As the boosting capacitor must be connectedto the gate-source of the transfer switch in each on and off state,so the Vb distributor network must work with the same clock ofthe charge pump circuit. As the boosting capacitor never discharged and its terminals is swap between gate and source of the transfer switches, the dynamic power consumption is limited to the parasitic leakages and the Vb distributor still offers insignificantdynamic power consumption.The switches in Vb distributor are implemented using simple NMOS and PMOS transistors. Low-voltage switching techniques such as gate-boosting and bootstrap switches can be employed to increase the Vb distributor operability.

Simulation Results:

In order to compare the charge pump characteristics, some eight-stage NMOS charge pumps where designed and simulated in a 0.18 µm CMOS technology including a simple Dickson charge pump, an external Vth cancellation (EVC) charge pump, and an enhanced external cancellation charge pump (EEVC). Simulations performed for different load conditions and with different supply voltages. Also, frequency is set to 10 MHz.The size of transfer switches as well as the pumping capacitors were chosen so as to achieve the optimum charge pump. Fig. 5 shows the resulted output voltage versus the supply voltages ranging from 0.6 V to 1.8 V under 0.1 MΩ resistive load condition. The slope of this characteristic implies an increasing pattern in pumping gainfrom Dickson to EVC and EEVC. Fig. 6 represents the output voltage versus different resistive loads ranging from 0.1 MΩ to 10 MΩ. The results show the effectiveness of the proposed techniques to reduce the voltage losses across the switching devices and increase the output voltage. Fig. 7 shows the delay for the output voltage to reach to its final value, normalized by pumping gain as the higher output voltages need longer time to settle. The results imply that the EEVC offers the least and constant delay while the supply voltage varies. Fig. 8 represents the same parameter versus different load condition. EVC and EEVC offers constant delay in contrast with the simple Dickson charge pump. Fig. 9 shows the pumping efficiency versus the pumping gain for different load conditions. The pumping efficiency and pumping gain of the EEVC is higher for equal load conditions while the EVC offers higher pumping gain with similar pumping efficiency to Dickson charge pump. Higher pumping gain results in higher pumping efficiency.This is because of equation (2) and the fact that to gain a desired output voltage, circuits with higher pumping gain use lower number of stages and offer higher pumping efficiency. Fig. 10 represents the pumping efficiency versus the load current under different load conditions. The EEVC offers higher load current with higher pumping efficiency while the EVC deliver higher load current with a pumping efficiency equals to that of Dickson. Fig. 11 compares the pumping efficiency of the EVC and EEVC versus load current variations resulted from supply voltage variation ranging from 0.6 V to 1.8 V. The overall efficiency of the EEVC is higher than EVC and it offers higher load currents with the same supply voltage. The current in which the efficiency is maximizeddetermines the load that the charge pump is optimized for.

II. Conclusion

A new charge pump circuit has been proposed using the external Vth cancellation technique. It has been shown that he proposed charge pump is suitable for low-voltage applications and offers higher pumping gain, efficiency and load current. The proposed charge pump has the drawbacks of limited boosting voltage and off-leakage. An enhancement technique has been proposed to solve the problem. The enhanced proposed charge pump shows the highest possible pumping gain and efficiency while still works well in low-voltage operations.

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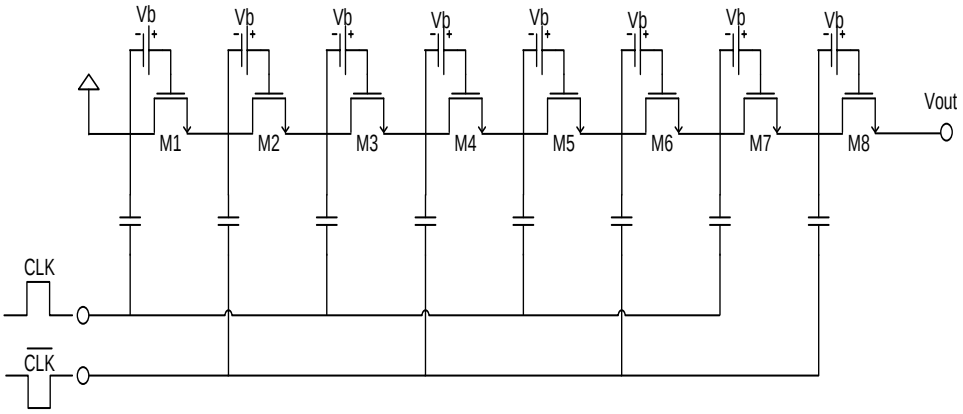

Fig.1 Schematic of an eight-stage NMOS charge pump using external Vth cancellation (Bodies of all transistors are connected to ground.)

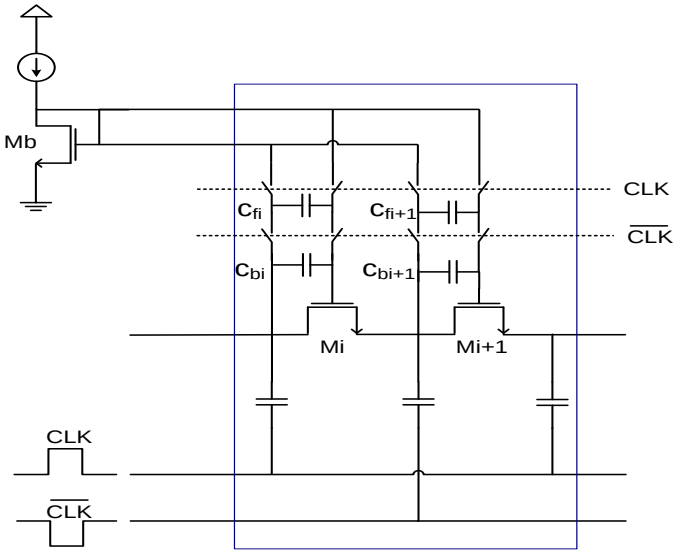

Fig. 2 Implementation of external Vth cancellation (EVC) technique.

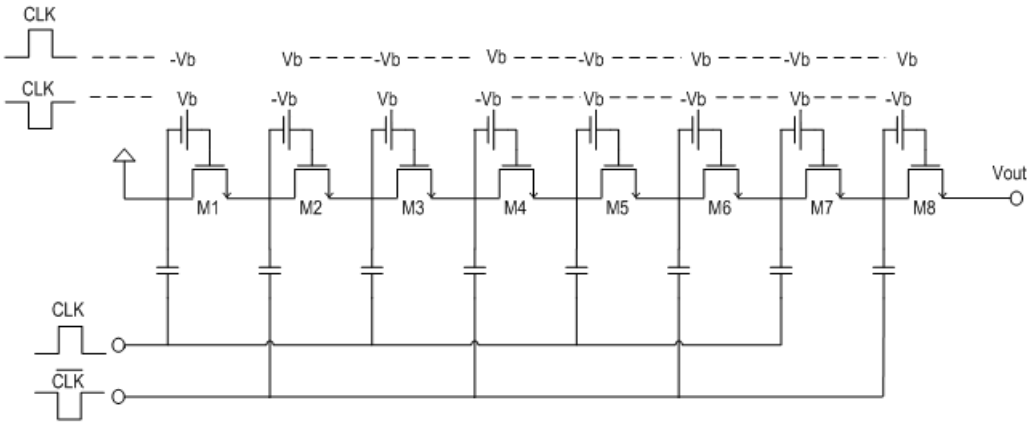

Fig. 3 Schematic of an eight-stage NMOS charge pump using enhanced external Vth cancellation. (Bodies of all transistors are connected to ground.)

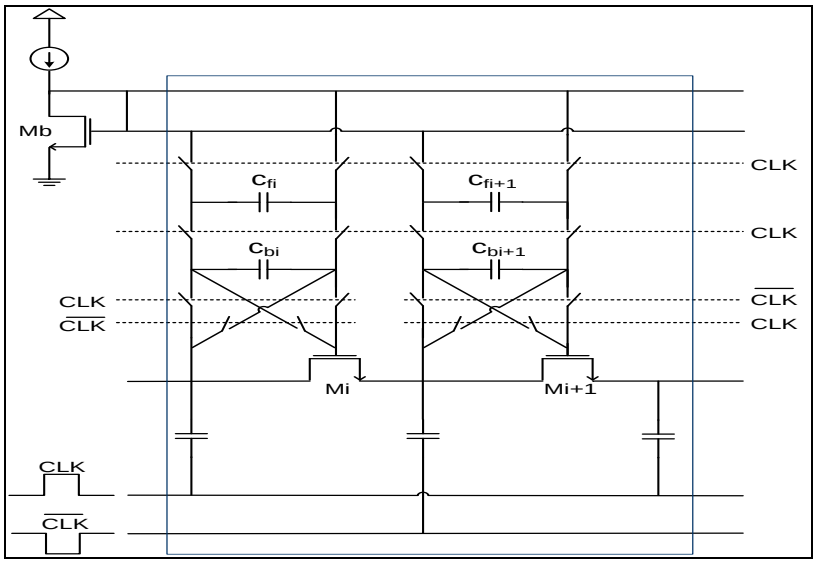

Fig. 4 Implementation of enhanced external Vth cancellation (EEVC) technique.

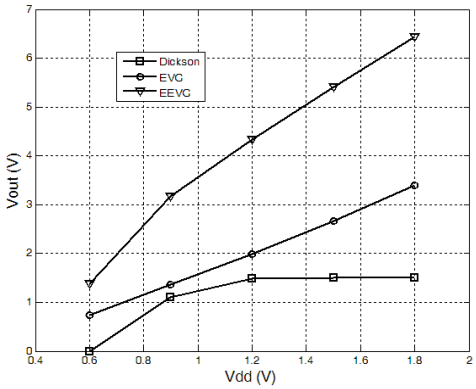

Fig. 5 Output voltage versus. the supply voltage

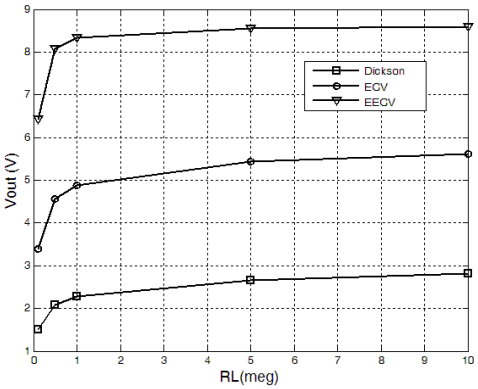

Fig. 6 Output voltage versus the load resistance.

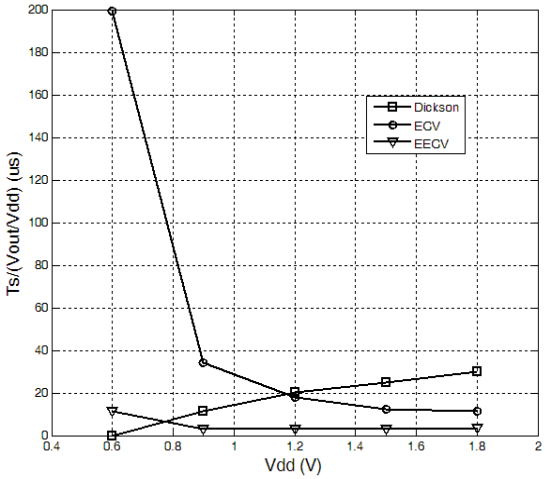

Fig. 7 Normalized output voltage settling time versus the supply voltage.

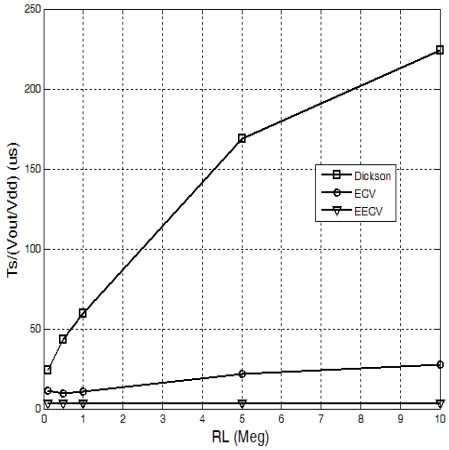

Fig. 8 Normalized output voltage settling time versus the load resistance.

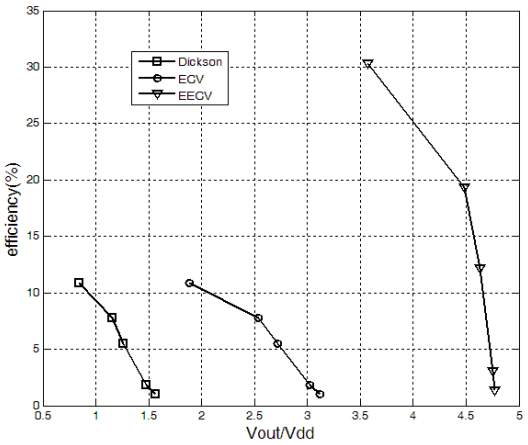

Fig. 9 Pumping efficiency versus the pumping gain for different load conditions.

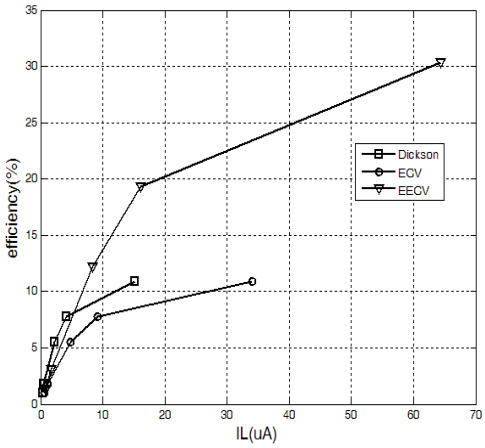

Fig. 10 Pumping efficiency versus the load current under different load conditions.

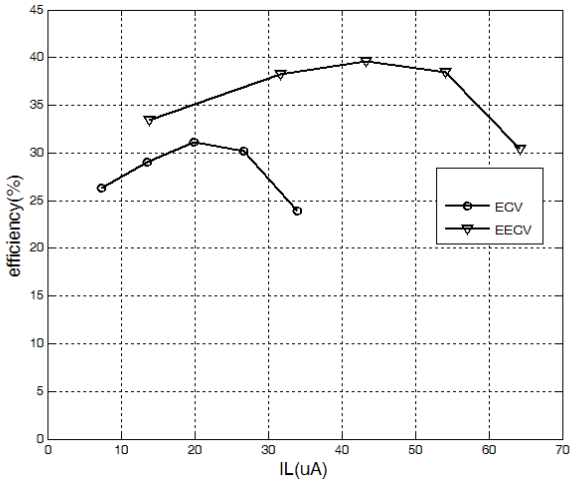

Fig. 11 Pumping efficiency of the EVC and EEVC with load current variations with the supply voltage variation.