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Control and Analysis of the Transistor Clamped H bridge Split Phase PWM Inverter

Jayamohan. M[1], David. E[2]
[1](Department of EEE, M.Tech student of NCERC Pampady, India)
[2](Department of EEE, Assistant Professor of NCERC Pampady, India)

Abstract: *In PWM inverters, the short through of the phase leg is always a problem for reliability, efficiency and higher switching frequency. Besides this, power device on/off time and the reverse recovery time of poor performance body diodes will limit the switching frequency and power conversion efficiency. This paper presents an analysis of a transistor clamped H-bridge split phase PWM inverter which could split the MOSFET based phase legs by coupled inductor to prevent the short through and disable poor performance body diode. Double using double reference single carrier modulation technique. Results are obtained using simulations done in MATLAB Simulink environment.*

Keywords: *Electro Magnetic Interference (EMI), Multi Level Inverter, Pulse Width Modulation, Total Harmonic Distortion(THD), Transistor Clamped H Bridge(TCHB)*

I. Introduction

The increasing energy consumption along with diminishing nature of fossil fuels creates a booming interest in renewable energy generation systems. The advancement in power electronics also promotes these renewable energy systems. A single-phase grid-connected inverter is usually used for residential or low-power applications of power ranges that are less than 10 kW. Types of single-phase grid-connected inverters have been investigated [3]. One of the drawback of single phase inverter is the short through problem. The traditional solution for this problem is to simply add a dead time into the switching interval, which brings the duty cycle loss to some extent and also limit the switching frequency. The high di/dt and dv/dt from diode reverse recovery will also possible destroy power device. To better improve the efficiency and reliability of the inverter some new inverter structures are proposed to solve this problem, such as the dual buck inverter, the split phase PWM inverter, and so forth [1]. These structures are all widely used in the application for the advantage of having no short through problem and low reverse recovery loss. This topology could both solve the problem of short through problem and the reverse recovery problem of the bad performed body diode. To improve the output the level must be increased. A common topology of this inverter is full-bridge three-level. The three-level inverter can satisfy specifications through its very high switching, but it could also unfortunately increase switching losses, acoustic noise, and level of interference to other equipment. Improving its output waveform reduces its harmonic content and, hence, also the size of the filter used and the level of electromagnetic interference (EMI) generated by the inverter's switching operation [3]. Multilevel inverters are promising; they have nearly sinusoidal output-voltage waveforms, output current with better harmonic profile, less stressing of electronic components owing to decreased voltages, switching losses that are lower than those of conventional two-level inverters, a smaller filter size, and lower EMI, all of which make them cheaper, lighter, and more compact [3]. A typical single-phase three-level inverter adopts full-bridge configuration by using approximate sinusoidal modulation technique as the power circuits. The output voltage then has the following three values: zero, positive (+Vdc), and negative (−Vdc) supply dc voltage (assuming that Vdc is the supply voltage). The harmonic components of the output voltage are determined by the carrier frequency and switching functions. Therefore, their harmonic reduction is limited to a certain degree [4]. To overcome this limitation, this paper presents a transistor clamped H bridge split phase PWM inverter whose output voltage can be represented in the following five levels: Vdc, +1/2Vdc, zero, −1/2Vdc, and −Vdc. As the number of output levels increases, the harmonic content can be reduced. This inverter topology uses two reference signals, instead of one reference signal, to generate PWM signals for the switches.

II. Proposed System

The proposed inverter topology is shown in Fig. 1. In which the coupled inductors L1, L2, L3 and L4 avoid the shoot through problem in the power switches by reducing large inrush current at switching transitions[1]. This causes reduction high di/dt across the switches thereby allowing lower rated switches.

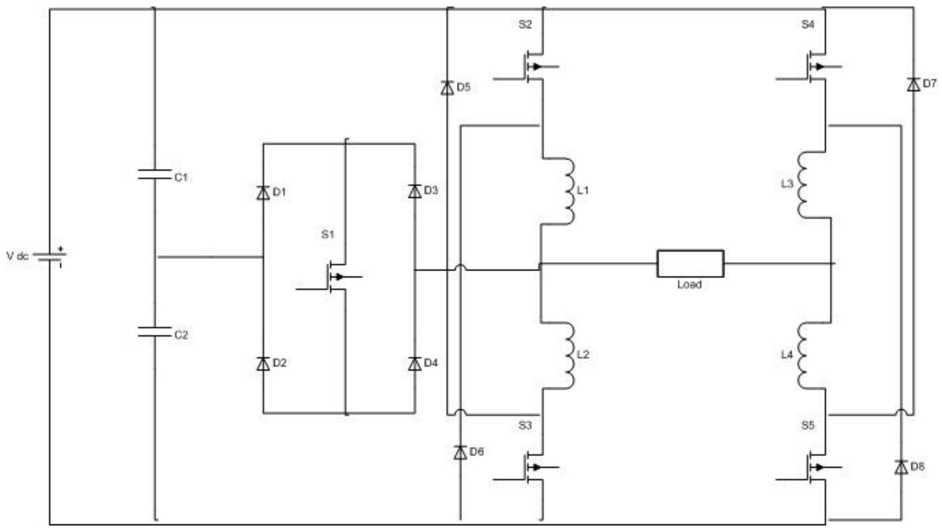

Figure 1- Circuit diagram of the proposed circuit

According to the control algorithm the switching action takes place such a way that the proposed inverter generates five level output voltages, i.e., +V, +V/2, 0, −V/2, and –V[3]. The switching transitions and corresponding output voltage are given in Table I. In which the state= 0 represents OFF position and state= 1 represents ON position of switches. The generation of five level output voltages are given as follows.

1) When S2 and S5 are in ON position and all other switches are in OFF position, the maximum input voltage V appeared across load.

2) When S1 and S5 are in ON position and all other switches are in OFF position, the half of the input voltage, V/2 appeared across load.

3) When S2 and S4 are in OFF position or S3 and S5 are in OFF, there is no voltage appeared across load.

4) When S1 and S4 are in ON position and all other switches are in OFF position, the half of the input voltage with negative polarity, –V/2 appeared across load.

5) When S3 and S4 are in ON position and all other switches are in OFF position, the maximum input voltage with negative polarity, **-**V appeared across load.

Based on valid switch combinations, S1−S5 in Table I, the cell output voltage Vout can be represented by equation(1).

$$V_{out}=V(S5-S4)\{(1/2)S1+|S2-S4|.|S3-S5|\} \quad (1)$$

Table I: Transisitor clamped H bridge split phase pwm inverter output voltage

S1	S2	S3	S4	S5	Vout
0	1	0	0	1	V
1	0	0	0	1	V/2
0	0 or 1	1 or 0	0 or 1	1 or 0	0
1	0	0	1	0	-V/2
0	0	1	1	0	-V

The gate pulses generated by comparing two sinusoidal reference signals Vref1 and Vref2 are compared with the high frequency triangular carrier signal at a time[2]. The pulse generation is done as follows. When Vref2<V3<Vref1, S1 is enable; Vref1&Vref2 >V3, S2 is enable; Vref1&Vref2 <V3, S3 is enable;. This will lead to a switching pattern, as shown in Fig. 2.

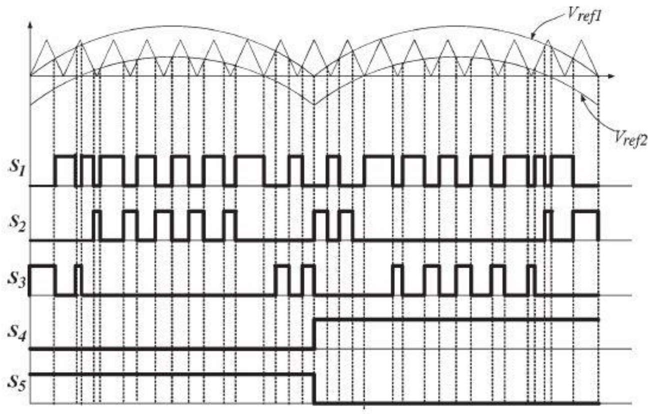

Figure 2- Switching pattern for the single-phase five-level inverter

Switches S1–S3 will be switching at the rate of the carrier signal frequency, whereas S4 and S5 will operate at a frequency equivalent to the fundamental frequency. Table I illustrates the level of Vinv during S1–S5 switch on and off. The coupled inductor will help to protection from high current, high di/dt, dv/dt, and also no shoot through problem etc.

III. Results And Discussions

The Transistor Clamped H Bridge split phase PWM inverter with reduced number of switches is simulated using MATLAB-Simulink platform. The Simulink model of the proposed system, its output voltage, THD are shown in figure.

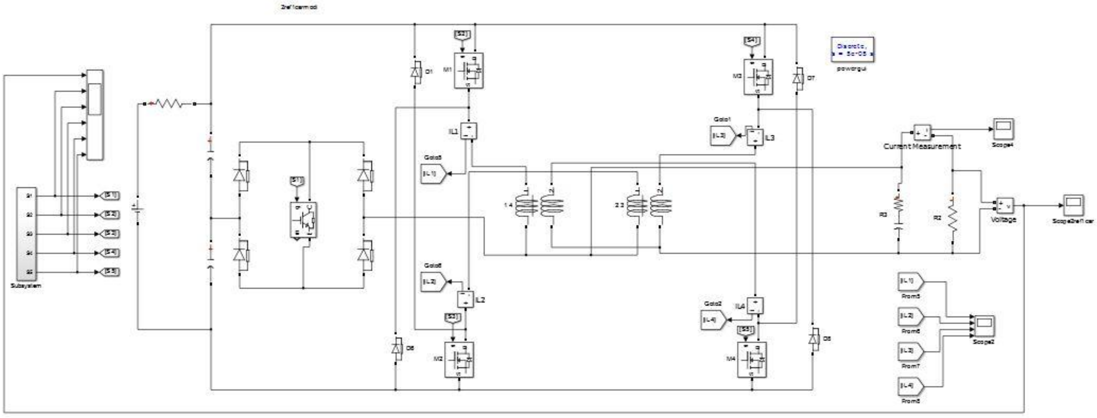

Figure 3: The simulink model of TCHB splitphase inverter

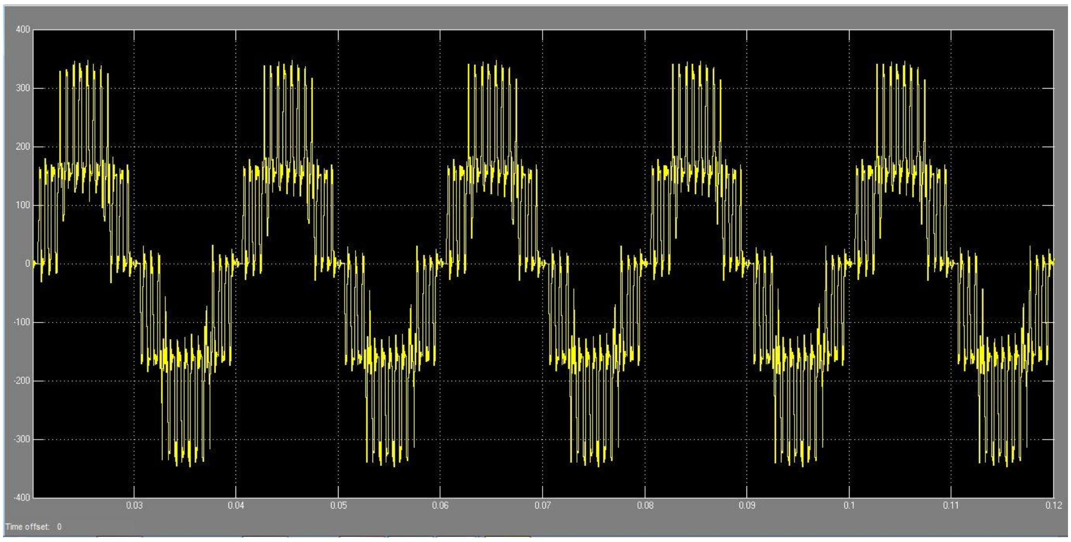

Figure 4- The output voltage waveform

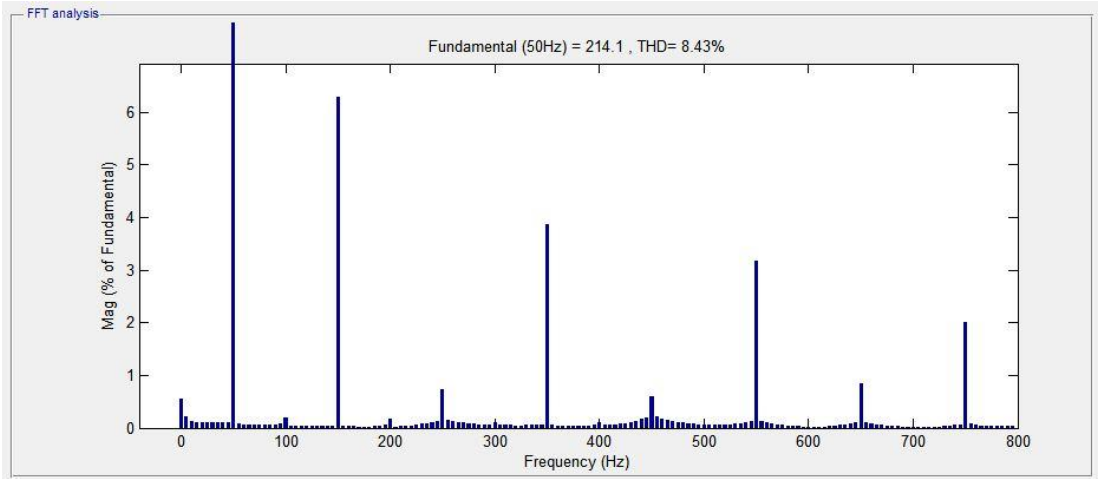

Figure 5- The THD of the output voltage get 8.43%

The output of the inverter get a five level voltage. The total harmonics is reduced to 8.43%.

IV. Conclusion

In this paper, double reference single carrier modulation technique is employed for a transistor clamped H-bridge split phase inverter. The harmonics present in the inverter output voltage is determined through FFT analysis. Simulation results indicate that the THD of proposed inverter is much lesser than that of conventional cascaded inverter. The THD of voltage (Vout) of a proposed inverter is 8.43%. The proposed inverter is simulated by using MATLAB/ Simulink performance waveforms are verified.

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