

Design and Analysis of Sram Cell for Reducing Leakage in Submicron Technologies Using Cadence Tool

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Abstract: Leakage power has become a great challenge now a days. As the size of the device shrink the leakage power increases. So the leakage power is the very serious problem in CMOS chips. As we move towards the submicron technology the device consistency and the threshold voltage become smaller. When decreasing the supply voltage, the threshold voltage and the oxide thickness decreases due to this leakage increases. The main motivation of this work is to reduce the leakage of the SRAM. The circuit of the SRAM is designed by using different leakage reduction technique like sleep transistor technique, force stack technique, sleepy stack technique and simulated in the cadence virtuoso tool using 45nm, 90nm, 180nm process technology.

Keywords: SRAM, leakage power, submicron, threshold voltage, cadence tool.

I. Introduction

Leakage power is the serious issue in VLSI circuits, for which CMOS is the primary technology. The leakage current depends on the threshold voltage, channel physical dimensions, channel doping, physical dimensions, drain and source junction depth, gate oxide thickness, temperature and supply voltage [1]. Today as the size of the device or chips reduces. The ITRS report that the leakage power dissipation may come to overcome the total power consumption [2] Scaling improves transistor density and functionality on a chip. Scaling helps to increase speed and frequency of operation and hence higher performance. At the same time power dissipation increases. To counteract increase in active and leakage power V_{th} should also be scaled. Leakage power is catching up with the dynamic power in CMOS circuits as shown in Fig. 1.

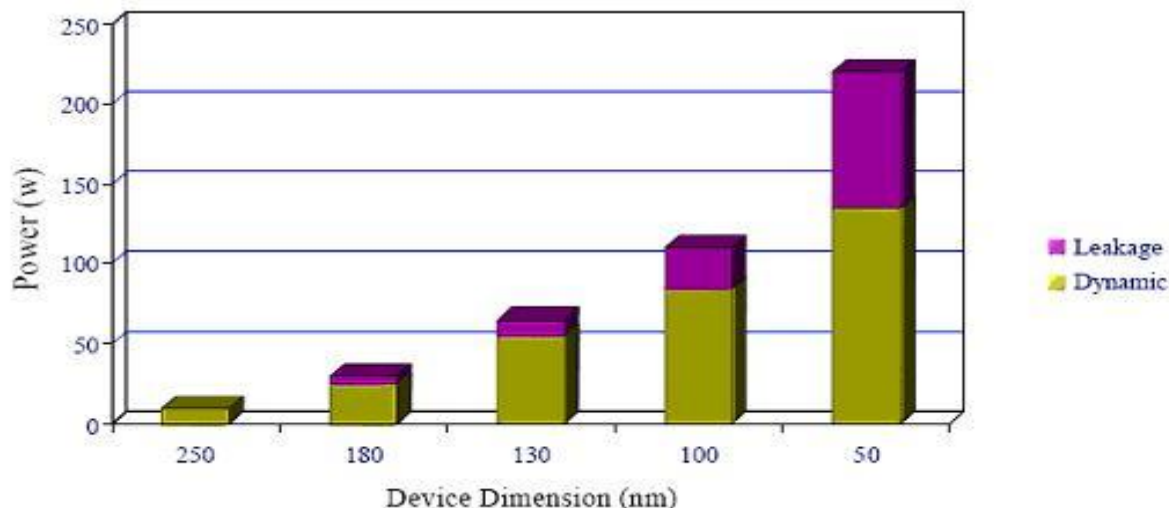


Fig.1 Leakage vs. Dynamic power [3]

To solve this problem of leakage many researchers proposed various technique to reduce this leakage like sleep, stack, sleepy stack and sleepy keeper etc. However there is no universal way to avoid the tradeoff between power, delay, and area .thus the designer are required to choose appropriate technique that satisfy application and product need.

According to Sung Mo Kang et al. [4] and Anantha P. Chandrakasan et al. [5] power consumption in a circuit can be divided into 3 different components. They are:

- i) Dynamic
- ii) Static (or leakage) and
- iii) Short circuit power consumption.

Dynamic (or switching) power consumption occurs when signals which go through the CMOS circuits change their logic state charging and discharging of output node capacitor. Leakage power consumption is the power consumed by the sub threshold currents and by reverse biased diodes in a CMOS transistor. Short circuit power consumption occurs during switching of both NMOS and PMOS transistors in the circuit and they conduct simultaneously for a short amount of time. In the previous days the dynamic power consumption was the serious issue as the dynamic power is 90% of the total power of the chip. Therefore many previous technique like voltage scaling and frequency scaling are mainly focus on the dynamic power. However as now a days due to decrease in size static power exceed the dynamic power. Kim et al. report that subthreshold power of chip may exceed dynamic power dissipation at 65nm feature size [6]. Also when the threshold voltage scaling results increase of threshold current (I_{SUB}) [7]. There are basically four main source of leakage in the MOSFET [8].

- (i) Reverse biased junction leakage current [I_{REV}].
- (ii) Gain induced drain leakage [I_{GIDL}].
- (iii) Gate direct tunneling leakage [I_G].
- (iv) Subthreshold leakage [I_{SUB}].

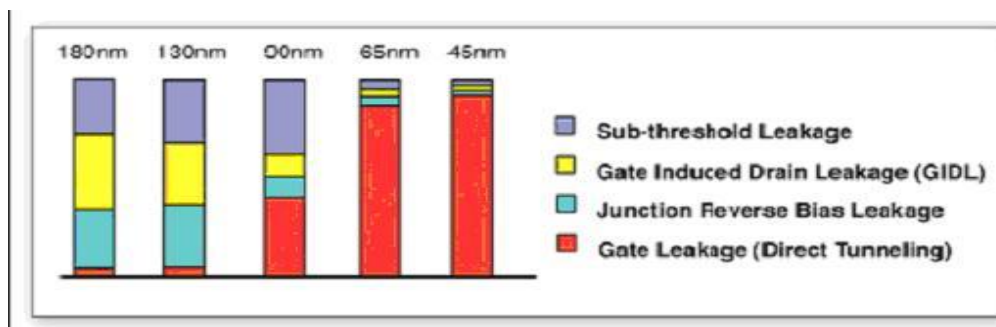


Fig. 2 Technology shrinking vs. Leakage components

To reduce the leakage there are many technique these technique can be grouped into two categories (i) state saving technique where the circuit state (present) is retained and (ii) circuit state destroyed [6]. A state saving technique has one advantage over the state destructive technique is that in state saving technique the circuitry can immediately resume operation. State destructive technique cutoff transistor (pull up or pull down or both) network from supply voltage or ground using sleep transistor [9].

Section 2- SRAM design by various technique

Section 3- Results and discussion

Section 4- conclusion.

II. Sram Design Using Various Techniques

2.1 Base Case

Fig. 3. Shows the schematic of the basic 6-T SRAM. In this circuit WL represent the word length. BL and BLBAR represent the bit line and bit line bar. Here the Width of the PMOS transistor is double of the NMOS transistor. Here the power dissipated during the active and the standby mode is very high. So we use different techniques to reduce the power of the circuit.

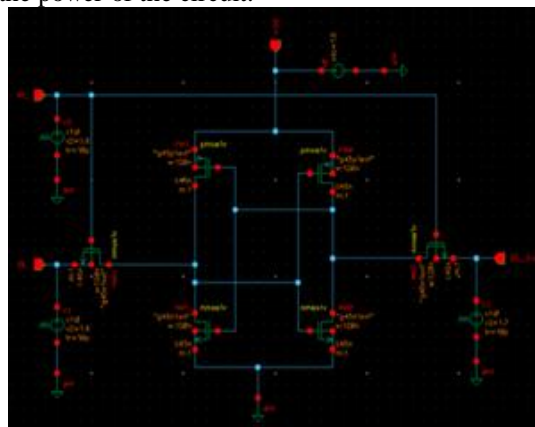


Fig.3. basic 6-T SRAM

2.2 Sleep Transistor Techniques.

In this technique sleep transistors are used at two different position one is between VDD and pull-up network and other is between ground and the pull-down network. The sleep transistors are turned off when circuit is not in use. This technique reduces the leakage power dramatically in sleep mode but sleep transistor increase the delay and area of the circuit. Furthermore in this technique state will lose during sleep mode. Due to this wake up time and energy of the sleep technique affect. Fig.4 shows the SRAM using the sleep transistor technique. Here the W/L of the PMOS transistor is double of the NMOS. High V_{th} transistors are used for the sleep transistor. By isolating the logic network using sleep transistor leakage reduces.



Fig. 4 SRAM using sleep transistor technique

2.3 Forced stack technique

This technique overcome the disadvantage of the sleep technique i.e. it retain the state but it take more wake up time. This technique for leakage power reduction is forces a stack effect by breaking down an existing transistor into two half size transistors [10]. When the two transistors are turned off together, induced reverse bias between the two transistors results in sub-threshold leakage current reduction. Narendra et al study the effectiveness of the stack effect including the effect of the increasing the channel length [11] but it increase the delay of the circuit. Fig. 5 shows the structure of the SRAM using the forced stack technique.

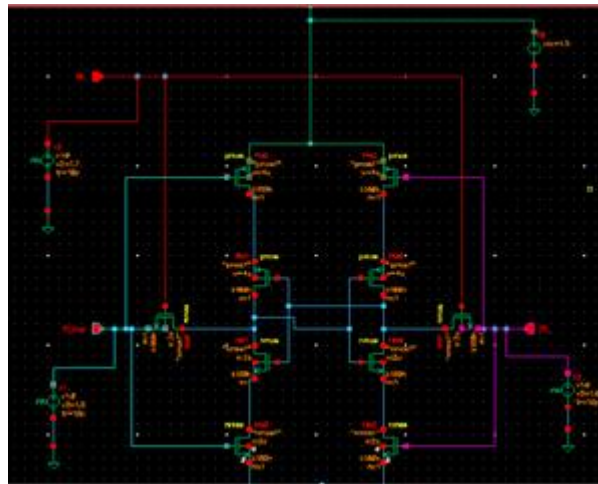


Fig. 5 SRAM using force stack technique

2.4 Sleepy stack technique

The sleepy stack approach combines the sleep and stack approach [12] i.e. Sleepy stack technique is the combination of both sleep transistor and the forced stack technique. it overcome the disadvantage of both sleep transistor and forced stack i.e. it retain the logic state and it can use high V_{th} transistor. This technique can achieve ultra-low leakage power consumption while saving state. In this technique we divide the original transistor into two transistor each typically with the same width $W1$ half of the size of the original single transistor width $W0$ (i.e. $W1 = W0/2$). The leakage reduction of the sleepy stack structure occurs in two ways. First, leakage power is suppressed by high- V_{th} transistors, which are applied to the sleep transistors and the

transistors parallel to the sleep transistors. Second, stacked and turned off transistors induce the stack effect [13] Fig.6 shows the sleepy stack SRAM using the sleepy stack technique.

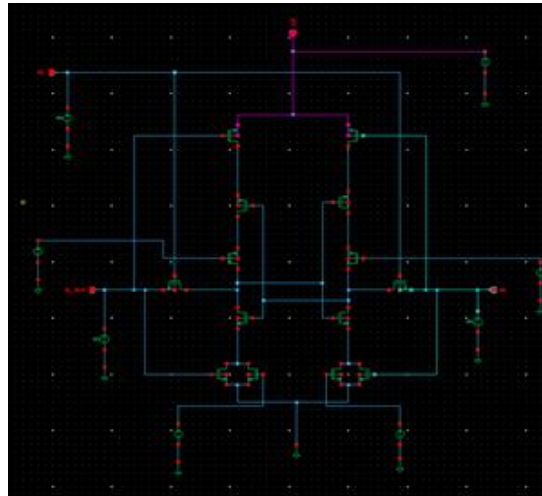


Fig.6 SRAM cell using the sleepy stack technique

III. Results And Discussion

Here, we compared the three technique of leakage i.e. sleep transistor , force stack and sleepy stack also the base of 6-T SRAM in terms of static and dynamic power.

The results shows that the sleepy stack technique produce higher leakage reduction and also produce more stability to the circuit as compare to the other technique. All the simulation are done using 45nm, 90nm and 180nm bulk MOSFET in cadence virtuoso tool using Spectre simulator.

The following graphs and the tables shows the static and dynamic power SRAM cell.

Fig.7 shows the static power versus various techniques and Fig.8. Shows the dynamic power versus various technique in 45nm, 90nm and 180nm of technology.

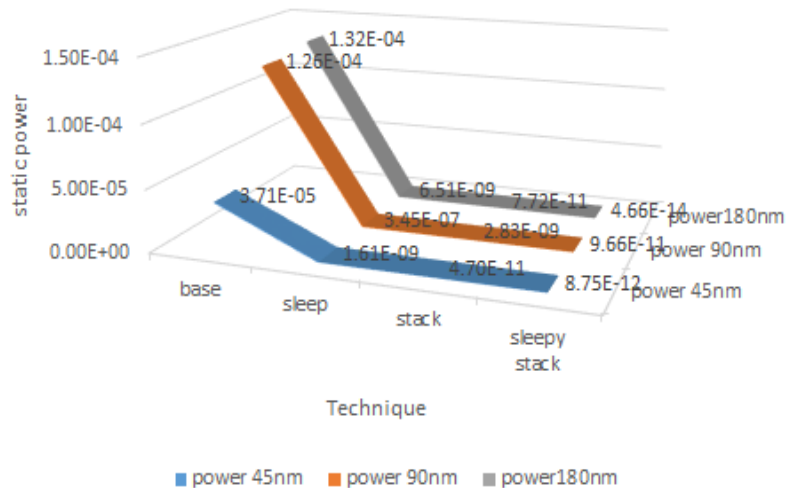


Fig.7. Static power vs various Technique

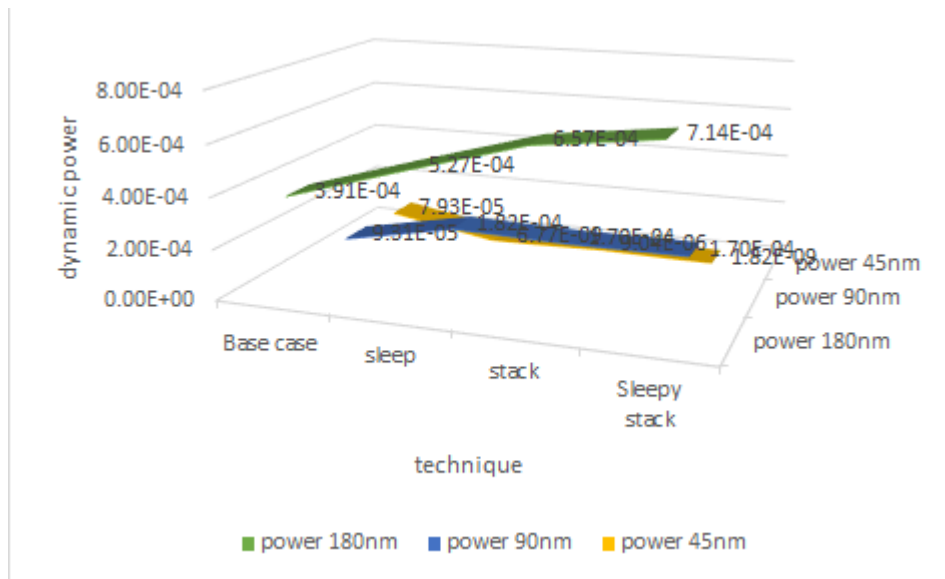


Fig.8. Dynamic power vs various Technique

Table-1: Static Power For Various Technique In Different Technology

S.NO	Technique	180nm	90nm	45nm
1.	Base case	1.32E-04	1.26E-04	3.71E-05
2.	Sleep transistor	6.51E-04	3.45E-07	1.61E-09
3.	Force stack	7.72E-11	2.83E-09	4.70E-11
4.	Sleepy stack	4.66E-14	9.66E-11	8.75E-12

Table -1 shows the static power for various technique in 45nm, 90nm and 180nm technology.

Table -2: Dynamic Power For Various Technique In Different Technology

S.NO	Technique	180nm	90nm	45nm
1.	Base case	3.91E-04	9.31E-05	7.93E-05
2.	Sleep transistor	5.27E-04	1.82E-04	6.77E-09
3.	Force stack	6.57E-04	1.701E-04	9.039E-06
4.	Sleepy stack	7.135E-04	1.704E-04	1.82E-09

Table -2 shows the dynamic power for various technique in 45nm, 90nm and 180nm technology.

IV. Conclusion

The leakage power become high as we go towards the finest technology. In this paper we used various technique to reduce leakage. The sleepy stack technique produce higher leakage reduction but increase in chip area. The sleepy stack is a combined structure of forced stack and the sleep transistor technique. While compare to the sleep transistor technique it retain the logic state of the circuit.

In conclusion, we mainly focused on reducing the leakage power of the SRAM cell. The sleepy stack achieved the significant effect on SRAM cell. The result shows that sleepy stack produce higher reduction in the leakage power.

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