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A Novel Field Effect Diode (Fed) Structure For Improvement Of I_{on}/I_{off} Ratio Parameter In The Nanometer Regime

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Abstract: *Field Effect Diode (FED)s are interesting devices in providing the higher ON-state current and lower OFF-state current in comparison with SOI-MOSFET structures with similar dimensions. For channel length shorter than 75nm, Short Channel Effects (SCEs) deteriorates the FEDs electrical characteristics. The impact of band-to-band tunneling (BTBT) on the OFF-state current of the Side contacted FED (S-FED) has been investigated in this paper. Simulation results show that for the 65nm channel length, the BTBT increases the OFF-state current of the S-FED device noticeably. For the first time in this paper, we introduce a novel FED structure in which the oxide layer in the channel has been used. This is the so-called Silicon On Raised Insulator FED (SORI-FED). The oxide layer suppresses the electron tunneling path from the valence band into the conduction band at the device channel depth. Hence, OFF-state characteristic of the SORI-FED device improves. For 65nm channel length, the simulation results show that the SORI-FED OFF-state current is eight orders of magnitude lower than OFF-state current in M-FED. Furthermore, the SORI-FED provides 35% reduction in gate delay in comparison with M-FED.*

Keywords: *Band-To-Band-Tunneling (BTBT), Field Effect Diode (FED), Modified FED (M-FED), Side contacted FED (S-FED), Silicon On Raied Insultor FED (SORI-FED)*

I. Introduction

As the technology progresses, Metal Oxide Semiconductor Feld Effect Transistor (MOSFET) device dimensions are aggressively scaled down to the nanometer regime. The aims of this scaling include achieving lower power consumption, higher speed and higher chip density. However, reduction of the channel length results in the leakage current increment and limits the scaling of the devices [1-4]. Several approaches have been used to reduce the OFF-state current in MOSFET devices [5-10]. Furthermore, to overcome the channel length scaling limitations, new device structures are required as an alternative structure to conventional MOSFET. One of these devices is the Field Effect Diode which its fabrication procedure is compatible with Complementary Metal Oxide Semiconductor (CMOS) processing [11-13]. The FED is a pin diode in which the potential in the intrinsic region is controlled by two gates over the channel. It provides ON-state current (I_{ON}) which is twice greater than that of corresponding SOI-MOSFET structure for channel length greater than 200nm and results in a decreased gate delay [12, 13]. However, the regular FED provides high OFF-state current for the channel length shorter than 75nm and the device could not be turned off [11-13]. To overcome this shortcoming Raissi et.al suggested a new structure, namely Modified FED (M-FED) [12-15]. In this structure, p^+ and n^+ reservoirs in the source and the drain in off mode causes hole injection to the sub-gate close to t source and electron injection to sub-gate close to the drain respectively. So an n^+pnp^+ structure will develop and the device will turn off. Manavizadeh et.al proposed another new structure, namely Side contacted FED (S-FED), which its fabrication process is simple in comparison with an M-FED [14, 15]. The S-FED operational principle is similar to the M-FED operational principle.

Although many researchers have studied the physical modeling of S-FED and M-FED devices [12-15], to the great extent, however, the effect of Band-To-Band Tunneling (BTBT) on their electrical characteristics has not yet been considered. For the first time in this paper, the S-FED device by taking BTBT into account has been simulated. Our numerical simulations show that the BTBT model affects the OFF-state characteristic of the S-FED device. Use of an oxide step in the channel has been proposed to suppress the electron tunneling from the valence band into the conduction band at the device channel depth. The proposed structure called Silicon On Raised Insulator FED (SORI-FED). Two figures of merit are compared to S-FED and SORI-FED for 65nm channel lengths. These figures of merit are gate delay time and the I_{ON}/I_{OFF} ratio parameters.

This paper is organized as follows: in Section 2 the structure and parameters employed for simulations are described. Section 3, explains the impact of the tunneling phenomena on the S-FED electrical characteristics. The new FED structure is presented in Section 4. Finally, we conclude this paper in Section 5.

II. The Device Structure and Simulation Method

The FED operation can be explained in terms of a pin diode in which the potential in the intrinsic region is controlled by two gates over the channel. The regular FED structure is shown in Fig.1 (a) with 30nm Gate1 length (Lg1), 30nm Gate2 length (Lg2) and 5nm spacing between two gates. The gate oxide thickness and device width are 2nm and 1μm, respectively. The source, the drain and the channel doping are equal to $1\times10^{21}cm^{-3}$, $1\times10^{14}cm^{-3}$, $1\times10^{21}cm^{-3}$, respectively. These values and other structural parameters are consistent with [11, 12]. The simulations are carried out by a commercial tool. In order to take the high doping concentration into account in the source and drain regions, Slotboom Band Gap Narrowing model is included. The Shockley-Read-Hall (SRH) model and Band-TO-Band-Tunneling (BTBT) model have been considered for estimation of the leakage currents [16, 17]. A Mobility Model which accounts for lattice scattering, impurity scattering and carrier-carrier scattering is employed. High electric field velocity saturation is also taken into account.

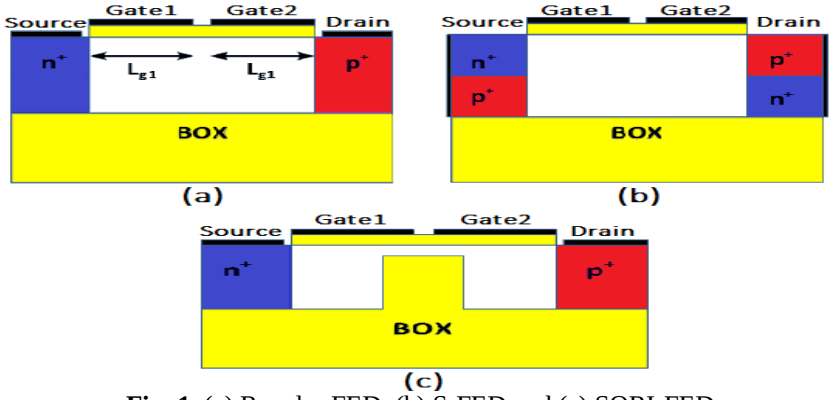

Fig. 1. (a) Regular FED, (b) S-FED and (c) SORI-FED.

III. Theoretical Background

The Fig.2 demonstrates the I-V characteristics of the regular FED device for the 65nm channel length (Lg1 + Lg2 + spacing between two gates). As seen, the regular FED device cannot be turned off. In fact, applying bias to Gate1 and Gate2 cannot modulate the barrier height at source/channel interface and drain/channel interface, respectively. Hence electron injection from the source into the channel, under Gate1, and hole injection from the drain into the channel, under Gate2, is increased. Therefore the channel converts into an intrinsic region and the device operates as a forward bias pin diode. Hence the device does not turn off. This problem has been addressed earlier by [12, 13] for channel length less than 75nm. To alleviate this problem the S-FED structure was suggested in [14]. In the S-FED structure in the off mode, p^+ and n^+ reservoirs in the source and the drain regions causes hole injection into the channel, under Gate1, and electron injection into the channel, under Gate2, respectively. So an n^+pnp^+ structure forms and the device turns off. In this section, we investigate the impact of BTBT phenomena on the electrical characteristics of the S-FED device in the nanometer regime. The S-FED device simulation in this section has a 65nm channel length and other structural parameters are consistent with [14].

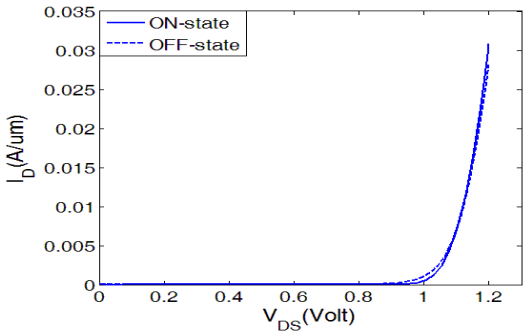

Fig. 2. I_D-V_{DS} characteristic of the regular FED device shown in Fig. 1(a) for 65nm channel length.

3.1. BTBT effect

The Simulation results show that BTBT model affects the OFF-state current of the S-FED device. To model the BTBT, we have used the field depended Kanes model [16, 17]. Figure 3(a) shows the I-V characteristic of 65nm channel length S-FED in the OFF-state. The OFF-state current simulated by taking BTBT into account is several orders higher compared with the OFF-state current when the BTBT is absent.

Figure 3(b) shows the electron-hole pairs generation rate by taking BTBT into account in the M-FED device. Figure 4(a) shows that there exists a band bending in the distance between two gates close to the device surface. Furthermore, the band diagram at distances greater than 25nm from the surface is different than that close to the device surface [Fig.4 (b)]. These band diagrams in the lateral direction of the device are very similar to the band diagram in a Zener diode. Band overlap between the valence band and the conduction band, at close to the surface and distances greater than 25nm from the surface, causes significant BTBT of electrons from the valence band into the conduction band in the lateral direction. Additional electron hole pairs generated with BTBT are contributed to the OFF-state current, thus, OFF-state current is increased.

IV. Results And Discussions

4.1. Silicon On Raised Insulator FED (SORI-FED) structure

We now intend to provide a novel nanoscale FED structure, namely SORI-FED for 65nm channel length in this section. The proposed structure has been shown in Fig. 1(c). The difference between this structure and the regular FED is the existence of a SiO2 physical barrier in the channel. Other device structural parameters are similar to those given for the device in Fig. 1(a). Oxide geometry in the channel can be optimized such that the SORI-FED provides higher I_{ON}/I_{OFF} ration in comparison with that of the S-FED. Simulation results show that oxide optimal height and oxide optimal width for 65nm channel length are 45nm and 35nm, respectively. Simulation results show that the oxide layer in the channel helps Gate1 and Gate2 to better control the barrier heights at the source/channel interface and drain/channel interface, respectively. Hence the SORI-FED device can be turned off for 65nm channel length.

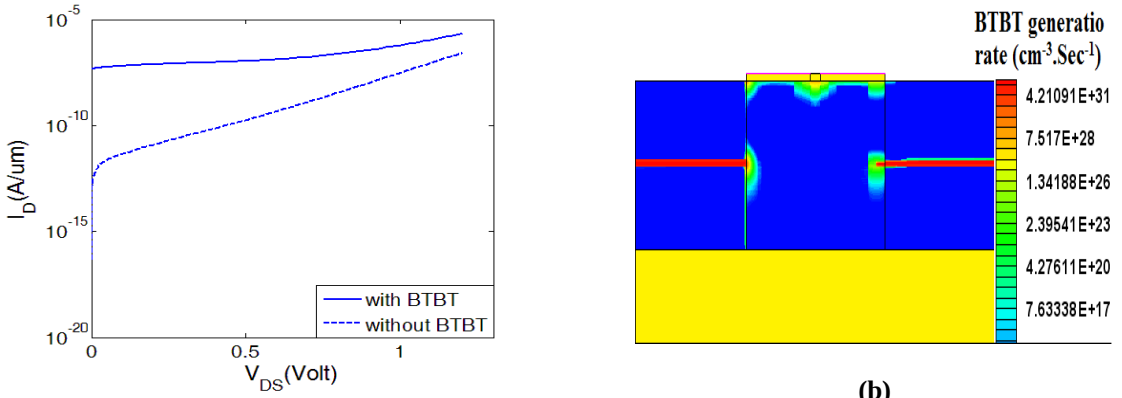

Fig. 3. (a) I_D–V_{DS} with BTBT model, (b) Two-dimensional contour for band-to-band generation rate across the S-FED device when the BTBT model is included for 65nm channel length.

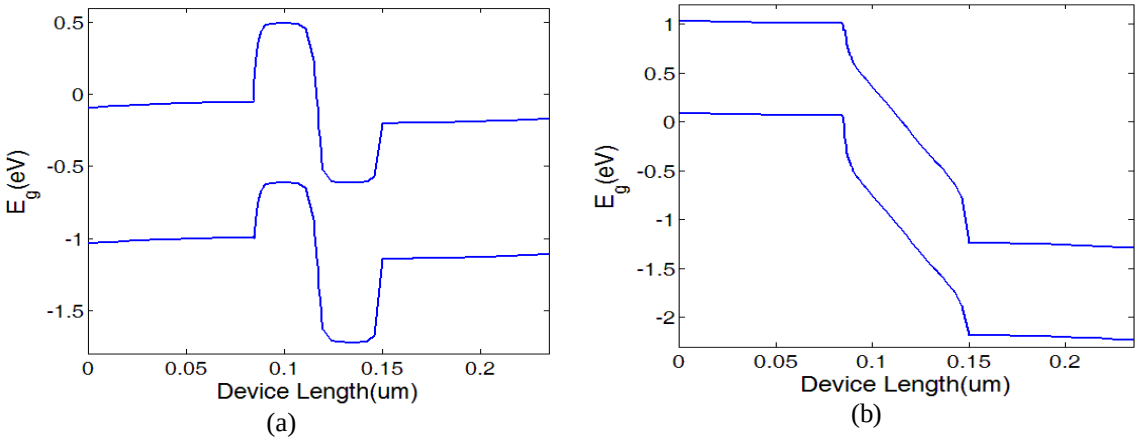

Fig. 4. Band diagram in lateral direction across the S-FED device at a distance of **(a)** 1 nm from the surface and **(b)** 27 nm from the surface.

4.2. Comparison between SORI-FED and S-FED

Fig. 5 compares the I-V characteristics of S-FED and SORI-FED device in the OFF-state by taking BTBT into account. As shown in the Fig. 5, OFF-state current of SORI-FED is eight orders of magnitude less than that of the S-FED. In fact, oxide layer in the channel results in the BTBT at the device depth eliminates.

Furthermore, SiO_2 barrier in the channel results in the large gates induced potential in the channel. Therefore, OFF-state current of SORI-FED, as compared with S-FED, is reduced. Table I compares the I_{ON}, I_{OFF}, I_{ON}/I_{OFF} ratio and gate delay parameters for SORI-FED and S-FED devices. The gate delay time of a transistor is defined in [18]. As seen in the Table I, the I_{ON}/I_{OFF} ratio of the SORI-FED is eight orders of magnitude greater than the I_{ON}/I_{OFF} ratio of the S-FED. This is attributed to that OFF-state current of SORI-FED device is less than OFF-state current of S-FED device, noticeably. Furthermore, SORI-FED provides less gate delay in comparison with S-FED. This is attributed to the fact that ON-state current of SORI-FED is more than ON-state current of S-FED.

Table1. Simulation results for 65nm channel length S-FED and SORI-FED devices.

	I_{ON}(mA)	I_{OFF}(mA)	I_{ON}/I_{OFF}	Gate delay(PSec)
SORI-FED	5mA	$3.8E10^{-11}$	$1.31E10^{11}$	0.11
S-FED	3.5mA	$2.23E10^{-3}$	$1.57E10^{3}$	0.17

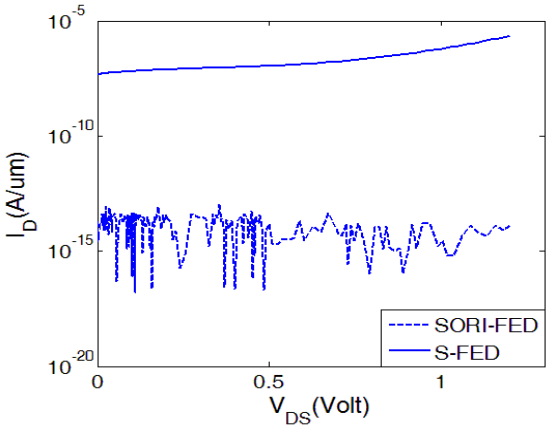

Fig. 5. I_D-V_{DS} characteristic by taking BTBT into account for 65nm channel length in the off mode.

V. Conclusion

For the channel lengths less than 75nm, regular FED does not turn off. To alleviate this problem S-FED device was suggested in [14]. It appears that in S-FED device physics has been reported in [14, 15] no BTBT has been taken into account. Simulation results in this paper show that the band diagram of the S-FED device for distances of greater than 25nm is similar to the band diagram of the Ziner diode. Hence electron tunneling from the valence band into the conduction band is formed. As a result, additional electron hole pairs are generated and contribute to the OFF-state current. Therefore, BTBT increases the OFF-state current of the S-FED device. Use of an oxide barrier in the channel has been proposed to suppress the BTBT in the device depth. Furthermore, the oxide barrier in the channel helps to apply biases to Gate1 and Gate2 raises the channel potential in SORI-FED. Hence Gate1 and Gate2 exert better control on the barrier at the source/channel or drain/channel interface and barrier height reduction is negligible in the off mode. Proposed structure provides less OFF-state current in comparison to the S-FED device. Our studies show that for 65nm channel length, I_{ON}/I_{OFF} ratio in SORI-FED device is three orders of magnitude greater than I_{ON}/I_{OFF} ratio in the S-FED device. More ON-state current in SORI-FED than S-FED leads to less delay of SORI-FED than S-FED. Low leakage current in SORI-FED structure reduces the device power consumption considerably.

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