

Design of Low Power Vlsi Circuits Using Cascode Logic Style

Revathi Loganathan¹, Deepika.P²,

Department of EST,

¹-Velalar College of Engineering & Technology, ²Nandha Engineering College, Erode, Tamilnadu, India
revathilogu15@gmail.com, deepikakarish@gmail.com

ABSTRACT: Due to the trade-off between power, area and performance, various efforts have been done. This work is also based to reduce the power dissipation of the vlsi circuits with the performance upto the acceptable level. The dominant term in a well designed vlsi circuit is the switching power and low-power design thus becomes the task of minimizing this switching power. So, to design a low-power vlsi circuit, it is preferable to use Non-clocked logic styles as they have less switching power. In this work various Non-clocked logic styles are compared by performing transistor level simulations for half adder circuit using TSMC 0.18 μm Technology and Eldo simulator of Mentor graphics.

Keywords— Low-power, Non-clocked logic style, Half adder, DCVS, DSL, CNTL.

I. INTRODUCTION

The need for low-power VLSI systems arises from two main forces. First, with the steady growth of processing capacity per chip, large current has to be delivered and the heat due to large power consumption must be removed by proper cooling techniques. Second, battery life in portable electronic devices is limited. Low-power design directly leads to prolonged operation time in these portable devices [1-2]. The increasing demand for low-power VLSI can be addressed at different design levels, such as the architectural, circuit, layout, and the process technology level [3]. The power can significant be reduced at the circuit design level by means of proper choice of a design style for implementing combinational circuits. This is because all the important parameters governing power dissipation- switching capacitance, transition activity and short circuit currents- are strongly influenced by the chosen logic style [4].

As opposed to the static gates, dynamic gates are clocked and work in two phases, a precharge and an evaluation phase. The logic function is realized in a single NMOS pull-down or NMOS pull-up network resulting in small input capacitances and fast evaluation times. This makes dynamic logic attractive for high speed applications. However, the large clock loads and the high signal transition activities due the pre-charging mechanism result in an excessive high power dissipation [4]. In contrast, non-clocked circuit families do not require logic preconditioning, nor do they segment the microprocessor's clock cycle into distinct "evaluate" or "precharge" periods. Rather, non-clocked circuits respond instantaneously to changes in their inputs. If inputs to a non-clocked circuit do not change, then its outputs do not toggle, assuring that low-activity-factor paths return lower non-switching power consumption [5].

II. SOURCES OF POWER DISSIPATION AND ITS REDUCTION

There are three major sources of power dissipation in digital CMOS circuits, which are summarized in the following equation:

$$P_{total} = \alpha C_L f_{clk} V_{DD}^2 + I_{SC} V_{DD} + I_{leakage} V_{DD} \quad (1)$$

The first term represents the switching component of power, where α is the switching factor, C_L is the loading capacitance, and f_{clk} is the clock frequency. The second term is due to the direct path short circuit current I_{SC} , which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground. Finally, the leakage current, which can arise from substrate injection and subthreshold effects, is primarily determined by fabrication technology considerations. The dominant term in a "well-designed" circuit is the switching component, and low-power design thus becomes the task of minimizing C_L, V_{DD} and f_{clk} , while retaining the required functionality [6]. Therefore, for low-power what we have to look out for is the switching power dissipation and techniques to reduce switching power dissipation. Some general logic style requirements for low-power circuit implementation are as follows:

1. Switched capacitance reduction:

Capacitive load, originating from transistor capacitances (gate and diffusion) and interconnect wiring, is to be minimized. This is achieved by having as few transistors and circuit nodes as possible, and by reducing transistor sizes to a minimum [6].

2. Supply voltage reduction:

A logic style providing fast logic gates to speed up critical signal paths allows a reduction of the supply voltage in order to achieve a given throughput. For that purpose, a logic style must be robust against supply voltage reduction [6].

3. Switching activity reduction:

At the circuit level, large differences are primarily observed between static and dynamic logic styles. Only minor transition activity variations are observed among different static logic styles [6].

4. Short circuit current reduction:

Short circuit currents (also known as dynamic leakage currents) may vary by a considerable amount between different logic styles. Their contribution to the overall power consumption is rather limited but not negligible (10-30 %), except for very low voltages (V_{DD}), where the short circuit currents disappear. A low-power design should have minimal short circuit current [6].

So, if we are looking out for low-power design, then it is preferable to use Non-clocked logic style as it assures low activity factor path returning lower switching power consumption.

III. NON CLOCKED LOGIC STYLES

Non clocked logic is ubiquitous in electronic design, due to a no. of considerations including:

Low power consumption
Straightforward delay rule timing
Inherent reliability and noise immunity
Process variation and defect tolerance
Migratability into successive technology generations [5].

Generally speaking, non clocked circuits are quite reliable. Nodes which determine the value of successive stages are never left to float, providing implicit noise immunity. Careful device size selection allows PFET/NFET device ratio tuning to achieve desired switch points and unity gain points for specific noise concerns. Because nodes are strongly held at all times in a complementary fashion, non clocked is especially forgiving to defects and process variation. Since control devices receive full gate voltage even after its capacitive load has been charged, the device remains inverted, and the current is readily available if needed to overcome the short circuit paths or leakage mechanisms caused by minor defects. High degree of tolerance enables the easy translation of a non clocked design into a successive generation of the technology [5]. Differential Cascode Voltage Switch (DCVS) is claimed to have advantages over the traditional static CMOS design in terms of circuit delay, layout area, logic flexibility, and power dissipation [7] [8]. DCVS also has an inherent self-testing property which can provide coverage for stuck-at and dynamic faults [9]. There are a number of non clocked DCVS variations, all employing the basic concept of using pairs of differential logic inputs to flip a static cross coupled device pair and store an output state [5]:

1. Differential Cascode Voltage Switch Logic (DCVSL)
2. Differential Split-Level Logic (DSL)
3. Cascode Non-Threshold Logic (CNTL)

1. Differential Cascode Voltage Switch Logic (DCVSL) :

DCVS has been found to offer a performance advantage of 4X compared to the CMOS/NMOS primitive NAND/NOR logic families, while maintaining the expected low-power characteristics of CMOS circuitry. Since the inputs drive only the NMOS tree devices, input gate capacitance loading is typically a factor of 3X smaller than CMOS circuits that require the complementary n-channel and p-channel devices to be driven [10]. A basic structure of AND logic using DCVS is shown in Fig. 1.

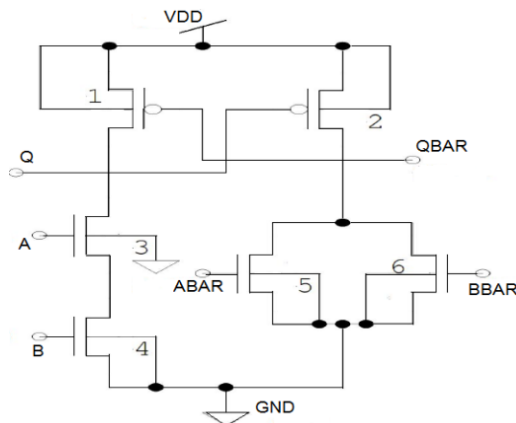


Fig. 1 AND Logic using DCVSL

TABLE I
 CHARACTERISTICS OF DCVSL [5]

Strengths	Weaknesses
Superior logic density	Dual rail wiring
Implicit invert available	Struggle between PMOS output strength and latch hysteresis
High reliability and noise immunity	Higher device count and in some applications

2. Differential Switch Logic (DSL) :

DSL is a circuit technique which allows, in any given technology, shorter channel length owing to a reduced drain-source voltage. This circuit logic is substantially different from DCVSL as there are two extra NMOS transistors placed between the PMOS part and the logic NMOS part. These gates are controlled by the reference voltage, which must be equal to half of supply voltage V_{DD} plus threshold voltage of the NMOS transistors to guarantee the optimum circuit operation [11].

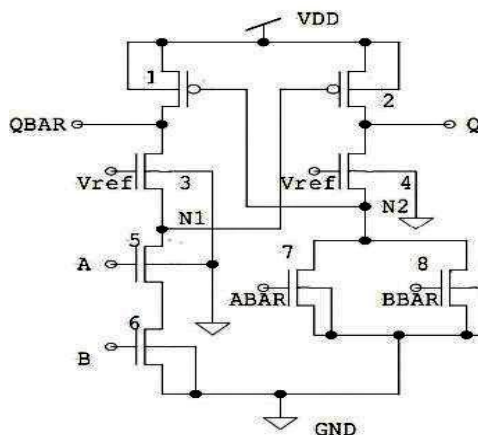


Fig. 2 AND Logic using DSL

DSL provides hastened transitions as the nodes N1 and N2 in Fig.2 need only to be discharged from $V_{DD}/2$ rather than V_{DD} . Since, the NMOS pull down device never sees drain voltage higher than $V_{DD}/2$, the channel hot-electron based performance degradation is minimized. It can argue that this enables the usage of technology with channels shorter than what would be expected for the given V_{DD} , realizing higher performance. The added resistance of the added reference device necessarily reduces the total possible tree height [5].

TABLE II
 CHARACTERISTICS OF DSL [5]

Strength	Weakness
Lower AC power	Higher standby current, power dissipation
Superior static performance High reliability	Reference Higher device count
Reduced channel hot-electron wearout	

3. Cascode Non-threshold Logic (CNTL):

CNTL improves upon DSL by not requiring a precision voltage reference. The devices which add additional voltage drop have their gates tied to or to a feedback node, instead of a reference. The negative feedback substantially reduces the power consumption of the NTL origin, but at the expense of some performance. The performance penalty is addressed with the shunt capacitor [12].

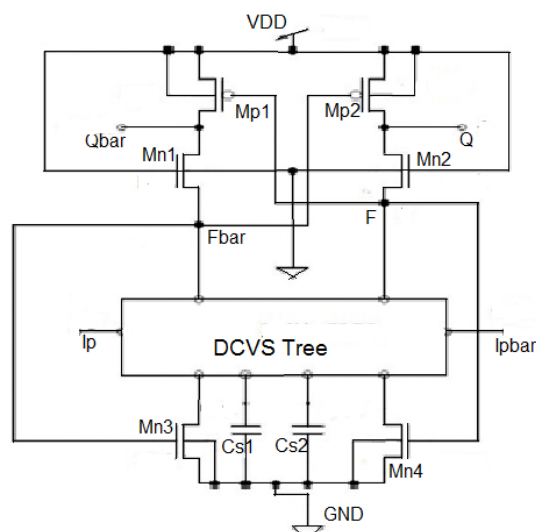


Fig. 3 Basic Structure of CNTL

TABLE III
 CHARACTERISTICS OF CNTL [5]

Strength	Weakness
Low power	Compromised performance
Heavy Load Drive Capability	Substantial area increase
Differential noise immunity	Shunting capacitance needed

IV. DESIGN AND SIMULATION RESULTS FOR VARIOUS LOGIC STYLES

In this work, Half-Adder circuits have been designed using different non-clocked logic styles and then the power is compared for these logic styles, so that the appropriate logic style among them can be used for low-power VLSI design. All the designs, in this work, have been done using standard TSMC 0.18 μm Technology, and simulations have been done using ELDO simulator of Mentor Graphics.

1. Half-Adder using DCVSL

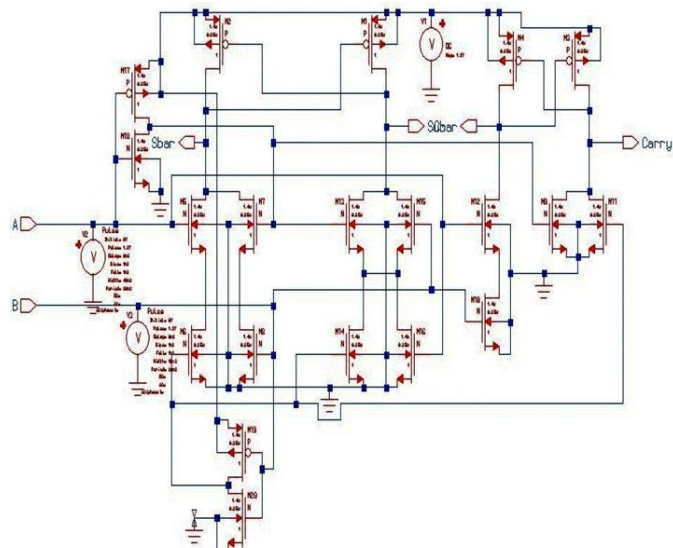


Fig. 4 Half-Adder circuit using DCVSL

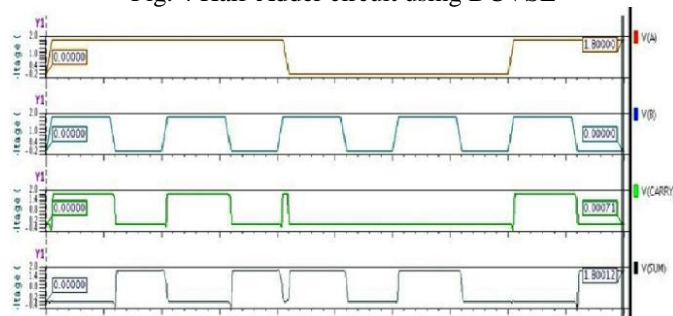


Fig. 5 Simulation result of transient analysis for Half-Adder using DCVSL

2. Half-Adder using DSL

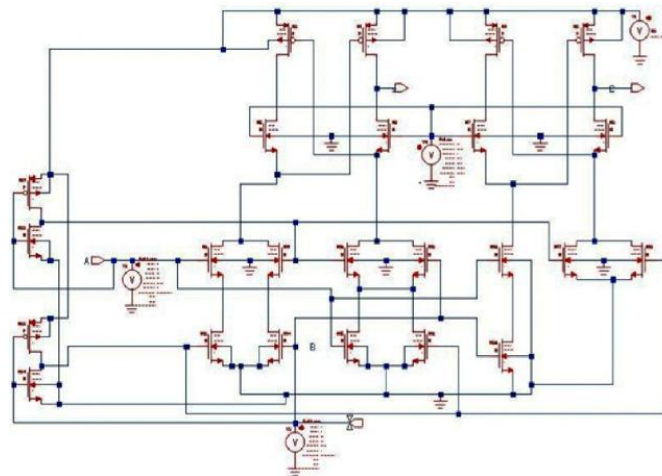


Fig. 6 Half-Adder circuit using DSL

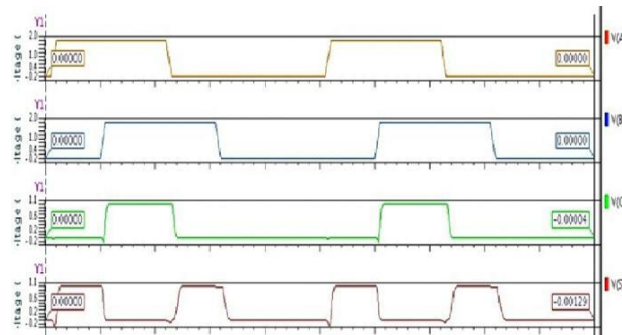


Fig. 7 Simulation result of transient analysis for Half-Adder using DSL

3. Half-Adder using CNTL

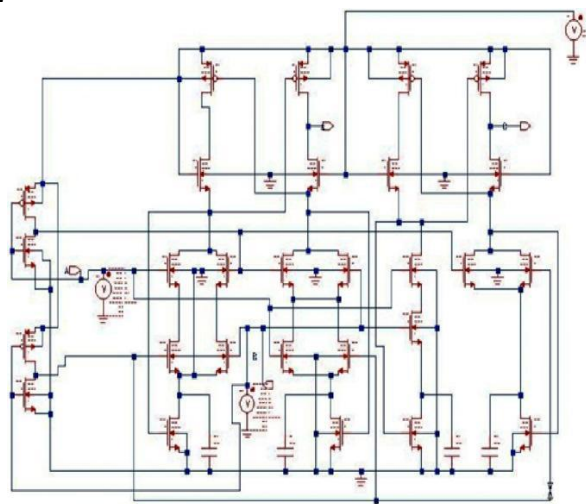


Fig. 8 Half-Adder circuit using CNTL

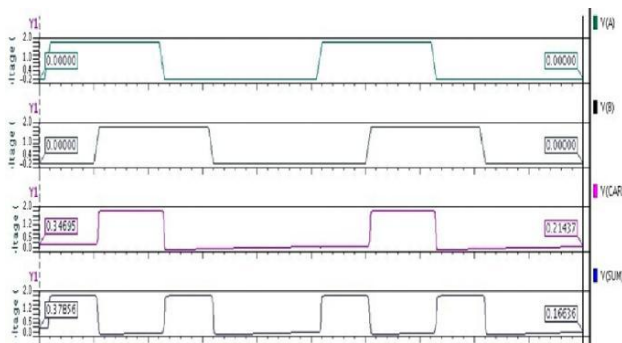


Fig. 9 Simulation result of transient analysis for Half-Adder using CNTL

TABLE IV
 POWER DISSIPATION IN HALF ADDER CIRCUIT FOR DIFFERENT LOGIC STYLES

Logic Style	Static Power(nW)	Dynamic Power
DCVS	92.29	92.72
DCS	40.70	55.12
CNTL	22.57	25.95

V. CONCLUSIONS

Non-clocked logic style provides a good opportunity to significantly reduce the power for different VLSI circuits. In this work, some of the non-clocked design styles (DCVSL, DSL and CNTL) have been compared, on the basis of power dissipation for half-adder circuit, and according to the results, it is found that CNTL is providing the minimum power dissipation among these logic styles. These non-clocked logic styles are preferred for high speed application. So, CNTL design style can be a great solution to provide high speed and low-power VLSI design.

REFERENCES

- [1] V. Sharma and S. Kumar, "Low-Power 1-bit CMOS Full Adder using Subthreshold Conduction Region," *International Journal of Scientific & Engineering Research*, vol. 2, June 2011.
- [2] S. Hanson, B. Zhai, K. Bernstein, D. Blaauw, A. Bryant, L. Chang, K. K. Das, W. Haensch, E. J. Nowak and D. Sylvester, "Ultra-Low Voltage, Minimum-Energy CMOS," *IBM Journal of Research and Development*, vol. 50, no. 4-5, pp. 469-490, 2006.
- [3] A. P. Chandrakasan and R. W. Brodersen, *Low Power Digital CMOS Design*, Kluwer Academic Publishers, 1995.
- [4] R. Zimmermann and W. Fichtner, "Low-Power Logic Styles: CMOS versus Pass-Transistor Logic," *IEEE Journal of Solid-State Circuits*, vol.32, no. 7, July 1997.
- [5] K. Bernstein, K. M. Carrig, C. M. Durham, P. R. Hansen, D. Hogenmiller, E. J. Nowak and N. J. Rohrer, *High Speed CMOS Design Styles*, Kluwer Academic Publishers, 2001.
- [6] A. P. Chandrakasan, S. Sheng and R. W. Brodersen, "Low-Power CMOS Digital Design," *IEEE Journal of Solid State Circuits*, vol. 27, no. 4, pp. 473-484, April 1999.
- [7] K. M. Chu and D. I. Pulfrey, "A Comparison of CMOS Circuit Techniques: Differential Cascode Voltage Switch Logic versus Conventional Logic," *IEEE Journal of Solid State Circuits*, vol. SC-22, pp. 528-532, 1987.
- [8] K. M. Chu and D. I. Pulfrey, "Design Procedures for Differential Cascode Voltage Switch Circuits," *IEEE Journal of Solid State Circuits*, vol. SC-21, pp. 1082-1087, 1986.
- [9] R. K. Montoye, "Testing Scheme for Differential Cascode Voltage Switch Circuits," *IBM Tech. Disc. Bull.*, vol. 27, pp. 6148-6152, 1985.
- [10] L. G. Heller, "Cascode Voltage Switch Logic: A Differential CMOS Logic Family," in *proceedings of IEEE International Solid State Circuit Conference*, pp. 16-17, 1984.
- [11] L. Pfenning, "Differential Split Level CMOS Logic for Subnanosecnds Speed," *IEEE Journal of Solid State Circuits*, vol. SC-20, no. 5, October 1985.
- [12] J. S. Wang, "CMOS Non-Threshold Logic (NTL) and Cascode Non-Threshold Logic (CNTL) for High-Speed Applications," *IEEE Journal of Solid State Circuits*, vol. 24, no. 3, pp. 779-786, June 1989.