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Implementation of Efficient Adaptive Noise Canceller using Least Mean Square Algorithm

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***Abstract*:** *The digital signal processing has contributed in solving problems such as constructive interference, electrical echo, environmental noise, atmospheric noise, etc.Adaptive filters can be used to solve such problems. Nowadays FPGA systems are replacing dedicated programmable digital signal processor (PDSP) system due to their flexibility and large bandwidth, resulting from their parallel architecture. This paper presents implementation of adaptive noise canceller for cancelling noise signals present in speech signal. Least mean square algorithm is used for adaption of filter coefficients. The adaptive noise cancellation system is implemented in VHDL and tested for cancelling noise in speech signals. The simulation results of VHDL designed digital adaptive filter is performed and analyzed on basis of signal to noise ratio (SNR), Mean square error (MSE) convergence speed and tracking ability.*

***Keywords*:** *Adaptive filtering, LMS algorithm, Noise cancellation, VHDL Design, Signal to noise ratio (SNR), Convergence Speed.*

I. INTRODUCTION

Digital signal processing, which spans a wide variety of application areas including speech and image processing, communications, networks, and so on, is becoming increasingly important in our daily life. Digital signal processing applications impose considerable constraints on area, power dissipation, speed and cost. Thus the design tool should be carefully chosen. . The most commonly used tools for the design of signal processing systems are: Application Specific Integrated Circuit (ASIC), Digital Signal Processors (DSP) and FPGA. DSP is well suited to extremely complex math-intensive tasks, but cannot process high sampling rate applications due to its serial architecture. ASIC can meet all the constraints of digital signal processing, however, it lacks flexibility and requires long design cycle. FPGA can make up the disadvantages of ASIC and DSP. With flexibility, time-to-market, risk-mitigation and lower system costs advantages, FPGA has become the first choice for many digital circuits' designers. The digital signal processing applications impose considerable constrains on area, power dissipation, speed and cost. Thus the design tool should be carefully chosen. The most common tools for the design of such application are ASIC, DSP and FPGA. The DSP used for extremely complex math-intensive tasks but can't process high sampling rate applications due to its serial architecture. Whereas ASIC faces lack of flexibility and require long design cycle. The FPGA (Field programmable Gate Array) can make up disadvantages of ASIC and DSP. Hence FPGA has become the best choice for the design of signal processing system due to their greater flexibility and higher bandwidth, resulting from their parallel architecture. FPGA system for real time audio processing systems. In recent years, acoustic noises become more evident due to wide spread use of industrial equipments. An Active (also called as Adaptive) noise cancellation (ANC) is a technique that effectively attenuates low frequencies unwanted noise where as passive methods are either ineffective or tends to be very expensive or bulky. An ANC system is based on a destructive interference of an anti-noise, which have equal amplitude and opposite phase replica of primary unwanted noise. Following the superposition principle, the result is noise free original sound. ANC systems are distinguished by their different goals that lead to different architectures. If all ambient sound shall be reduced, a feedback system with its simpler architecture may be used. If, as in our case, single sources of unwanted sound shall be compensated, a feed forward system is required. A feed forward system as shown in fig. 1 is characterized by two audio inputs per channel: one reference signal input for the sound to be removed, and second error input for the sound after the compensation.

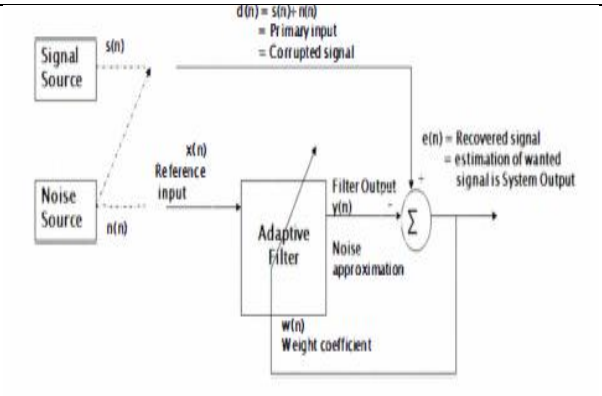

Figure 1. Adaptive Noise Canceller

An adaptive FIR feed forward system is shown in simple way. For the selective cancellation of disturbing noise without affecting other sounds. [2] It is dual input system. The first inputs is primary signal d(n)) which is wanted signal (say s(n)) corrupted by noise (say n(n)). The second input is reference signal x (n) can be interfacing noise supposed to be uncorre1ated with the wanted signal but correlated with noise affecting original signal in an unknown way. The filter output signal yen) is an estimate of the noise signal with inverted sign. This signal and the primary signal are superposed, so that the noise signal is cancelled and error signal e(n) is the result of this superposition which constitutes the overall system output. The adaptive filtering operation achieved the best results when system output is noise free. This goal is achieved by minimizing the mean square of the error signal [3]. The widely preferred LMS algorithm is used for the adaption of the filter coefficients.

II. LMS ALGORITHM

The LMS algorithm is a widely used algorithm for adaptive filtering. The algorithm is described by the following equations:

$$y(n) = wi(n) * x(n-i) \quad (1)$$
$$e(n) = d(n) - y(n) \quad (2)$$
$$wi(n+1) = wi(n) + 2ue(n)x(n-i) \quad (3)$$

In these equations, the tap inputs x (n), x (n-1),……, x (n-M+1) form the elements of the reference signal x(n), where M-1 is the number of delay elements. d (n) denotes the primary input signal, e(n) denotes the error signal and constitutes the overall system output. **w**i (n) denotes the tap weight at the nth iteration. In equation (3), the tap weights update in accordance with the estimation error. And the scaling factor u is the step-size parameter. u controls the stability and convergence speed of the LMS algorithm. The LMS algorithm is convergent in the mean square if and only if u satisfies the condition:

$0 < u < 1/$ tap input power

Least Mean Squares (LMS), one of the widely used algorithms in many signals processing environment, is implemented for adaption of the filter coefficients. The cancellation system is implemented in VHDL and tested for noise cancellation in speech signal.

1.1 Mathematical Treatment

Consider the transversal filter with input x (n) i.e. vector of the M (filter length) most recent input samples at sampling point n.

$$x(n) = [x(n), x(n-1), \ldots x(n-M+1)] \quad (1)$$

and w (n) i.e. vector of filter coefficients as

$$w(n) = [w_0(n), w_1(n), \ldots w(M-1)(n)] \quad (2)$$

At some discrete time n, the filter produces an output yen) which is linear convolution sum given by

$$y(n) = \sum_{k=0}^{m-1} w(n)x(n-k) \quad (3)$$

Also can be represent in vector form as

$$Y(n) = w^{T}(n)\, x(n) \quad (4)$$

The error signal is difference of this output with the primary signal d (n) given by,

$$E(n) = d(n) - x(n) \quad (5)$$

And by squaring error we get

$$e2(n) = d2(n) - 2d(n)xT(n)w(n) + WI(n)x(n)xT(n)w(n) \quad (6)$$

Where E denotes the statistical expectation operator. Applying the operator V to the cost function J, a gradient vector V J obtain as

$$V'J(n) = -2P + 2Rw(n) \quad (7)$$

$$= -2x(n)\, d(n) + 2x(n)\, xT(n)\, w(n) \quad (8)$$

This is a mathematical statement of unconstrained optimization.
Starting with w (O), generate a sequence of weight
vector w (1), w (2) . . . , such that the cost function J (w) is reduced at each iteration of the algorithm therefore

$$J(w(n+1)) < J(w(n)) \quad (9)$$

Where w (n) is the old value of the weight vector and w (n+ 1) is its updated value Substituting the estimate of equation 7 for the gradient vector V' J (n) III the steepest-descent algorithm, a new recursive relation obtain for updating the weight vector as.

$$W(n+1) = w(n) + \mu x(n)\, e(n) \quad (10)$$

A scaling factor 1.1 introduced here is step size parameter used to control the step width of the iteration and thus the stability and convergence speed of the algorithm [4, 5].
The LMS algorithm is convergent in mean square if and only if satisfies the condition.

$$0<\mu<\frac{1}{(M\,P)}$$

Where, P is the average power of tap input and M is Filter length.

III. VHDL IMPLEMENTATION OF SYSTEM

The VHDL design of the system is as shown figure. Arithmetic is modelled with Q format number representation which provides for each pipeline stage an appropriate number of guard bits for representing the integer part and avoiding overflow effects.

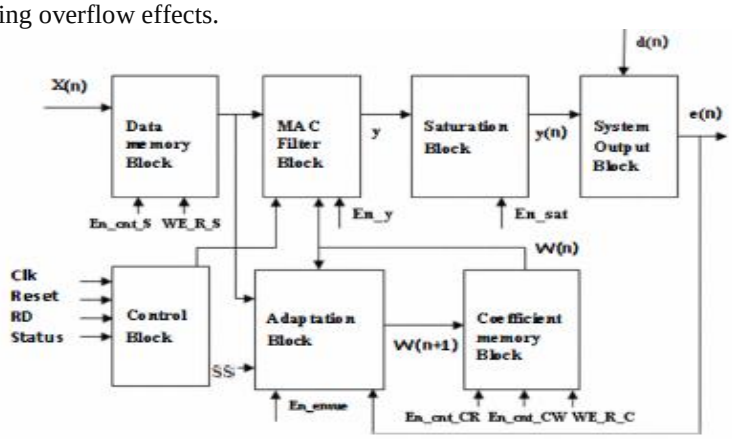

Figure 2. VLSI Design of Adaptive filter

The design splits into seven blocks as follows:
Data Memory block: The single port RAM is designed for storage of the audio samples.

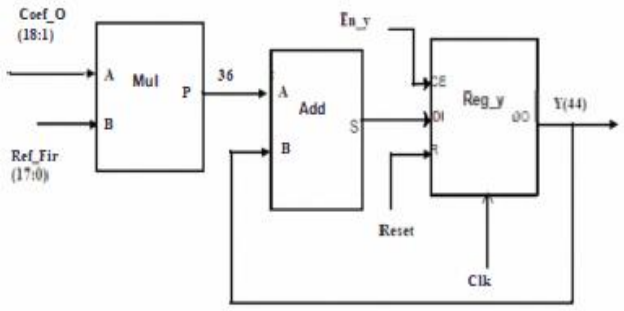

Figure 3. FIR Filter Block

maximum data path length short, The filter is implemented as a sequential MAC unit which performs M accumulations of products during every sample period so that a resource sharing can be utilized. Since the audio sample period fs provides a large amount of available clock cycles per audio sample, no parallel structure with M multipliers and M-1 adders is necessary. This block is designed as three-stage pipeline for the filtering cycle The input samples read from the data RAM block are multiplied with their corresponding filter coefficient taken from the dual-ported Coefficient RAM block and stored in the accumulator.

Saturation Block: The filter output signal is fed to the saturation block, which prevents the filter output from overflow and inverts the sign of the output signal to provide the phase shift for the compensation step.

System output block: The Adder unit is used to implement equation of error signal e(n) from saturation block output y(n) and primary signal d(n). This output is the required system output.

Adaption Block algorithm: A four-stage pipeline structure designed for the adaptation of the coefficients. The coefficient is calculated by a product of the input sample (Ref_Fir), the error signal (Err) and Step size parameter (SS). A register is inserted to this path that splits the arithmetic chain for achieving a shorter signal delay so that a clock frequency of fCLK = 50MHz can be met.

Coefficients Memory block: This block designed for storage of the current filter coefficients. The dual port RAM is chosen to support a parallel processing of the coefficient update block and the FIR Filter block. With two address inputs the reading address of the coefficients and the address for writing back the updated coefficients can be incremented within two interleaved clock periods.

Control Block: The Control path functionality is implemented as the Finite state machine (FSM). The FSM controls the processing of the two parallel pipelined data paths. The state diagram of the FSM shown figure describes

MAC Filter Block: The FIR filter design is based on the transposed direct form in order to keep the

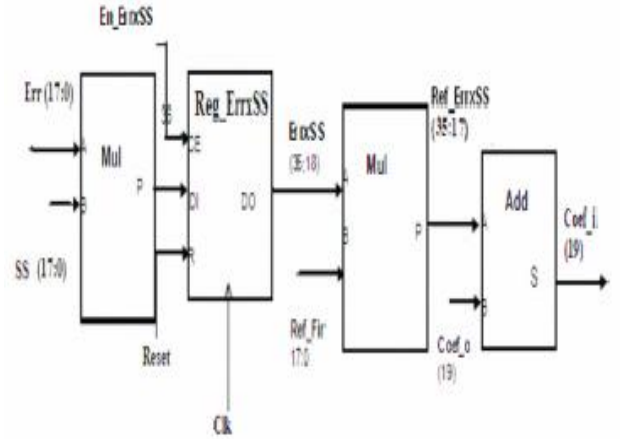

Figure 4. Co-efficient Adaptation Unit

The FSM will go through the following sequence:

START: This is default state in which all registers clears results from the previous calculation cycle. Through an input RD, a new sample XN is stored in RAM by the signal.

ERRXSS: performs calculation of the product of error signal Err and step size factor SS and stored in the register Reg_ ErrxSS by the signal ERRXSS: performs calculation of the product of error signal Err and step size factor SS and stored in the register Reg_ErrxSS by the signal En_Errxss.

FILTER / ADAPT: There is alternating Sequence of two pipeline operations runs in parallel. The filter block performs operations of updating address for reading input sample and coefficient, outputting memory and accumulating product of sample and Coefficient and saving in Register Reg_Y by the signal En _Y. The pipeline for the adaptation of the coefficients performs operations of updating address for reading input sample and coefficient, outputting memory, updating address for writing, Accumulation of a product from Ref_Fir and ErrxSS on the current coefficient and storage of the adapted coefficient. The status Cnt_st indicates the highest reading at the address is coefficient present at dual port RAM.
STOP: It is the last multiplication of sample and coefficient and accumulation of the result by the signal En _ Y. Then read address of coefficient from memory for the transition to a next state.
UPDATE: The accumulation result (filter Output) stored in the output register by the signal. En _sat and fed to the saturation block, which holds this value for one sample period and performs the adjustment of the RAM address counters for the next sequence.
RESET: When system is reset, state becomes reset to reset all registers and content of RAMs.

Table 1. Performance analysis

Sr.No	SNR (db)of original noise signal	SNR(db) of denoised signal	Mean Square Error
1	4.1731	33.7733	2.7684 E_005
2	13.0461	34.2360	2.0341 E_004
3	13.4070	28.9671	1.9350 E_004

IV. SIMULATION AND RESULT

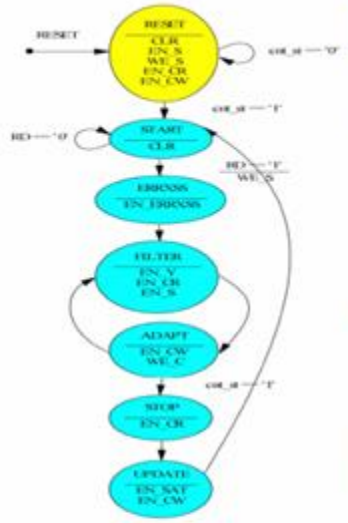

Figure 5. State Diagram of FSM of Adaptive filter.

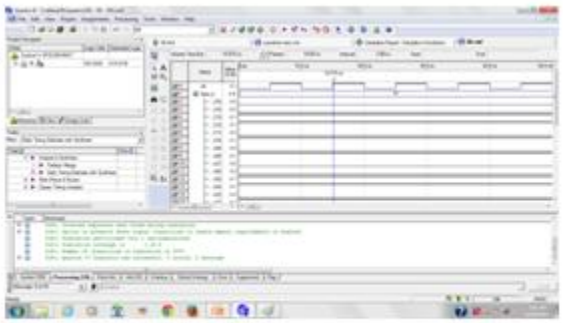

Figure 6. Simulation Waveform

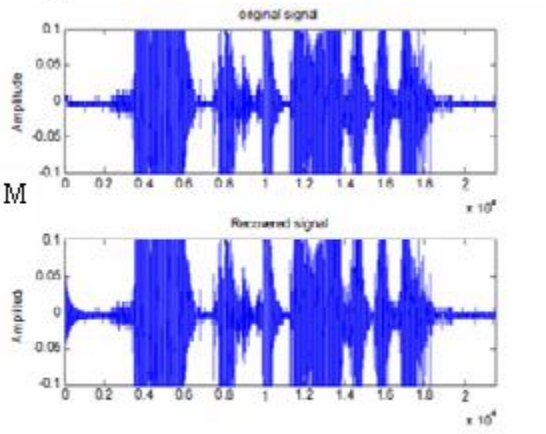

Figure 6. Original and Recovered Signal

V. CONCLUSIONS

The FPGA platform is well suited for the complex real time signal processing. An adaptive noise canceller has successfully been implemented. When tested with different signals the system showed improved performance compared to original signal. For future work, we planned to implement this system with LMS algorithm and try to remove noise from source signal and converge rapidly with lower complexity.

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