

Design of High Speed Reconfigurable Coprocessor for Multiplier/Adder and Subtractions Operations

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Abstract: As the quantity of data transmission and reception increases, there is a gradual increase in bandwidth on demand and quality of service. This further increases data traffic which leads to loss of information, reduced accuracy and reliability. To overcome this drawback, we proposed coprocessor can be used for communication operations, such as scrambling, interleaving, convolutional encoding, viterbi decoding, FFT, and several other functions using the proposed design. The coprocessor has been modeled by VHDL. Performance comparisons shows that the number of clock cycles can be reduced about 48% for scrambling and 84% for convolutional encoding compared with existing DSPs. From the results, performance of proposed coprocessor is better than conventional DSP (SC140) in terms of number of clock per cycle and gate counts.

Keywords: scrambling, convolutional encoding, interleaving, modulation, viterbi decoding, FFT.

I. INTRODUCTION

The recent communication system uses more complicated standards for communication services, which resulted in number of competing and incompatible standards. There are some standards are include like FHSS (Frequency-Hopping Spread Spectrum) [1] DSSS (Direct-Sequence Spread Spectrum) [2] DAB (Digital Audio Broadcast) [3] OFDM (Orthogonal frequency-division multiplexing) OSHA's Hazard Communication Standard (HCS) [4], CSMA(Carrier Sense Multiple Access)[5], DVB(Digital video broadcast), ADSL++ (Asymmetric Digital Subscriber Line plus) is a flexible communication system that supports multimedia broadcast and multi-band programmable processor and several other functions each are perform similar operation in various standards that are having different characteristics according to the standards. As a result, some of the flexible processors are developed which produces a solution that are more attractive than the above said methods. This paper proposes a Reconfigurable Coprocessor for Multiplier/Adder and Subtractions Operations .this is highly reliable, more accurate and also has less delay better performance than existing general Multiply, Add, and Subtract operations .this design has been modelled by using VHDL code, model-sim and evaluated performance and comparisons with existing DSP chip. This paper organized as follows .Section 2 communication system. Section 3 proposed Reconfigurable structure for Multiplier/Adder and Subtractions Operations. Section 4 Comparisons. Section 5 Results and Screenshots. Section 6. Conclusion.

II. Communication System

In basic communication systems, the baseband data may be human voice ,television picture, teletype data, atmospheric temperature and pressure etc at transmitted side first scrambled with a PN sequence (source coding) the scrambling data than coded with a convolutional encoder (channel coding). The punctured output of the convolutional encoder output is given to interleaved, modulated after this the coded data is transmitted. In the receiver side, the opposite operations are performed.

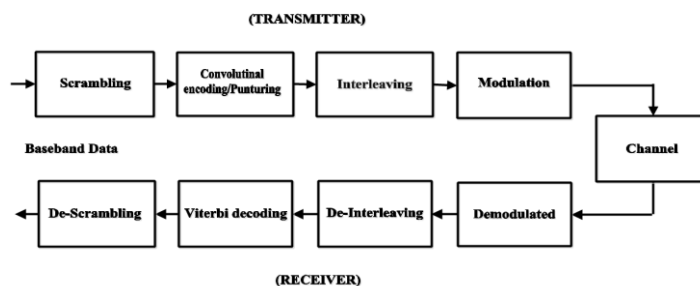


Figure.1. Commutation System

Figure 1 shows a brief illustration of communication systems. Channel coding performs scrambling, convolutional encoding, turbo encoding Reed-Solomon encoding, interleaving, etc. Modulation may use one of schemes, such as Quadrature Phase Shift Keying (QPSK), Quadrature Amplitude Modulation (QAM), offset QPSK (OQPSK) and OFDM(orthogonal frequency division multiplexer) etc. FFT (Fast Fourier transformer) and IFFT (Inverse Fast Fourier Transform) both are used to OFDM. These functional blocks have different

parameters and characteristics according to the standards, but they have similar basic operations. According to the operations of communication systems can be classified into three basic operations [1].

2.1 Block diagram description

The communication system consists of the following functional components Scrambling, Convolutional encoding/puncturing, Interleaving, Modulation, Channel, Demodulation, De-interleaving, Viterbi Decoding, Descrambling.

2.1.1 Scrambling and de-scrambling

The Scrambling is a process of adding new components to the original signal or the changing of some important component to the original signal in order to make extraction of the original signal difficult to the un-authorization person [6] as shown in Figure 2. The scrambler further classified as time domain scrambling, frequency domain scrambling variable-band scrambling, additive (synchronous) scramblers and multiplicative (self-synchronizing) scramblers. Figure 2 shows example of additive scrambling and additive de-scrambling with polynomial $=1+X^5+X^7$.

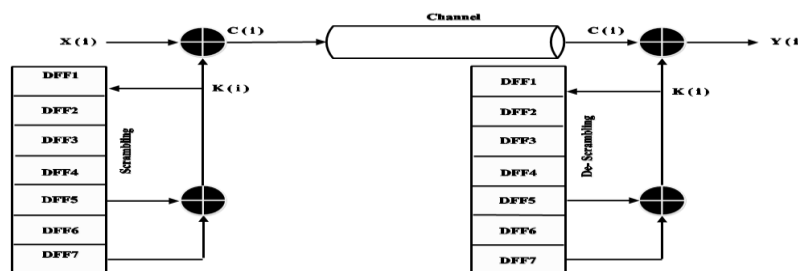


Figure.2. Scrambling and De-scrambling

Its characteristics polynomial is $1+X^5+X^7$ because the polynomial function is performed by the output of register 5 and 8 and repeats its sequence after $2^N-1=128$. In this operation performed by the help of linear feedback shift register in additional modulo-2 adder (XOR gate), where polynomial degree is represents by N , X(i) represents the data to be scrambled (at time i), scrambled codeword is represents by C(i), and the “key” produced by the linear feedback shift register is represents by K(i). The original data X(i) can be shown as follows $C(i) = X(i) + K(i)$. Because $K(i) = K(i-5) \text{ XOR } K(i-7)$, $C(i) = X(i) \text{ XOR } K(i-7)$ results. At the descrambling $Y(i) = C(i) \text{ XOR } K(i)$ is computed. Assuming that the two function are synchronized, $Y(i) = C(i) \text{ XOR } K(i-5) \text{ XOR } K(i-7)$ results, hence $Y(i) = X(i) \text{ XOR } K(i-5) \text{ XOR } K(i-7) \text{ XOR } K(i-5) \text{ XOR } K(i-7) = X(i)$.

2.1.2 Convolutional encoding

The Convolutional codes are used for communication system in numerous applications in order to achieve good performance with low implementation cost, high accurate, reliable data transfer, including digital video, radio, mobile communication, and satellite communication. They operate on data stream, not static block [7]. To convolutional encode data, used to converts binary data to data streams that helpful to high accurate data transmission start with k memory registers, initially all k memory registers are contain an assign with zeros. After the input applied by user to k memory registers then value changes to input bits. The convolutional encoder has ‘n’ modulo-2 adders (modulo 2 adders can be implemented with a single boolean XOR gate and ‘n’ generator polynomials one for each adder shown in Figure 3). First applied an input bit m_1 to the leftmost register by the help of generator polynomials and already existing registers values, the encoder outputs ‘n’ bits, now bit shift all register values to the right (m_1 moves to m_0 , m_0 moves to m_{-1}) and wait for the next input bit is applied. If there are no remaining input bits is applied to convolutional encoder, the encoder continues produced output until all registers have returned to the zero initials state. The Figure 3 is a rate 1/3 (S/T) encoder with constraint length (k) of 3. Generator polynomials are $X_1 = (1, 1, 1)$, $X_2 = (0, 1, 1)$, and $X_3 = (1, 0, 1)$. Therefore, output bits are calculated (modulo 2) as follows: $T_1 = S_1 + S_0 + S_{-1}$, $T_2 = S_0 + S_{-1}$, $T_3 = S_1 + S_{-1}$ [8].

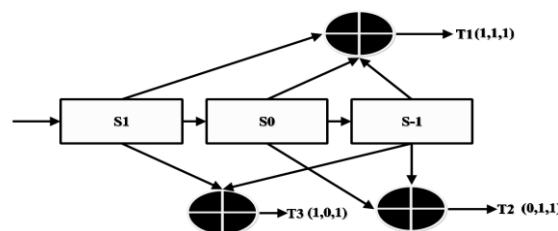


Figure.3. Convolution Encoding

2.1.3 Interleaving and De-interleaving

The interleaver arranged in the form of two-dimensional array, the data is read in along its row wise. Once the array is full, same data is read out along its column wise, thus changing the order of the data. (The interleaver process is denoted by the Greek letter π and de-interleaver process is denoted by π^{-1} .) The interleaver process is illustrated in Figure 4 the original data order can be restored by a corresponding de-interleaver process. The de-interleaver arranged in the form of two-dimensional array, the data is read in along its column wise and read out by row wise. This interleaver may be present between the outer encoder and inner encoder at transmitter side there is two component codes uses a concatenated code .the de-interleaver between the inner decoder and outer decoder at receiver side, as shown in Figure 4. Due this process the changing of some order of original data in order to interleaver arranged in the form of two-dimensional array, the data is read in along its row wise. Once the array is full, same data is read out along its column wise, thus changing the order of the data. (The interleaver process is denoted by the Greek letter π and de-interleaver process is denoted by π^{-1} .)

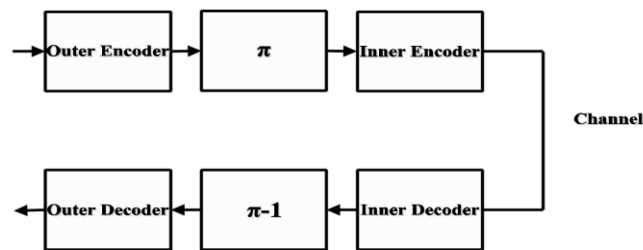


Figure.4. Concatenated code Encoder and Decoder with Interleaver

The interleaver process is illustrated in Figure 4 the original data order can be restored by a corresponding de-interleaver process. The de-interleaver arranged in the form of two-dimensional array, the data is read in along its column wise and read out by row wise. This interleaver may be present between the outer encoder and inner encoder at transmitter side there is two component codes uses a concatenated code .the de-interleaver between the inner decoder and outer decoder at receiver side, as shown in Figure 4, due to this process the changing of some order of original data in order to make extraction of the original signal difficult to the un-authorization person this process shown in Figure 5.

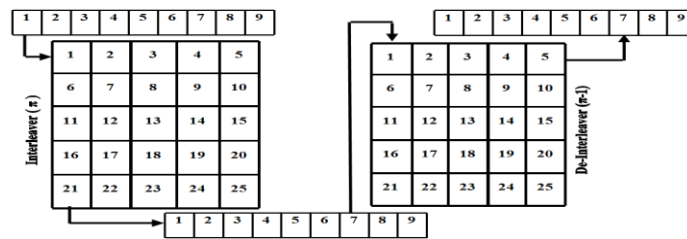


Figure.5. Operations of Interleaver and De-Interleaver

2.1.4 Modulation and De-modulation

In a communication system, the transmitter modifies the message signal into a form suitable for transmission over the channel, by using a process known as modulation. Modulation is defined as the process by which changing some characteristics of a high frequency sine wave called carrier signal. The carrier signal is varied with respect to the instantaneous amplitude of the message signal called the modulating signal. Demodulation is a process of extracting the original signal from a modulated carrier wave using an envelop detector circuit. Modulation and De-modulation process is very important for communication system there are many other modulation process is used for communication operation like such as Quadrature Phase Shift Keying (QPSK), Quadrature Amplitude Modulation (QAM), Offset QPSK (OQPSK) and OFDM (orthogonal frequency division multiplexer) this process useful to transmits signal for long distance and receive the accurate information.

2.1.5 Channel

The channel is a medium through which signal is sent from one place to another place. The different channels are used or selected in digital communication is based on the following parameter like, bandwidth, power, amplitude and phase requirement at the output, Linear and non-linear characteristics requirement, Effect of external interference on the channel. In this communication system we are using optical fiber channel it consists of a very fine inner core of silica glass surrounded by a concentric layer called cladding that is made up of glass. The glass in the core has a higher refractive index (RI) than that of the glass in the cladding. Optical

fiber channel work on the principle of total internal reflection. They are free from external electrical interference. Optical fiber channel has wide bandwidth and longer repeater separations, here we are using Optical fiber channel following characteristics like frequency range (10^{14} to 10^{15} Hz), maximum repeater spacing (2km), and effect of external noise (minimum).

2.1.6 Viterbi decoder

The Viterbi algorithm is used in a most of the communications system and also for data storage applications. It is commonly used for decoding convolutional codes, in detection of recorded data in magnetic disk drives and also for in baseband information detection for wireless systems.

III. Reconfigurable structure for communication systems

The operations of communication systems can be classified into three basic operations

- Multiply, Add, and Subtract operations
- Shift and logical operations
- Bit manipulation operations

These sections proposes a reconfigurable structure and performs of basic multiply, add and subtract operations and shows comparison of both general multiply, add and subtract operation and proposed multiply, add and subtract operation.

3.1 Multiply, Add, and Subtract operations

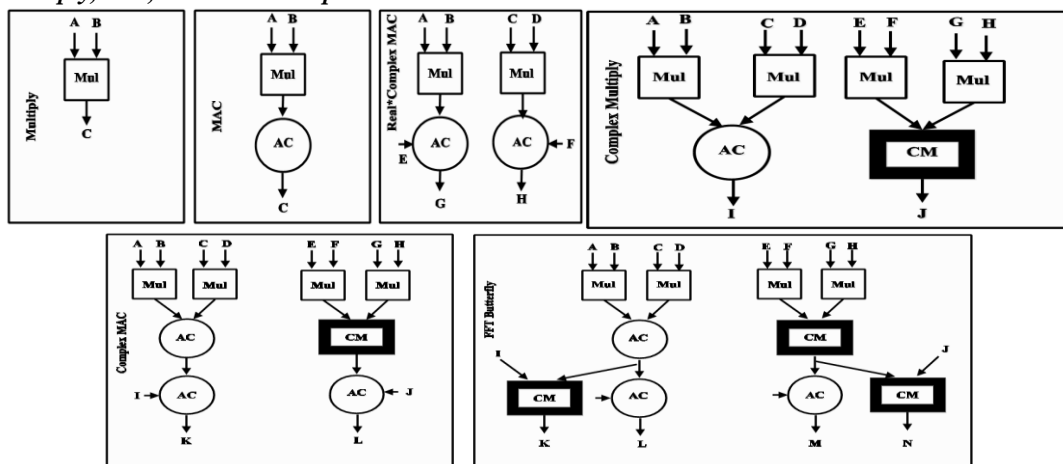


Figure.6. General Operations Based On multiply, MAC, real*complex MAC, complex MAC, complex multiply and FFT butterfly

Convolution Finite Impulse Response filter (FIR), Discrete Cosine Transform (DCT), vector operation, adaptive filter, synchronization, viterbi decoding, correlation, Turbo decoding, FFT several other operation can be performed by the help of add/subtract/ multiply operations. [11] multiply/add operations are used for filtering, FFT, correlation and synchronization, add/subtract/compare operations are used for turbo decoding and viterbi decoding, Figure.6 the General Operations Based On multiply, MAC, real*complex MAC, complex MAC, complex multiply and FFT butterfly. An FFT butterfly requires add operations and intensive multiply. Therefore, the proposed structure employs four 16 bit multipliers and six 32 bit adders/sub tractors that can support the operation of an FFT butterfly. Figure 7 shows the proposed multiplier/adder/subtractor architecture that can support the operations shown in Figure 6.

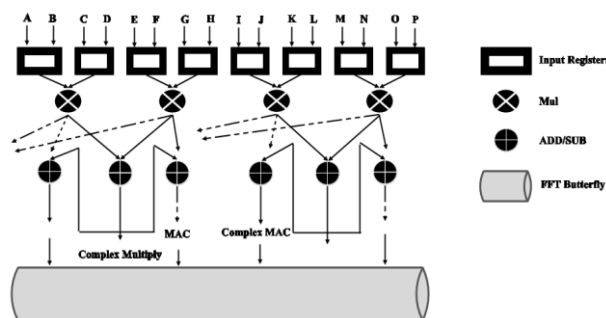


Figure .7 Proposed Multiplier/Adder/subtractor architecture

The adder/subtractor in Figure 7 can support one 32 bit operation for FFT, multiply and accumulate, etc. and two 16 bit operations for branch metric, path metric, etc.

3.2 Additions and subtractions using the proposed structure

The various additions and subtractions using the proposed structure show in Figure 8, Figure 8.1 and Figure 8.2 describe one 16 bit addition and subtraction. Figure 8.3 and Figure 8.4 show one 32 bit addition and subtraction. Figure 8.5 and Figure 8.6 describe two 16 bit additions and subtractions. Figure 8.7 shows the operation that performs a subtraction between upper/lower 16 bit of X (32) and lower/upper 16 bit of Y (32). The additions and subtractions in Figure 8 can support various operations, such as Viterbi decoding, Turbo decoding, etc.

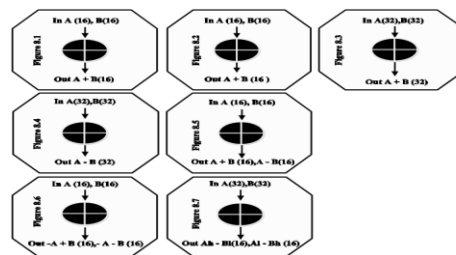


Figure. 8 Additions and Subtractions Using the Proposed Structure

IV. Comparisons

The proposed coprocessor has been evaluated for various communication algorithms using the simulator. Table 1 and figure 9 shows the performance comparisons between the proposed coprocessor and the conventional DSP (SC140) that is VLIW architecture. The proposed coprocessor shows better performance than the conventional DSP (SC140) [12].

Table 1. Performance Comparisons for Various Operations

Operation	SC140(Operation/Cycle)	Proposed (Opration/Cycle)
Multiply	4	4
Addition and Subtraction	2.5	4
MAC	4	4.5
Complex Multiply	1	1.5
Complex MAC	1	1.5
FFT Butterfly	1	2

*numbers represent # of operation per cycle

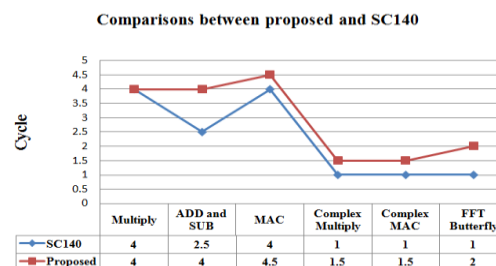


Figure.9. Comparison between proposed and SC140

In Table 1 represent the number of operations per cycle and comparison of both general multiply, add and subtract operation and proposed multiply, add and subtract operation by the help of this comparisons we can easily analysis what are the changes between basic and proposed multiply, addition and subtraction operation by this evolution the performs will be increase, accuracy and fast data transmission take place between transceiver and receiver. For example, SC140 performs 2 trellis butterfly calculations per cycle while the proposed coprocessor performs three butterfly calculations per cycle. The proposed architecture can reduce the clock cycles about 67% for convolutional encoding, and about 78% for block interleaving. Comparing with TI 62 x, the proposed multiplier/adder architecture can reduce the clock cycles about 48% for scrambling, 54 % interleaving and by about 84% for convolutional encoding for the IEEE 802.11a standard (12 Mbps data rate).

V. Conclusions

In this work, we show the design and the implementation of a reconfiguration coprocessor for next generation multiplier/adder and subtractions the reconfigurable coprocessor that can support various

communication standards and algorithms. An efficient operation of distribution communication system networks can be achieved by using reconfiguration techniques. The communication system network reconfiguration is carried out by changing the code rate and an instructions status of the sectionalizing switches. The proposed coprocessor can be used for communication operations, such as scrambling, interleaving, convolutional encoding, viterbi decoding, FFT, and several other functions using the proposed design. The coprocessor has been modelled by VHDL. Performance comparisons shows that the number of clock cycles can be reduced about 48% for scrambling and 84% for convolutional encoding compared with existing DSPs. From the results, performance of proposed coprocessor is better than conventional DSP (SC140) in terms of number of clock per cycle.

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