

## Efficient Explicit Pulsed Double Edge Triggered Flip-Flop by Using Dependency on Data

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**Abstract :** Dual edge triggering is an emerging effective method for reducing the power consumption in the clock distribution network. This paper compares three existing design of dual edge triggered flip-flop EP\_CDFF, EP\_CPF and DET-SAFF with the proposed design of the dual edge triggered flip-flop (DET-FF). The design eliminates the redundant transitions of internal nodes when current data is same as the previous one using conditional technique and also to disable the clock when the input invokes no output changes provide a control circuit. The design significantly reduces the power dissipation. Various TSPICE simulation with different input sequences show that reduction in power is 15.25% of those of the prior art. The design has been simulated using Tanner 13.0 EDA tool with 0.35  $\mu\text{m}$  technology at 25°C temperature

**Keywords** - Clock Distribution Network, Transmission Gate, Pulse Generator, Conditional Precharge, Conditional Discharge, Sense Amplifier

### I. INTRODUCTION

Continuous scaling of complementary metal-oxide semiconductor (CMOS) technology increases device density and enhances circuit performance in terms of computing power. CMOS has been the dominant technology for very large scale integration (VLSI) implementations. VLSI circuits are growing day by day and working in deep submicron, integration level is increased and higher clock speed is obtained. [1] Higher speed of clock, increase level of integration and technology scaling are reasons for high increases in power consumption. Therefore low power consumption is becoming very crucial factor for VLSI circuits. [2] Microprocessor power consumption is increasing approximately 20% per year. Since the flip-flops are the essential elements for designing the [3] semiconductor devices, they have a crucial influence on determining the parameters like speed, power consumption, clock skew tolerance and layout area. Timing elements i.e. latches and flip-flops are critical for the performance [4] of the digital systems because of the tight time constraints and requirements of low power. In many digital VLSI designs, the clock system consists of clock distribution network and flip-flops. By its action as timing signal the system controls the working rhythm of the chip. The digital system basically consists of set of flip-flops and interconnected combinational logic, the synchronous clock signal controls all flip-flops for sampling and storing their data synchronously. Approximately 30 to 60% of total system power consumption is dissipated in the clock distribution network, which has highest capacitance and operates at high frequencies. And out of which 90% of the power is consumed by the last branches of the clock distribution network. [5, 6] With the recent trend in frequency scaling and deep pipelining, this clocking system power may be even more pronounced. Moreover, because of the tight timing budget at high frequency operation, the latency of the flip-flop should be minimized. Timing parameters such data to output latency and setup and hold times are becoming equally important because the timing budget is getting tighter as the clock frequency approaches multi-gigahertz operating range [7]. In fig.1 schematic of conventional single edge triggered flip-flop is shown in which master stage has a transmission gate (TG1) to receive the data signal D. As is well known, TG1 is controlled to transmit the received data signal D by the true and complementary clock signal CLK and CLKB respectively. Thus transmission gate 1 is controlled to pass the data signal D prior to positive edge of the clock. The slave stage also include the transmission gate TG2 and a latch. However, TG2 is configured to be conductive when TG1 is non-conductive and vice-versa. Therefore the conventional rising SET flip-flop is capable of performing one bit access during a clock cycle. The schematic diagram of the single edge triggered flip-flop is shown below:-

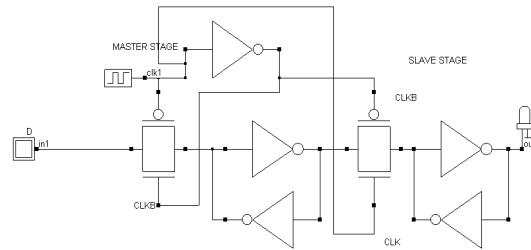


Fig.1 Single edge triggered flip-flop

However the operation performed at the one edge of the clock pulse either on the rising edge of the clock pulse or falling edge of the clock pulse. Data is sampled at the one clock edge. Dual edge triggering is a technique used to minimize power without the need to reduce supply voltage. In this type of flip-flop dual edge triggering is used. Using dual edge triggered flip-flops in clock distribution networks reduces the frequency of operation by half which can save about 50% of the network power consumption. In this type of triggering data is taken by the flip-flop both on negative and falling edge of the flip-flop i.e. sample the data at both rising and falling edge of the clock. Dual edge triggered flip-flop is sensitive to edge of clock that captures the value of the input after both rising or falling edge clock transitions as shown in fig 2. DET flip-flop changes its output at every clock transition that's why known as double edge triggered flip-flop or dual edge triggered flip-flop. The symbol which is used for the clock of the dual edge triggering is shown below:

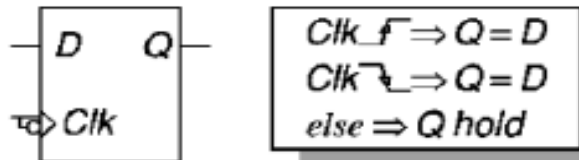


Fig.2 Symbol and Function of Dual Edge Triggered Flip-Flop

There are different types of the dual edge triggered flip-flop used in the different synchronous circuits. There are many microprocessors which use master-slave and pulse triggered flip-flops. Master slave dual edge triggered flip flop which is made up of two stages, one is master and other is slave. They are characterized by the positive set up time and large D to Q delay. Also there is duplicating of the latch part one is for master and other is for slave. Examples of master-slave flip-flops include the transmission gated transmission gated based flip-flop, push-pull dual edge flip-flop and transmission gate latch mux (TGLM). In pulse triggered flip-flops, one is implicit pulse triggered flip-flop in which for generating the clock pulse implicit pulse generator is used and other one is explicit pulse triggered flip-flop in which generation of the clock pulse by explicit pulse generator [10]. In implicit pulse generation of the clock pulse is inside the flip-flop therefore cannot be used by the neighbouring flip-flops in the entire circuit. In explicit pulse triggered flip-flop, the pulse is generated externally by the pulse generator. In this type of the flip-flop can have the pulse generator being shared by the neighbouring flip-flop, a technique which is not utilized in the implicit pulse triggered flip-flop. The number of transistors is less in this case as compared to the internal pulse generator type flip-flop.

## II. REVIEW OF DOUBLE EDGE TRIGGERED FLIP-FLOP

Several Dual edge triggered flip-flop have been described by replicating the latch elements of a SET (Single Edge Triggered Flip-Flop) and multiplexing the output. This paper compares the three existing dual edge triggered flip-flop and the proposed circuit for their power consumption.

In first type of dual edge triggered flip flop [7] which is shown in fig.3, firstly the pulse generator is used which produce the dual pulse which is active at both rising and falling edge of the clock. In this type, conditional discharge technique is used for reducing the redundant transitions. Redundant transitions means unnecessary charging and discharging of the internal major nodes when the input is same for the long time, which is reason for the power consumption. At that time when the input is stable that means no significant change in the output. But still at that time circuit evaluate the input. This is basically used to control the discharge path. The dual triggered pulse generator produces a brief pulse signal synchronized at both rising and falling clock edges. After that latch part is used to hold the output. This is a single ended flip-flop therefore always delay is present between Q and QB. The schematic of this flip-flop is shown in the figure 3:

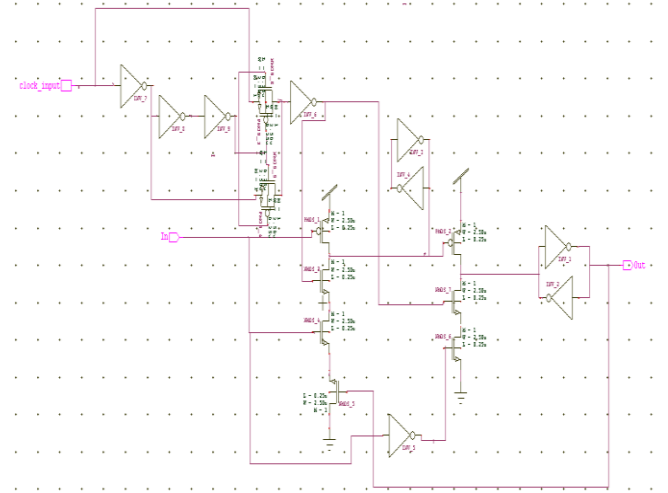


Fig.3 Schematic Representation of EP\_CDFD

In second type of flip-flop [11], conditional precharge technique is used for removing the redundant transitions of the flip-flop to reduce the power dissipation. The schematic of this type of circuit is shown in fig 4. In this conditional technique for preventing the precharging of internal node discharging path is controlled when the input remains is high for long time. The flip-flop's output is examined and the transition is allowed only if there is a significant change in the output of the flip-flop. The correct choice of flip-flop and its corresponding design has a deep effect in reducing the power consumption. Pulse triggered flip-flops gave better output as compared master slave latch flip-flops because of timing issues. In the CMOS synchronous circuit clock is considered as major factors for the power dissipation since which is signal that switches all the time.

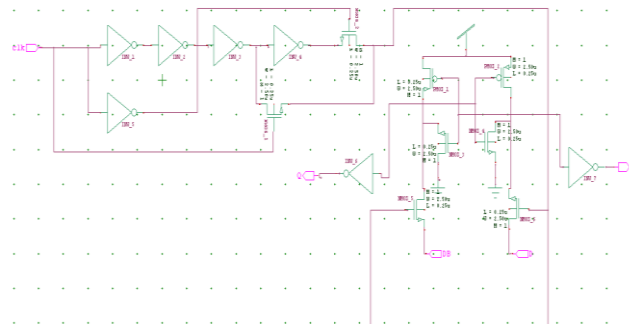


Figure 4. Schematic representation of EP\_CPFF

In third design, which [12] is shown in fig.5 sense amplifier approach is used for flip-flop design. In this basically pulse generator is used for generation of the clock pulse of short duration which is active at both rising and falling edge of the clock. After that in the sensing stage is used to sense the output and the after that nickolic latch is used to hold data. This flip-flop circuit results in reduction of power but still there is power dissipation. Power saving technique is only applicable to the latch part of the flip-flops. When the input is not changes at that time still the pulse generator is on and consumed a lot of power.

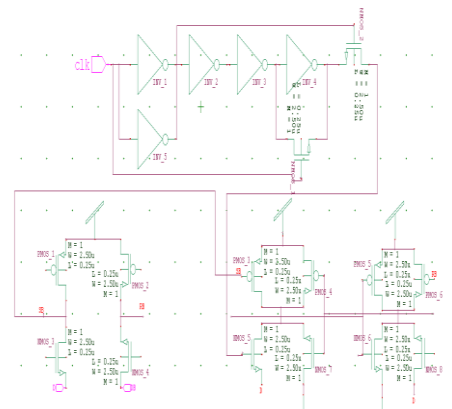


Fig.5 Schematic representation of DET-SAFF

### III. PROPOSED DUAL EDGE TRIGGERED FLIP-FLOP

In the above circuits of the flip-flop, the power reduction technique is only applied to at latch part only when the input is same for the long time which is not sufficient. In this proposed circuit of flip-flop some type of controlling circuit is embedded so that clock is disabling when the input invokes no output change. In order to eliminate the redundant transitions this data dependent technique based flip-flop is proposed. This results in saving of the power because the clock is disable at the point when no significant change at output because of stable input. The schematic of this circuit is shown below which is made by using Tanner EDA tool 13.1: firstly the control circuit is shown in which xoring is done between D and Q, and DB and QB as shown. That is this is depends upon the data because in this basically compares the data D with the output Q. Then the control signal GCLK is provided to the pulse generator and then sensing stage in which sense amplifier is used and after that latch part is used. The schematic of this proposed flip-flop is shown in Figure 6.

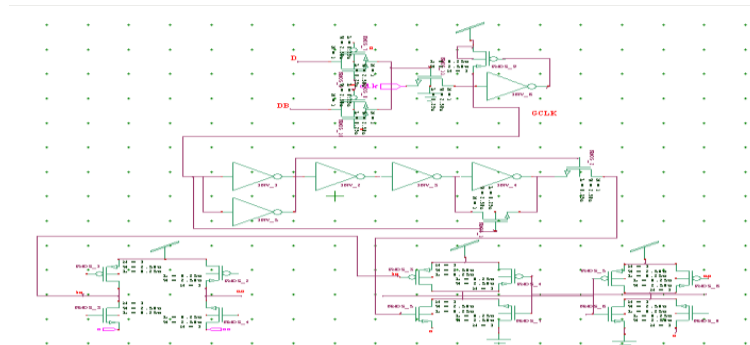


Fig.6 Schematic representation Proposed work

### IV. SIMULATION AND RESULTS

In this section the layout and corresponding analog simulation of above flip-flop design is shown. Firstly the layout and simulation of flip-flop circuit of fig.3 is shown. Layout of the ep\_CDFF is shown below in fig 7. Layout is the general concept that describes the geometric representation of the circuits by the means of the layers and polygons. Different logical layers are used by the designers to generate the layout. There are specific layers for metal, polysilicon, contacts or diffusion areas. In this red color shows polysilicon, green color shown n+ diffusion, light green color shows p+ diffusion, light blue color shows metal1 and dark blue color shows metal 2.

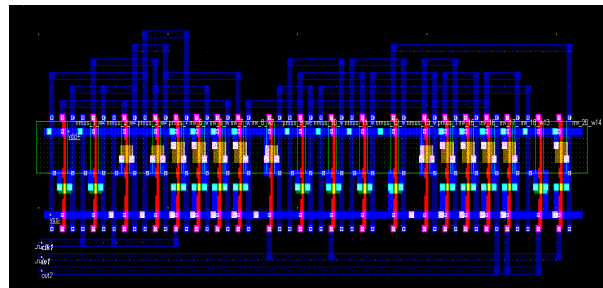


Fig.7 Layout Design of Ep\_CDFF

Fig. 8 shows the simulation waveform for the ep\_CDFF. The waveforms of puls, D input, Q output and QB is shown. The puls is very short duration appears at both rising and falling edge of the clock which is output of the pulse generator. When the clock input is applied to the pulse generator the corresponding output is puls which are produced at each edge of the flip-flop i.e. both at rising edge and falling edge of the flip-flop. After that when the data sequence is applied to the input of the flip-flop, the corresponding output Q and inverted output QB is shown in figure 6.

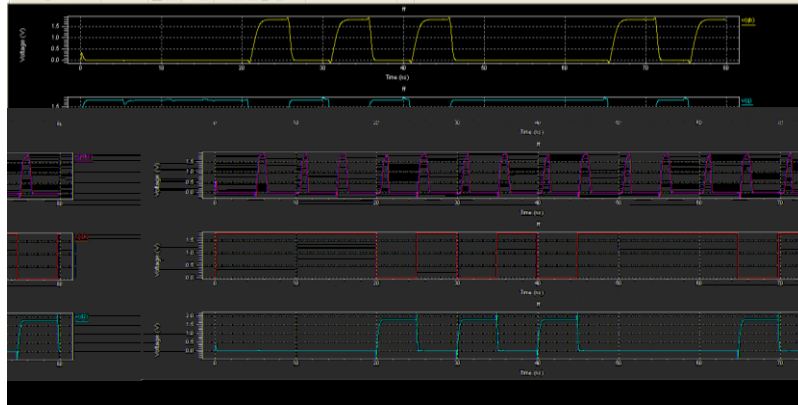


Fig.8 Simulation waveform of Ep\_CDFD

Fig.9 shows the layout of the fig4 (Ep\_CPFF) flip-flop. In this circuit conditional precharge technique is employed to reduce the redundant transitions at major internal nodes. To preventing these unnecessary charging and discharging of major internal nodes a simple PMOS transistor is embedded in the precharging path.

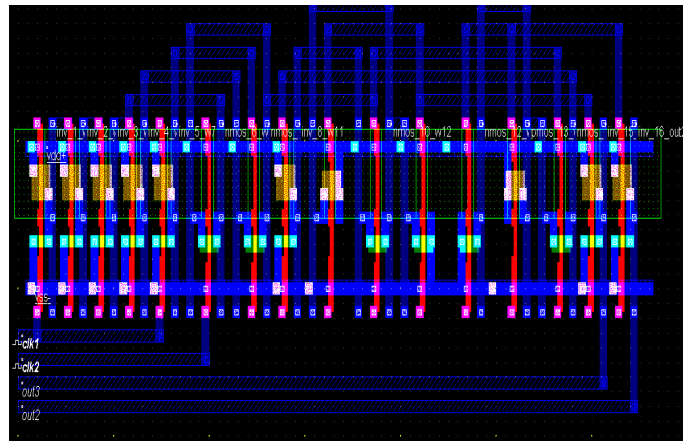


Fig.9 Layout design of Ep\_CPFF

The simulation waveform of the ep\_CPFF is shown in the fig.10. in this waveform the clock pulse applied to the pulse generator is shown and the corresponding out pulse of short duration produced at the output of the pulse generator is shown which is active at both rising and falling edge of the clock. The input D is applied and corresponding Q output is produced which is shown below and inverted output OB is also shown.

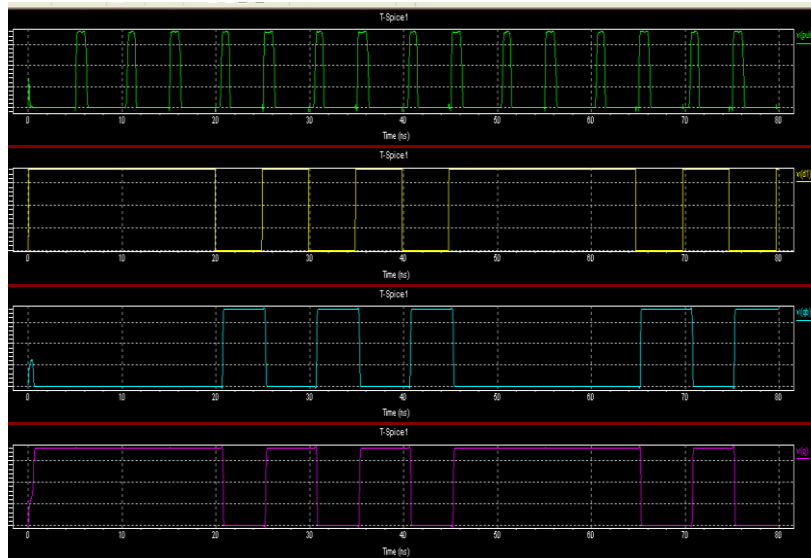


Fig.10 Simulation Waveform of ep\_CPFF

Fig. 11 shows the layout of DETSAFF of the fig. 5 design DET-SAFF. And in fig.12 corresponding simulation waveform is shown. In this waveform plot of input D, output Q and puls is shown. Also the plot of internal nodes RB and SB is also shown in the fig. The short duration pulsed is on for both the edges of the clock. When the input D is applied to the flip-flop corresponding output Q is obtained. From the waveform, it can be seen that clock is present all the time whether the input invokes no change at the output. Thus to provide the solution of this problem is data dependent technique which is shown in the proposed work.

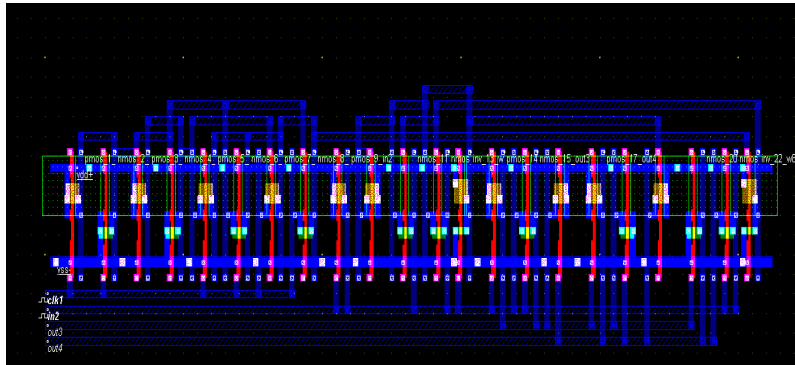


Fig.11 Layout design of DET-SAFF

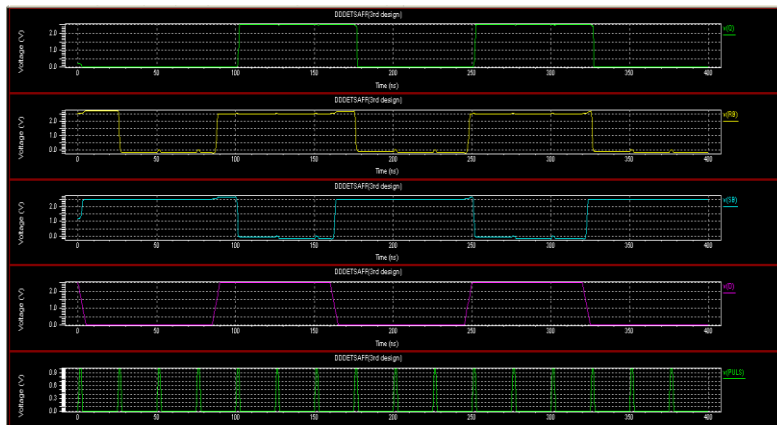


Fig.12 Simulation waveform of DET-SAFF

Fig. 13 shows the layout of the proposed work. And in fig.14 is the analog simulation waveform of the proposed flip-flop is shown. In this puls is the waveform produced when the clock controlling circuit is used which is basically a Gclk as discussed above. As shown in simulation when input D is not changes then at that time puls is not present. Thus disabling the clock generator and results in saving of the 15.25% power as compared to the 3<sup>rd</sup> design.

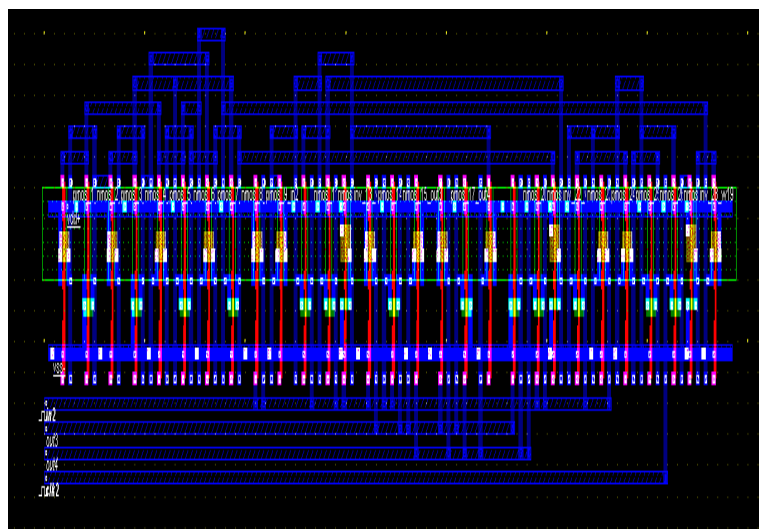


Fig.13 Layout Design of Proposed Work



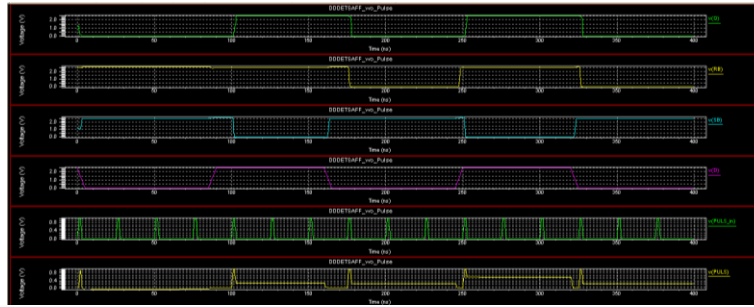


Fig.14 Simulation Waveform of Proposed Work

The comparison table of different parameters for this circuit is shown below in table1. The circuits are simulated with 0.35 $\mu$ m CMOS technology with 2.5 V supply voltage and temperature at 25°C. The operating clock frequency is 250MHZ. The proposed work is 15.25% efficient as compared to prior art i.e. from DET-SAFF.

TABLE1. PERFORMANCE COMPARISON OF FLIP-FLOPS

Parameter	Designs			
	<i>EP_CDFD</i>	<i>EP_CPF</i>	<i>DET-SAFF</i>	<i>Proposed DETFF</i>
Average Current	19.8 $\mu$ A	40.84 $\mu$ A	6.56 $\mu$ A	5.56 $\mu$ A
Power Consumption	49.72 $\mu$ W	102.10 $\mu$ W	16.4 $\mu$ W	13.9 $\mu$ W

## V. CONCLUSION

Dual edge triggered flip-flops reduce clock frequency by half leading to 50% reduction in the network power consumption while paying virtually no penalty in throughput. In this paper compare three previously published double edge triggered flip-flop design in which conditional techniques are used for reducing redundant transitions. ep\_CDFD implements conditional discharge technique to reduce unnecessary charging and discharging of internal nodes and ep\_CPF implements conditional precharge technique for reducing the redundant transitions and DET-SAFF used sense amplifier approach and conditional precharge technique. In the proposed work dual edge triggering is combined with the sense amplifier approach and data dependent technique for reducing power consumption. TSPICE simulation result shows, proposed flip-flop design is 15.25% efficient in terms of power consumption as compared to DET-SAFF.

## VI. Acknowledgements

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