

## Lateral I - Mos (Impact – Ionization) Transistor

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**Abstract:** One of the “fundamental” problems in the continued scaling of MOSFETs is the 60 mV/decade room temperature limit in sub-threshold slope. Therefore initial studies on a new kind of transistor, the I-MOS, is done. The I - MOS uses modulation of the breakdown voltage of a gated p - i - n structure in order to switch from the OFF to the ON state and vice versa. Since impact-ionization is an abrupt function of the electric field (or the carrier energy), simulations show that the device has a sub-threshold slope much lower than the above mentioned. This TCAD Sentaurus project simulates the electrical characteristics of an n-channel impact ionization metal–oxide–semiconductor (n-IMOS) transistor. The  $I_d$ – $V_g$  characteristics of a two dimensional (2D) n-IMOS structure are simulated. The  $I_d$ – $V_g$  characteristics are simulated for drain biases of 0 V and 1.1 V. In addition, various electrical parameters such as the breakdown voltage, the threshold voltage, the sub-threshold slope, and the on-current and off-current are extracted.

**Keywords** - I-MOS, p-i-n structure, sub-threshold, threshold voltage, on current, off current

### I. Introduction

The semiconductor industry has relied on the CMOS technology for the past four decades, as it is known for its power efficiency and operating speed [1]. The industry is continuously trying to make relatively smaller devices. But the concern is how small the smaller devices can be made as everything has a limit. CMOS scaling too is said to have reached its limit. Scaling CMOS sub-100nm poses several problems such as leakage currents, mobility, reliability, -affecting the device performance. Hence, the researchers in this field are looking for new materials and structures to address to the problems of scaling [2-6]. But still, the on-going research in this field is trying to focus on developing methods to go beyond the 45 nm technology .

Impact ionization MOSFET (I-MOS) [2] is one of the devices that is believed to have the potential to solve some of the problems of scaling. As we know that one of the “fundamental” problems in the continued scaling of MOSFETs is the 60 mV/decade room temperature limit in sub-threshold slope. Therefore initial studies on a new kind of transistor, the I-MOS, is done.

The I - MOS uses modulation of the breakdown voltage of a gated p - i - n structure in order to switch from the OFF to the ON state and vice versa. Since impact-ionization is an abrupt function of the electric field (or the carrier energy) , simulations show that the device has a sub-threshold slope much lower than the above mentioned.

The I – MOS is generally of two types that is Lateral I – MOS and Vertical I – MOS. Study in this project has been focused only to the lateral structure of the I - MOS . Lateral I - MOS with its gated PIN structure, works by modulating the channel length in transition from the OFF state to the ON state. At low gate voltages, there is no inversion layer formed and the effective channel length is the entire intrinsic region. As the gate voltage is increased, the effective channel length decreases, due to the formation of the inversion layer below the gate.

It uses the concept of impact ionization for carrier injection. This enables to produce sub-threshold slopes below 5mV/dec . Low sub-threshold slopes indicate good ION/IOFF ratio and low sub-threshold leakage currents . This is considered to be one of the major advantages of lateral IMOS.

Using the sentaurus device editor and sentaurus work bench of synopsys tool T – CAD the simulations are carried out to examine the device characteristics . In addition, various electrical parameters such as the breakdown voltage, the threshold voltage, the sub-threshold slope, and the on-current and off-current are extracted.

### II. LATERAL I – MOS

This project is used to perform the most common types of simulations used in n-IMOS device characterization and performance assessment. It contains device simulation set ups for breakdown and  $I_d$ – $V_g$  simulations. The project is based on an analytic n-IMOS structure, which is created using Sentaurus Structure Editor and uses the Inspect library extract most common electrical parameters such as the breakdown voltage, the threshold voltage, the subthreshold slope, and the on-current and off-current. The off-current of the n-IMOS device is dominated by band-to-band tunneling; whereas, the on-current is generated by avalanche breakdown due to impact ionization [7]. Therefore, both band-to-band tunneling and impact ionization models are crucial

for the simulation of n-IMOS device characteristics, and the device provides a comprehensive set of these models.

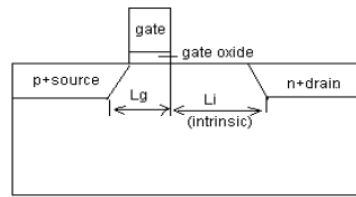


Fig 1: Schematic of Lateral IMOS

Lateral IMOS with its gated PIN structure, as shown in figure 1, works by modulating the channel length in transition from the OFF state to the ON state. At low gate voltages, there is no inversion layer formed and the effective channel length is the entire intrinsic region. As the gate voltage is increased, the effective channel length decreases, due to the formation of the inversion layer below the gate [2].

It uses the concept of impact ionization for carrier injection. This enables to produce sub-threshold slopes below as 5mV/dec. Low sub-threshold slopes indicate good ION/IOFF ratio and low sub-threshold leakage currents [12]. This is considered to be one of the major advantages of lateral IMOS. But, as I-MOS works on the concept of impact ionization, it requires high supply voltages for breakdown to occur, which results in hot carrier degradation effects [11]. Hot carriers are responsible for damaging the gate oxide and shifting the threshold voltage, which in turn affect the sub-threshold slopes [13]. Hence, to implement the I-MOS concept, more effectively, the research focus has been shifted towards the vertical IMOS

Figure 1 shows the n-IMOS device with a gate length of 60 nm and an intrinsic region length of 40nm, which is similar to the structure in the literature [8]. The basic IMOS structure is a gated p-i-n diode with a lightly doped intrinsic region [9]. The gate partially covers the intrinsic area. For an n-IMOS, the intrinsic region is p-doped. Impact ionization occurs in this region. Since this region is lightly doped, the electric fields required for impact ionization are reduced, which prevents a soft breakdown related to band to-band tunneling.

### III. SIMULATION RESULT OF LATERAL I-MOS

From here we can see the improvement in the sub-threshold slope as well as in other electrical parameters with respect to the results. Conceptually, the IMOS transistor can be regarded as a combination of a p-i-n diode and a MOS transistor [9]. To simulate the Id–Vg characteristics, the gated p-i-n diode is reverse biased close to its breakdown voltage. A positive bias is applied to the gate to build the conduction channel. As the gate bias increases, the lateral electric field increases ,leading to breakdown in the device. The device simulation of the IMOS involves the simulation of the breakdown as well as the Id–Vg of the MOS transistor.

For both the breakdown and Id–Vg simulations of the n-IMOS, the p-i-n diode is reverse biased [10] by keeping the drain at 0 V or 1.1 V, and the source at a negative bias. The box electrode is kept at 0 V for all experiments. For the breakdown simulations, the values of the drain and gate bias are defined by the Sentaurus Workbench parameters Vd and Vg, respectively. For the Id–Vg simulations, the values of the drain and source bias are defined by the Sentaurus Workbench parameters Vd and Vs, respectively.

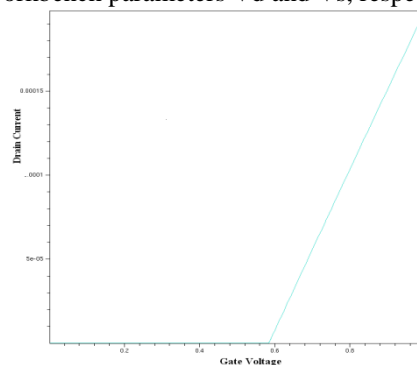


Fig 2. Id–Vg characteristics of n-IMOS

The Id–Vg Characteristics for the Id–Vg simulation, both the source and drain bias are ramped using the Quasistationary command. The voltage for the drain bias sweep is defined by the Sentaurus Workbench parameter Vd.

The sub-threshold slope,  $S_{min}$ , of the IMOS is defined as the minimum of the sub-threshold slopes at each bias point of the  $I_d$ - $V_g$  curve [7]. It is extracted using the Inspect command file. From the figure 3,  $S_{min} = 3.18$  mV/decade for  $V_d = 0$  V and  $S_{min} = 2.65$  mV/decade for  $V_d = 1$  V.

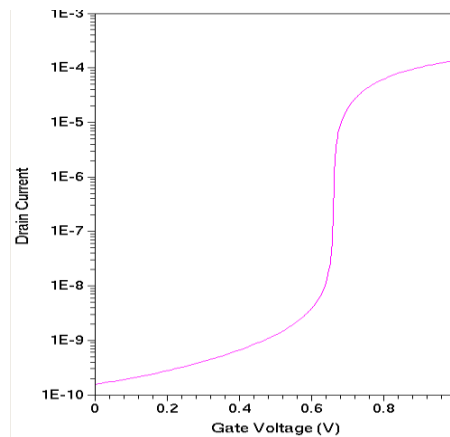


Fig 3.  $I_d$ - $V_g$  characteristics of n-IMOS

Extracting On-Current and Off-Current, the on-current and off-current of the n-IMOS are obtained from the  $I_d$ - $V_g$  characteristics. Here, the definitions of on current and off-current are similar to those used in the literature [10]. The on-current and off-current are defined as the value of the drain current at a gate voltage of  $V_{ts} + 0.3$  V and  $V_{ts} - 0.3$  V. From Figure 3, the on-current and off-current for  $V_d = 0$  V are  $1.23 \times 10^{-4}$  A/ $\mu\text{m}$  and  $5.35 \times 10^{-10}$  A/ $\mu\text{m}$ , respectively. For  $V_d = 0$  V,  $I_{on}/I_{off} = 2.299 \times 10^5$ .

#### IV. CONCLUSION

A brief study on the lateral IMOS device has been made. It is observed that it gives better on-off current ratio and also it gives better sub-threshold slope.

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