Relative Analysis of Speed and Noise Performance of SiGe HBT Between Experimental and Simulated Model

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Abstract: *Speed and Noise performance of SiGe HBTs in terms of the cut off frequency and the noise figure is investigated by ATLAS software. Noisy transistors disgrace the performance of mobile wireless receivers and put off amplifiers and oscillators from meeting the rigorous requirements forced on them while working at frequencies in the GHz range. Small noise improvements at the device level can have a large blow on overall system presentation. In this paper, a model is projected for speed and noise analysis of SiGe HBTs that is implemented in software ATLAS from SILVACO international and analyzed all the way through a thorough method. The results of experimental and simulated model has been compared and contrasted.*
Keywords: **SiGe HBT , ATLAS Software , parameter extraction**

I. INTRODUCTION

For high frequency ac operation, bipolar transistors are repeatedly assessed according to two figures of-merit. The first is known as the unity gain cut-off or transition frequency, f_T . The second is known as maximum frequency oscillation frequency. While both figures-of-merit may not unavoidably be appropriate for all application of SiGe HBTs, both are still widely quoted predominantly in device research publications. Brilliant speed performance is privileged for most practical semiconductor applications of today. The effectiveness of information dispensation strongly depends on the speed of devices that compose the system. The speed of a device can be represented by different measures and corresponding speed parameters. the most widely used speed parameters for transistors are the cutoff frequency f_T and the maximum oscillation frequency f_{max} , which are defined as the frequency point where the current gain and the power gain become unity, respectively[1].

Noise, as one of the crucial properties, exists in all kinds of semiconductor materials and acts a significant role in the performance of semiconductors, not only for an individual diode or transistor, but also for the whole circuit, and represents an unpredicted random interference. This observable fact limits the minimum signal level that any devices can profitably work on, since there will always be a small but important amount of noise arising. In an additional hand, noise also hold some useful information which can help scientists and engineers to distinguish the properties of the devices and further take the improvement of it, such as inquiring the fault density, the material purity and reliability, the circumstance of circuits, etc. Therefore, studying noise will redound to identify the characteristics of materials and perk up the performance of circuits[2][3].

Noise can be defined as "everything except desired signal". A noise source that can be condensed or eliminated using good defend system is called Artificial noise. For example, the noise sources that prying with broadcasting signal for radio and TV. On the other hand, a noise source that is intrinsic in the system or devices itself and is irreducible is called Fundamental noise. For example, the snow pictures in analog TV sets. Noisy transistors disgrace the performance of mobile wireless receivers and put off amplifiers and oscillators from meeting the rigorous requirements forced on them while working at frequencies in the GHz range. Small noise improvements at the device level can have a large blow on overall system presentation. A variety of analytical equations were used to determine the minimum noise figure NF_{min} of a bipolar transistor as a function of bias situation and transistor parameters. In recent times, a different approach for the NF_{min} calculation of bipolar transistors was used to give NF_{min} in terms of the small-signal parameters of the transistors. All of these approaches neglected an important cause that should be considered to get superior high-frequency (HF) noise modeling: the relationship between collector and base shot noise sources[4][5].

Currently, a very significant issue in electronic industry is modeling devices, since an exact model can help to understand internal mechanism that disgrace the device performance behavior in some manner, and then evade them as for as possible in order to optimize the device. Speed and noise is a result of these mechanism, and it can set a performance frontier of the device if it has an important role in the behavior so it can be condensed if the proposed model is accurate and shows the parameter that have a direct influence on it.

A new and very simple extraction method for determining the small signal Π topology equivalent circuits of silicon – germanium (SiGe) hetrojunction bipolar transistors (HBTs) has been developed [6][7][8]. Both intrinsic and extrinsic parameter can be extracted with the algorithm. Conservative procedures or methods based on simple bias measurements work very well if the extrinsic parameters of the HBT have been formerly determined. SiGe HBT is appropriate for RF, microwave and optical applications, since they attain high cut-off and oscillation frequency. SiGe HBTs are proficient devices at low cost because of their easy combination with Si technology, widely used in electronics in compare with iii-v technology which offer superior velocity but at higher costs.

In this work, we focus on device speed and noise performance in terms of cut-off frequency & minimum noise figure, and projected a model for speed and noise analysis of SiGe HBTs that is implemented in software ATLAS from SILVACO and analyzed all the way through a thorough method. The results of experimental and simulated model has been compared and contrasted. In the next two sections, a model is projected and methodical procedure is analyzed. Later on result is discussed based on experimental and simulation on SILVACO.

II. PROJECTED MODEL and DEVICE UNDER ANALYSIS

There are many ways to attain the prophecy of small signal as well as large-signal high-frequency properties of semiconductor devices. We can utilize Frequency domain perturbation investigation for the calculation of the small-signal characteristics. On the contrary, for a large-signal response, the Fourier analysis is required. In ATLAS to calculate small-signal characteristics at any frequency, the Frequency domain perturbation of a dc resolution can be used [9]. For investigation the small signals Π equivalent circuit of an HBT device is shown in figure 1 [10]. Variables are symbolized as the summation of a known dc factor as well as an unknown sinusoidal ac factor. In our work a small signal Π- model shown in the figure 1 is projected where the elements surrounded by the dotted square are the insintric part, whereas the parameters exterior the dotted square represents the parasitic elements due to contacts and pads.

Values of the intrinsic model of the device –

Table : 1

Parameter	Value
Rπ	20.923 KΩ
Gm	33.55 ms
Cμ	0.52074 fF
Cπ	19.0921 fF

Values of the extrinsic model for the device –

Table : 2

Parameter	Value
C_{JC}	57.86 aF
C_{BE}	306 Ff
C_{CE}	639 Ff
Rcc	5.7 Ω
R_L	1.5 Ω
R_{LC}	2 Ω
R_E	3.104 Ω

In order to express the validity of the model, first we compare results obtained by electrical simulation with results obtained all through analytical equations. The device has a constant Ge content of 25% in base , emitter area of $0.17 \times 5.7 \ \mu m^2$ and a doping level 4.3×10^{13} at / cm^2 .Intrinsic parameters and extrinsic parameters of the transistor are reported in Table 1 and Table 2 [11].
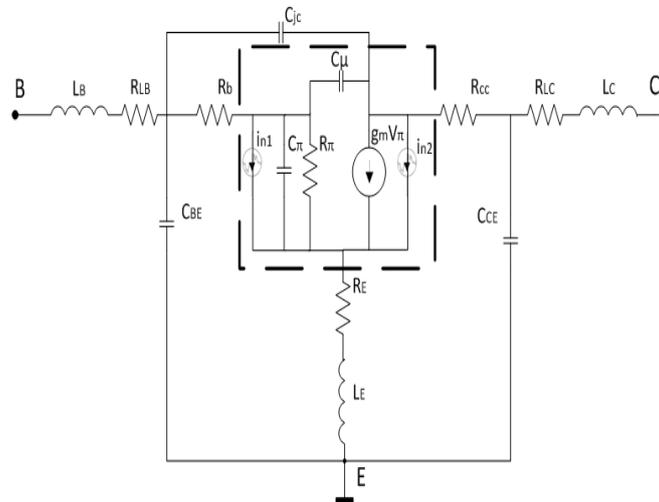

Fig. 1. small – signal Π model of a SiGe HBT

III. METHODICAL PROCEDURE

For high frequency ac operation, bipolar transistors are repeatedly assessed according to two figures of- merit. The first is known as the unity gain cut-off or transition frequency, f_T . The second is known as maximum frequency oscillation frequency. While both figures-of-merit may not unavoidably be appropriate for all application of SiGe HBTs, both are still widely quoted predominantly in device research publications.

The noise of a transistor can be characterized by an input current noise source i_n , and an input voltage noise source v_n. Noise figure (NF) is in broad a function of the source admittance Y_s. At a finest value $Y_{s,opt}$, noise figure reaches a minimum value of NF_{min}. The noise figure for arbitrary source admittance can be expressed   as:

$$NF = NF_{min} + \frac{R_n}{G_s} \left| Y_s - Y_{s,opt} \right|^2$$

(1)

where G, is the real part of Y_s, and R_n, is the noise resistance which determines the warmth of the total noise figure to deviations from $Y_{s,opt}$ [12] .
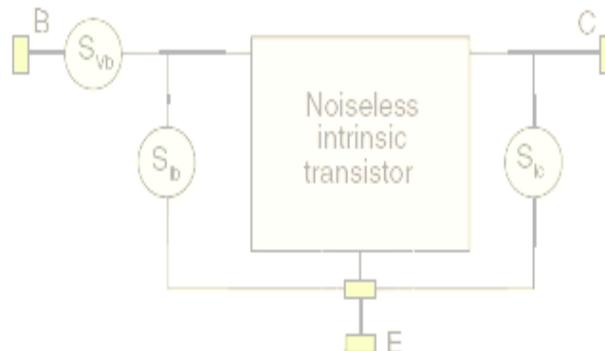

Figure : 2 Schematics of the noise sources in a transistor and its chain noisy tow port representation.

The methodical expression for f_T, f_{MAX} and NF_{min} are advantageous for gaining additional perceptive insight into device optimization for speed and noise. This can be skilled using methodical Y-Parameter equations. For this purpose a linear noisy two – port network is verified in figure – 2 [13][14][15].

In order to make such methodical expression realistic, the accuracy must be balanced against plainness of the functional form. the power spectral densities of the input noise current (Sin), the input noise voltage (Svn) and their cross-correlation (Sin. vn*.) are given by[16].

$$S_{vn} = \frac{V_{na} V_{na*}}{\Delta f} = \frac{S_{i_c}}{|Y_{21}|^2} = \frac{2q\, Ic}{|Y_{21}|^2} \qquad (2)$$

$$S_{in} = \frac{I_{na} I_{na^*}}{\Delta f} = S_{ib} + \frac{S_{i_c}}{|H_{21}|^2} = 2qI_b + \frac{2q\, I_c}{|H_{21}|^2} \qquad (3)$$

$$S_{in\, vn^*} = \frac{2\, q\, I_c\, Y_{11}}{|Y_{21}|^2} \qquad (4)$$

where Y_{11} is the input admittance, Y_{21} is the transfer admittance, and $h_{21} = Y_{21}/Y_{11}$ is the ac current gain. Noise figure can be condensed by decreasing $< v_n^2 >$ and $< i_n^2 >$. Physically, $< i_n^2 >$ is contributed by the base shot noise $2qI_B$ and the collector shot noise $2qI_c$, and $< v_n^2 >$ is contributed by the base thermal noise $4KTr_B$ and the collector shot noise $2qI_c$. $2qI_c$ contributes to mutually v_n and i_n, and determines $<v_n i_n^*>$.

In further step, we state the Y-Parameters in provisions of essential device parameters, for example β, gm etc. The small signal comparable circuit in simplified is shown in figure – 3 & figure- 4. The base resistance is not imperative for the input impedance at frequencies smaller than f_T. Thus it can be disregarded for simplicity, even though it is remarkable as a noise voltage generator. Intrinsic part of the model projected is shown in figure :3, where it can be identified two stages in the circuits connected in parallel [16].
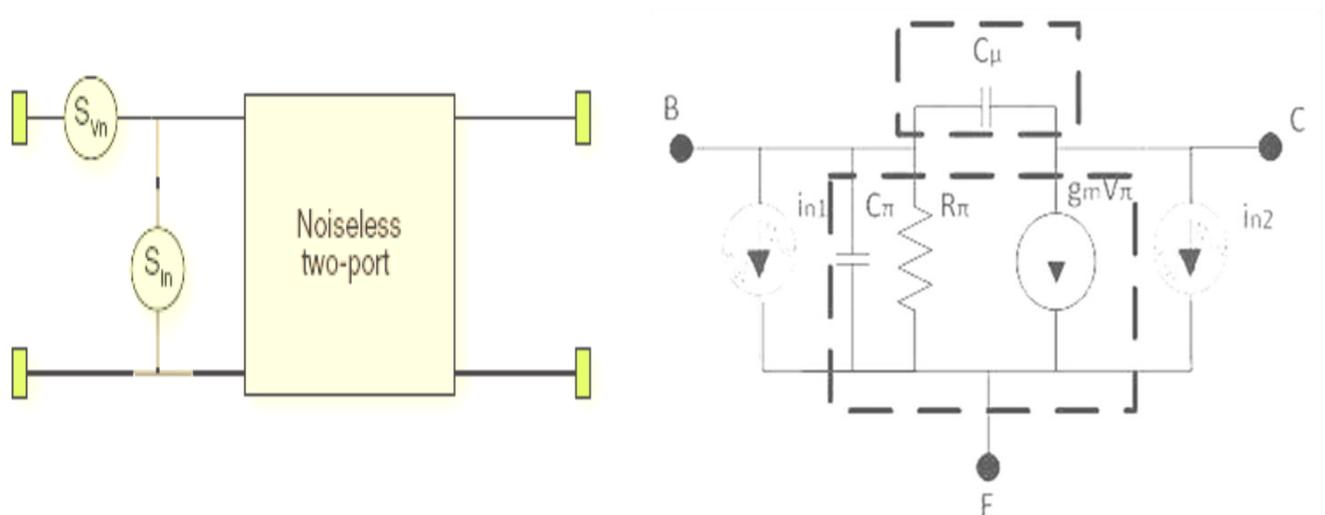

fig. 3- Intrinsic Part

$$Y_{11} = \frac{g_m}{\beta} + j\omega C_i \tag{5}$$

$$Y_{12} = -j\omega C_{BC} \tag{6}$$

$$Y_{21} = g_m \tag{7}$$

$$Y_{22} = j\omega C_{BC} \tag{8}$$

$$g_m = \frac{qkT}{I_c} = \frac{1}{r_e} \tag{9}$$

$$c_i = C_{be} + C_{bc} \tag{10}$$

The Cbe consists of the EB diffusion capacitance Si 1-x Ge x, and Extrinsic part involves besides intrinsic, parameters equivalent to parasitic elements related to device contacts and pads, so there are more stages than in intrinsic part. figure:4 shows the small – signal π – model spitted in ten stages essential for its study. Where the block includes the intrinsic part of the transistor with its related noise current and voltage sources: each resistor has related noise current source due to thermal noise and they are taken into account in the study.
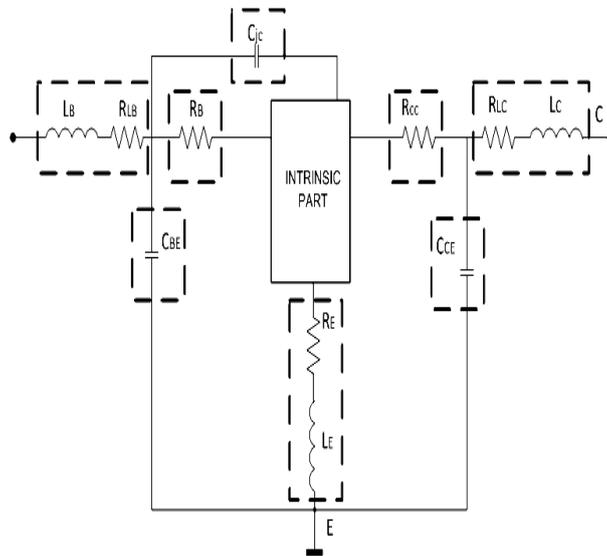

fig.4 Extrinsic Part

$$c_{be} = C_{te} + g_m\tau \tag{11}$$

where $\tau = transit\ time$

The Ci is related to fT and Cbc is the total CB junction capacitance, through ,

$$f_T = \frac{g_m}{2\pi C_i} \tag{12}$$

The oscillation frequency is expressed as

$$f_{max} = \sqrt{\frac{f_T}{8\pi C_{cb} R_b}}$$

(13)

Minimum noise figure is obtained as

$$NF_{min} = 1 + \frac{1}{\beta} + \sqrt{\left[\frac{2g_m R_n}{\beta} + \frac{2R_n(\omega C_i)^2}{g_m}\left(1 - \frac{1}{2g_m R_n}\right)\right]}$$

(14)

$$NF_{min} = 1 + \frac{1}{\beta} + \sqrt{2g_m R_b}\sqrt{\left[\frac{1}{\beta} + \left(\frac{f}{f_T}\right)^2\right]}$$

(15)

IV. RESULTS & DISCUSSION

In order to have a better reference to compare experimental model and simulated model, we add a comparison with speed and noise measurement in the device. It is needed to emphasize that in these cases that both extrinsic and intrinsic parts are taken into account. Now we compare speed in terms of cut-off frequency and noise figure in terms of NF_{min} variation with Ic at different frequencies using the ATLAS software from SILVACO international and measurements. Figure 5 and 6 shows how to evaluate cut-off frequency. the frequency at which AC current gain reaches unity or its value is 0 in dB, is known as cut-off frequency. figure 5 shows the evaluation of cut-off frequency for simulated model at ATLAS software from SILVACO international in the presence of 20% Ge concentration. The cut-off frequency for simulated model on ATLAS is 280.5 GHz. figure 6 shows the cut-off frequency evaluation of experimental model. The cut-off frequency for experimental model is 277.8 GHz.

figure 7 shows the variation of cut-off frequency of the device with Ge concentration. Two plots are there in the figure. the first plot shows the analysis of simulated model at ATLAS software from SILVACO international which has cut-off frequency of 267 GHz and 285 GHz at the presence of 2% Ge concentration and 25% Ge concentration respectively. the second plot shows the analysis of experimental model which has cut-off frequency of 264 GHz and 281 GHz at the presence of 2% Ge concentration 25% Ge concentration respectively. So, the percentage deviation of cut-off frequency of the two model is 1.12% at the presence of 2% Ge concentration and percentage deviation cut-off frequency of the two model is 1.75% . the ideal percentage deviation of the speed parameter of the two model should ne less than 3%. And this analysis shows the percentage deviation of speed parameter in terms of cut-off frequency less than 2%.
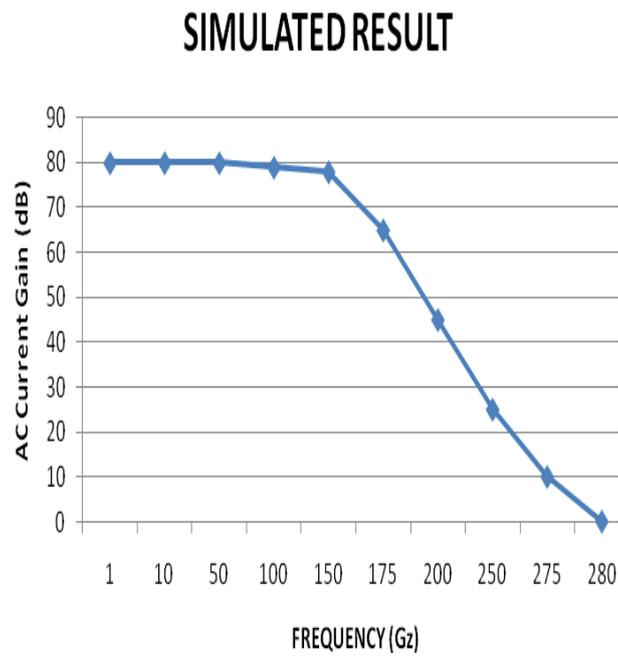
SIMULATED RESULT

Figure 5 : Evaluation of Cutt-off Frequecy for Simulated model
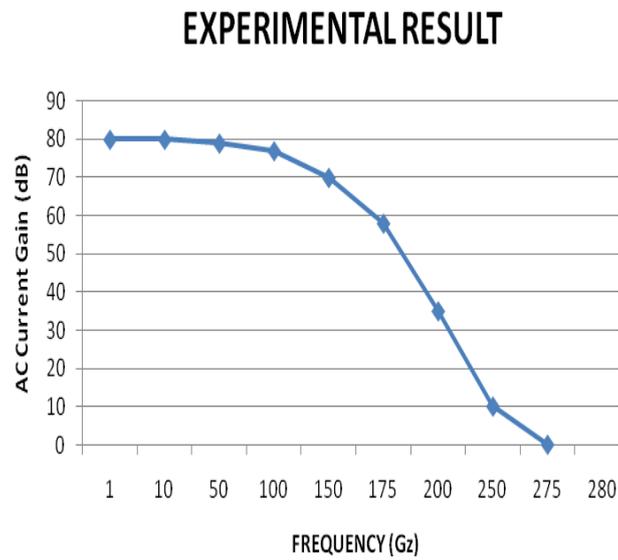
EXPERIMENTAL RESULT

Figure 6: Evaluation of Cutt-off Frequecy for Experimental model
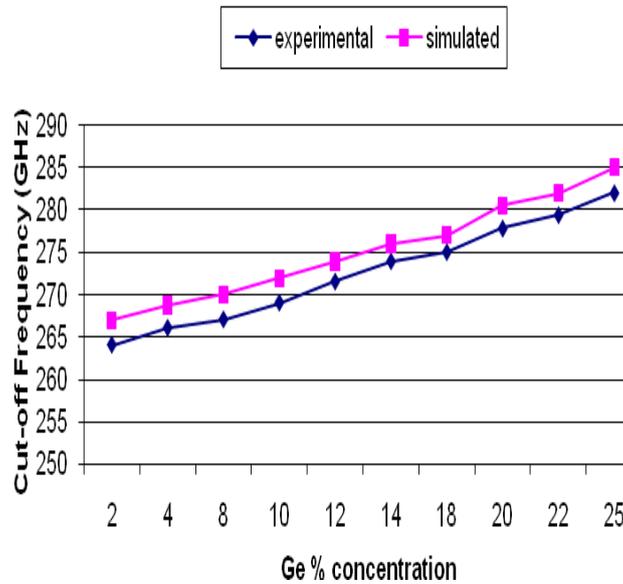
Cut-off Frequency Vs Ge % Concentration

Figure 7 : Variation of Cut-off frequency with Ge Concentration

figure 8 shows the variation of Noise Figure of the device with Collector Current (Ic). collector current axis is in milli ampere and Noise Figure is in dB. In this analysis, the noise figure of the experimental model at 1.5 mA is 0.048 dB and noise figure of simulated model from SILVACO international at 1.5 mA is 0.051 dB. The percentage deviation of the noise figure at 1.5 mA is 5.88%. The noise figure of experimental and simulated model at 2.5 mA are 0.40 dB and 0.42 dB respectively. The percentage deviation of the noise figure at 2.5 mA is 4.76%. The ideal percentage deviation of noise figure should be less than 8% for noise analysis and this analysis shows the percentage deviation of noise figure less than 6%. Yhe simulation is done on the ATLAS software from SILVACO international.

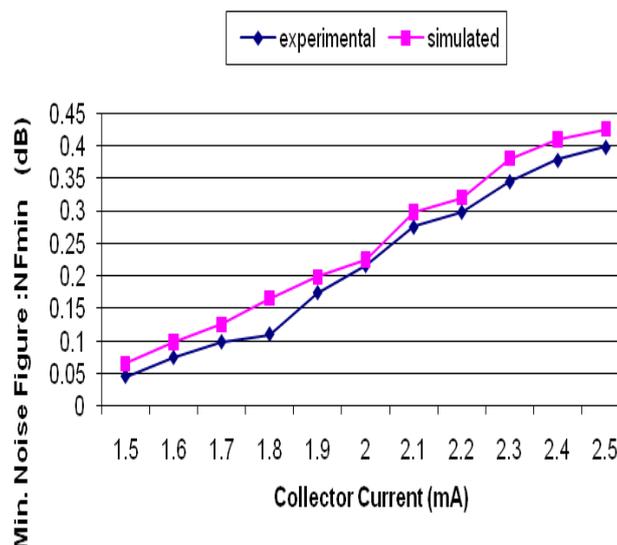**Min. Noise Figure Vs Collector Current**

Figure 8 : Variation of Noise Figure with Collector Current

        In order to have a complete picture of Noise behavior, a study of variation of noise parameters depending on frequency is also implemented. Figure 9 shows the variation of Noise Figure (dB) of the SiGe HBT with the cut-off frequency (GHz). This figure has two plots,one plot shows the analysis of simulated model at ATLAS software from SILVACO international and other plot shows the analysis of experimental model. The simulated model has noise figure of 0.051 dB and 0.42 dB at correspondingly cut-off frequency of 260 GHz and 280 GHz. The experimental model has noise figure of 0.048 dB and 0.40 dB at cut-off frequency of 260 GHz and 280 GHz respectively. The percentage deviation of noise figur of simulated and experimental model is 5.88% at 260 GHz and percentage deviation of both the model at 280 GHz is 4.76%. This analysis shows the percentage deviation of noise parameter less than 6% and ideal percentage deviation of noise parameter should be less than 8%. On increasing frequency the noise figure increases. analytical result has better speed, so it has more noisy in comparision to experimental result.
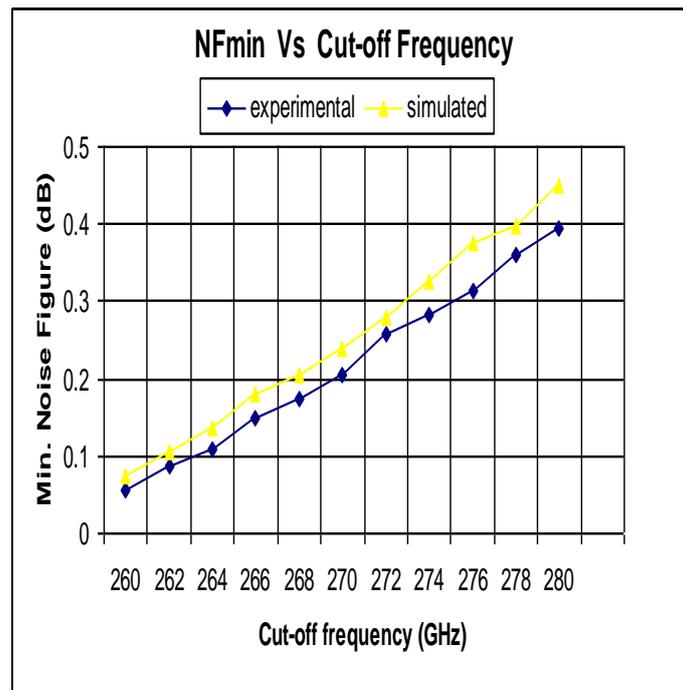

Figure 9 : Variation of Noise Figure with Cutt-off Frequency

V. CONCLUSION

        In this work, we focus on device speed and noise performance and projected a model for speed and noise analysis of SiGe HBTs that is implemented in software ATLAS and analyzed all the way through a thorough method. The results of experimental & simulated model are compared and contrasted. A comparative study of speed in terms of cut-off frequency and noise behavior in terms of minimum noise figure of SiGe Hetrojunction Bipolar Transistor has been presented in this work, involving real experimental measurement reported and projected model implanted on software ATLAS from SILVACO. In this analysis percentage deviation of speed parameter of SiGe HBT has been found less than 3% which should be theoretically less than 5%. The percentage deviation of noise parameter of SiGe has been found less than 6% which should be ideally less than 8%. Small signal Π model is selected to model and to analyze the device. Due to the fine approach that the expression obtained for every part of the transistor have with experimental measurement and simulation modeling, hence it is possible to say that these tools can be useful in the speed and noise optimization where SiGe Hetrojunction Bipolar Transistors are involved.

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