

Nano Technology - Spintronics

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ABSTRACT: *The Spintronics is the area of atomic level physics. It is the promising field in the area of data storage and memory requirement. Historically, its idea has a roots since quantum theory for atomic structure. The role played by electron and its spin is answer to wards the solution of memory requirement. Thekey features are utility of traditional semiconductorwith low power consumption, compact size, fastest and largest storage capacity.*

Keywords -*Atom, devices, memory, spin, storage capacity*

I. INTRODUCTION

In the area of portable memory, change in technology prevails. The exclusive change to pace with the rapid growth in technology leads to have huge space, small size and fast response. One of the probable answers is **Spintronics**. The technology wherein both the charge and spin of an electron is used to carry information has tremendous potential to fulfil the requirement of huge space, small size and fast response in the area of memory for its wide range of applications. Spintronics's biggest potential lies in embedded memories and non-volatile memory devices such as Magneto-resistive Random Access Memory (MRAM), which will revolutionize the memory market and aid the development of sophisticated and versatile computing and personal devices. "The behaviors of the magnetic element on a chip in both read and write modes is still a Research work to make MRAMs reliable". This leads towards a new class of device based on the quantum of electron spin, rather than on charge, may lead the next generation of micro-electronics[1].

Spintronics, or spin electronics, refers to the utility of the role played by electron (and more generally nuclear) spin in an atom of any material. Expected outcome is possible devices that exploits spin properties instead of or in addition to charge. For example, spin relaxation and spin transport in metals and semiconductors are of fundamental research interest. The device that is already in use in industry as a read head and a memory-storage cell is the Giant-Magneto Resistive (GMR) sandwich structure which consists of alternating ferromagnetic and nonmagnetic metal layers. Depending on the relative orientation of the magnetizations in the magnetic layers, the device resistance changes from small (parallel magnetizations) to large (anti parallel magnetizations). This change in resistance (also called magneto resistance) is used to sense changes in magnetic fields. Recent efforts in GMR technology have also involved magnetic tunnel junction devices where the tunneling current depends on spin orientations of the electrodes. Current efforts in designing and manufacturing spintronic devices involve two different approaches. The first is perfecting the existing GMR-based technology by either developing new materials with larger spin polarization of electrons or making improvements or variations in the existing devices that allow for better spin filtering. The second effort, which is more radical, focuses on finding novel ways of both generation and utilization of spin-polarized currents. These include investigation of spin transport in semiconductors and looking for ways in which semiconductors can function as spin polarizer's and spin valves. The importance of this effort lies in the fact that the existing metal-based devices do not amplify signals (although they are successful switches or valves), whereas semiconductor based spintronic devices could in principle provide amplification and serve, in general, as multifunctional devices. Perhaps even more importantly, it would be much easier for semiconductor-based devices to be integrated with traditional semiconductor technology. While there are clear advantages for introducing semiconductors in novel spintronic applications, many basic questions pertaining to combining semiconductors with other materials to produce a viable spintronic technology remain open. For example, whether placing a semiconductor in contact with another material would impede spin transport across the interface is far from well-understood. In the past, one of the strategies to advance understanding of spin transport in hybrid semiconductor structures was to directly borrow knowledge obtained from studies of more traditional magnetic materials. However, there is also

an alternative approach involving the direct investigation of spin transport in all-semiconductor device geometries. In such a scenario a combination of optical manipulation (for example, shining circularly polarized light to create net spin polarization) and material inhomogeneities (e.g. by suitable doping ferromagnetic materials) could be employed to tailor spin transport properties. In addition to various spin transistors and spin transport properties of semiconductors, subfield of spintronics is the application of electron and nuclear spins to quantum information processing and quantum computation. The quantum mechanics can provide great advantages over classical physics in physical computation. However, the real boom started after the advent of Shor's factorization algorithm and quantum error correction schemes. Among the many quantum computer hardware's that were proposed are the ones based on electron and nuclear spins. Obviously, the spins of electrons and spin-1/2 nuclei provide perfect candidates for quantum bits (qubits) as their Hilbert spaces are generally well-defined and their decoherence relatively slow [2].

II. THEORY

SPINTRONICS HISTORY:

The main purpose of development of Spintronics and its devices is to make memory more compact than today. For Spintronics, the density of storage of information is twelve months, which is much shorter than the law which describes that the number of transistors that can be incorporated in an integrated circuit doubles every 24 months i.e. two years. A 256 kb MRAM has read/write cycle of 50 nanoseconds. Other than MRAM's, another design in development, called the RACE TRACK MEMORY, encodes information in the direction of magnetization between the domain walls of a ferromagnetic metal wire.

Spin was first measured in the famous experiment of Stern and Gerlach in 1921. The research field of Spintronics emerged from experiments on spin-dependent electron transport phenomena in solid-state devices, including the observation of spin-polarized electron injection from a ferromagnetic metal to a normal metal, and the discovery of Giant magneto resistance. The origins can be traced back further to the Ferromagnet/superconductor tunneling experiments pioneered by Meservey and Tedrow, and initial experiments on magnetic tunnel junctions by Julliere in the 1970s. The use of semiconductors for Spintronics can be traced back at least as far as the theoretical proposal of a spin field-effect-transistor by Datta and Das in 1990

ARRANGEMENT OF SPINS

Spins can arrange themselves in a variety of ways that are important for spintronic devices. They can be completely random, with their spins pointing in every possible direction and located throughout a material in no particular order or these randomly located spins can all point in the same direction, called spin alignment. In solid state materials, the spins might be located in an orderly fashion on a crystal lattice forming a nonmagnetic material (unmagnetized).

The spins may be on a lattice and be aligned as in a magnetic material (Magnetized). The emitter emits electrons with their spins oriented along the direction of the electrode's magnetization, while the collector (with the same electrode magnetization) acts as a spin filter and accepts electrons with the same spin only. In the absence of any changes to the spins during transport, every emitted electron enters the collector. An electron passes through the collector if its spin is parallel, and does not if it is antiparallel, to the magnetization. If spintronic devices could be made from semiconductors, however, then in principle they would provide amplification and serve, in general, as Multi-functional devices. Perhaps even more importantly, semiconductor-based devices could much more easily be integrated with traditional semiconductor technology. Although semiconductors offer clear advantages for use in novel spintronic applications, many basic questions pertaining to combining semiconductors with other materials to produce viable spintronic technology remain unanswered.

III. SPINTRONICS DEVICES

(i) Giant magneto resistance (GMR):---

Magnetism is an intrinsic physical property associated with the spins of electrons in a material. Magnetism is already exploited in recording devices Such as computer hard disks. Data are recorded and stored as tiny areas of magnetized iron or chromium oxide. To access the information, a read head detects the minute changes in

magnetic field as the disk spins underneath it. Spintronics burst on the scene in 1988 when French and German physicists discovered a much more powerful effect called 'giant magneto resistance' (GMR). It results from subtle electron-spin effects in ultra-thin 'multilayer' of magnetic materials, which cause huge changes in their electrical resistance when a magnetic field is applied. The basic GMR device consists of a three-layer sandwich of a magnetic metal such as cobalt with a nonmagnetic metal filling such as silver. A current passes through the layers consisting of spin-up and spin-down electrons. Those oriented in the same direction as the electron spins in a magnetic layer pass through quite easily while those oriented in the opposite direction are scattered. If the orientation of one of the magnetic layers can easily be changed by the presence of a magnetic field then the device will act as a filter, or 'spin valve', letting through more electrons when the spin orientations in the two layers are the same and fewer when orientations are oppositely aligned. The electrical resistance of the device can therefore be changed dramatically. GMR is 200 times stronger than ordinary magneto resistance. IBM soon realized that read heads incorporating GMR materials would be able to sense much smaller magnetic fields, allowing the storage capacity of a hard disk to increase from 1 to 20 gigabits.

(ii) Magnetic random access memory (MRAM):----

The magnetic version of a random access memory (RAM) used in the computer is -'MRAM'. The advantage of magnetic random access memory (MRAM) is that it is 'non-volatile' - information isn't lost when the system is switched off.

Some potential advantages of MRAM are;

It allows information to be stored as 0's and 1's as in conventional transistor memory devices

MRAM uses magnetic hysteresis to store magneto resistance data and to read data.

GMR-based Pseudo spin valve memory cells are integrated on an IC chip and function like semiconductor RAM with additional feature that data are retained with power off.

Non-volatile, Small in size, Lower cost

100 times faster writer times than EEPROM and Flash memory. No wear out with write cycling

Require lower energy for writing

High data access time of about 1/10,000 than that of hard disks

These devices would be much more robust in extreme conditions such as high temperature and high level radiations or interferences.

Comparison to the memory devices

Racetrack Memory is expected to offer performance of the order of 20 to 32 ns to read or write a random bit. This compares to about 100,000 to 300,000 ns for a hard drive or 6 to 40 ns for conventional DRAM. There are also ways to improve the access times with the use of a "reservoir," improving to about 9.5 ns. Aggregate throughput, with or without the reservoir, is on the order of 250 to 670 Mbit/s for IBM Racetrack Memory, compared to 102400 for dual channel DDR to DRAM, 1000 for high-performance hard drives, and much slower performance on the order of 30 to 100 Mbit/s for Flash devices. The only current technology that offers a clear performance benefit over IBM Racetrack Memory is SRAM, on the order of 2 ns, but is much more expensive and far lower density. Flash, in particular, is a highly asymmetrical device. Although read performance is fairly fast, especially compared to a hard drive, writing is much slower. Flash works by "trapping" electrons in the chip surface, and requires a burst of high voltage to remove this charge and reset the cell. In order to do this, charge is accumulated in a device known as a charge pump, which takes a relatively long time to charge up. In the case of "NOR" flash, which allows random bit-wise access like IBM Racetrack Memory, read times are on the order of 70 ns, while write times are much slower, about 2,500 ns. To address this concern, "NAND" flash allows reading and writing only in large blocks, but this means that the time to access any random bit is greatly increased, to about 1,000 ns. Additionally, the use of the burst of high voltage physically degrades the cell, so most flash devices allow on the order of 100,000 writes to any particular bit before their operation becomes unpredictable. Wear leveling and other techniques can spread this out, but only if the underlying data can be re-arranged.

The key determinant of the cost of any memory device is the physical size of the storage medium. The reason for this is due to the way memory devices are fabricated. In the case of solid-state devices like Flash or DRAM, a large "wafer" of silicon is processed into many individual devices, which are then cut apart and packaged. The cost of packaging is about \$1 per device, so as the density increases and the number of bits per devices increases with it, the cost per bit falls by an equal amount. In the case of hard drives, data is stored on a number of rotating platters, and the cost of the device is strongly related to the number of platters. Increasing the density allows the number of platters to be reduced for any given amount of storage. In most cases memory devices store one bit in any given location, so they are typically compared in terms of "cell size", a cell storing one bit. Cell size itself is given in units of F^2 , where F is the design rule, representing usually the metal line width. Flash and racetrack both store multiple bits per cell, but the comparison can still be made. For instance, modern hard drives appear to be rapidly reaching their current theoretical limits around $650 \text{ nm}^2/\text{bit}$, which is defined primarily by our capability to read and write to tiny patches of the magnetic surface. DRAM has a cell size of about $6 F^2$, SRAM is much worse at $120 F^2$. NAND flash is currently the densest form of non-volatile memory in widespread use, with a cell size of about $4.5 F^2$, but storing two bits per cell for an effective size of $2.25 F^2$. NOR is slightly less dense, at an effective $4.75 F^2$, accounting for 2-bit operation on a $9.5 F^2$ cell size. Racetrack Memory appears to scale to much smaller sizes than any current memory device. In the vertical orientation (U-shaped) about 128 bits are stored per cell, which itself can have a physical size of at least about $20 F^2$. No other technology appears to be able to scale anywhere near these densities, representing a storage density about 100 times that of Flash. The caveat here is that bits at different positions on the "track" would take different times (from $\sim 10 \text{ ns}$ to nearly a microsecond, or 10 ns/bit) to be accessed by the read/write sensor, because the "track" is moved at fixed rate ($\sim 100 \text{ m/s}$) past the read/write sensor.

Racetrack Memory is one of a number of new technologies aiming to replace Flash, and potentially offer a "universal" memory device applicable to a wide variety of roles. Other leading contenders include MRAM, PCRAM and FeRAM. Most of these technologies offer densities similar to Flash, in most cases worse, and their primary advantage is the lack of write endurance limits like those in Flash. Field-MRAM offers excellent performance as high as 3 ns access time, but requires a large 25 to $40 F^2$ cell size. The highest densities from any of these devices is offered by PCRAM, which has a cell size of about $5.8 F^2$, similar to Flash, as well as fairly good performance around 50 ns . Nevertheless, none of these can come close to competing with Racetrack Memory in overall terms, especially density. For example, 50 ns allows about 5 bits to be operated in a Racetrack Memory device, resulting in an effective cell size of $20/5=4 F^2$, easily exceeding the performance - density product of PCRAM. On the other hand, without sacrificing bit density, the same $20 F^2$ area can also fit 2.5 2-bit $8 F^2$ alternative memory cells (such as RRAM or spin-torque transfer MRAM), each of which could individually operated much faster ($\sim 10 \text{ ns}$).

IV. ADVANTAGES & DISADVANTAGES

The advantages of Spintronics:

- Low power consumption
- No electric current required
- Faster Devices
- Larger storage capacity
- Compact devices

Spintronics does not require unique and specialized semiconductors; can be implemented or with common metals, such as Copper, Aluminium and Silver.

Since Spins don't change when power is turned off, the memory remains non-volatile.

The Disadvantages of Spintronics:

- Controlling the spin for long distances.
- Combining techniques between the semiconductor and magnetic Recording industry.
- Silicon causes electrons to lose their spin state.

Major challenges are:

Transport of spin polarized carriers across relevant length scales

Manipulation of both electron and nuclear spins on sufficiently fast time scales.

Future:

Spintronics is still in its infancy and it's difficult to predict how it will evolve.

New physics is being discovered and new materials are being developed, such as magnetic semiconductors

Several experiments have been carried out for progress in transporting spins over long distances and in high electric fields that will probably prove successful in the near future.

Spintronics in INDIA

The technology wherein both the charge and spin of an electron is used to carry information has generated excitement for its potential in a wide range of applications.

"The first applications of spintronics having been demonstrated, there is tremendous interest in the development of the next spintronics device.

Spintronics biggest potential lies in embedded memories and non-volatile memory devices such as magnetoresistive random access memory (MRAM), which will revolutionize the memory market. Other applications include the use of spintronics in quantum computation and the development of the quantum computer. Spin transistors are also could well challenge the monopoly of semiconductor electronics.

Research in spintronics faces several challenges, especially handling-related issues. Because spintronic devices use magnetism and materials such as nickel, iron, cobalt — with alloys not commonly used in normal semiconductor electronics — there are difficulties in etching and patterning as well as in integrating the magnetic material into a silicon process for manufacturing MRAMs. The behavior of the magnetic element on a chip in both read and write modes could be quite a hurdle it is required to make MRAMs reliable.

V. CONCLUSION

Interest in spintronics arises from the problem of exhausting the fundamental physical limits of conventional electronics. However, complete reconstruction of industry is unlikely and spintronics is a "variation" of current technology.

The spin of the electron has attracted renewed interest because it promises a wide variety of new devices that combine logic, storage and sensor applications. Moreover, these "spintronic" devices might lead to quantum computers and quantum communication based on electronic solid-state devices, thus changing the perspective of information technology in the 21st century.

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REFERENCES

Journal Papers:

- [1] Jeremy J Ramsden Dept of advanced material, cranefield university, Bedfordshire, UK
- [2] N Taniguchi, "On the basic concepts of Nano Technology" Proc. Intl conference prod engng, Tokyo
- [3] D M Eigler & E K Schweizer "Positioning single atoms with a scanning tunnelling microscope" Nature (Lond.) 344 (1990)
- [4] B C Regan et al "surface tension driven nano electromechanical relaxation oscillator" Appl Phys Lett 86 (2005) 123119

Books:

- [5] Rainer Waiser (2nd edition), "Nano electronics and information technology - Advanced electronic materials & devices"