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BPSK Transmitter Design Using FPGA with DAC And Pulse Shaping Filter To Minimize Inter-Symbol Interference(ISI)

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ABSTRACT- *In contrast to the sophisticated implementation of binary phase shift keying (BPSK) transmitter using application specific integrated circuit(ASIC), mixer, and local oscillator(LO) for carrier signal; software defined radio(SDR) provides a high performance, efficient and re-configurable platform to integrate all these individual functions of BPSK transmitter. This work presents a tutorial exploitation to design and implement BPSK transmitter using field programmable gate array(FPGA) for digital signal processing. The DSP-based BPSK transmitter is developed and compiled to VHDL(VHSIC Hardware Description Language) netlist. For proper interfacing D/A converter(DAC) with FPGA, a HDL module of configurations of LTC-2624 Analog Module and clock synthesizer is integrated with the HDL netlist of BPSK transmitter. The cascaded pulse-shaping filter is a Gaussian-filter that is used to eliminate any high-frequency noise component including sharp transitions caused by ISI. Finally,the optimally synthesized netlist of the integrated design is implemented into Xilinx Spartan-3E FPGA development board with DAC. The verification of DAC output signal via oscilloscope shows the empirical real-time result similar to the simulated result. Further up-conversion for the BPSK transmitted signal to higher frequency can be done using external analog RF devices with some design modifications.*

Keywords- *BPSK, FPGA, DAC, ISI, VHDL.*

I. INTRODUCTION

BPSK Modulator is one of the binary modulation techniques. BPSK gives the high immunity against noise & interference & a very robust modulation. A digital phase modulation which is the case for BPSK modulation uses phase variation to encode bits, each modulation symbol is equivalent to one phase an often used illustration for digital modulation is the constellation. Intersymbol interference (ISI) occurs due to multi-path signal reflections & nonlinear frequency response. Pulse shaping limits the out of band signals. The cascaded pulse-shaping filter is a Gaussian-filter that is used to eliminate any high-frequency noise component including sharp transitions caused by Intersymbol interference.

This work does not only present design and implementation of DSP-based BPSK transmitter using FPGA, but also HDL (Hardware Description Language) module of configurations of expansion Analog Module (especially DAC) and clock synthesizer that controls FPGA system clock frequency. The implementation issues for integration of HDL netlist of BPSK transmitter and HDL module of setup configuration will also be addressed.

The aim of this project is to design and implement BPSK transmitter using field programmable gate array with DAC LTC 2624 (Spartan -3E FPGA development board) which can be used for digital signal processing (DSP) applications. The main objective of this work is to minimize the ISI i.e. (inter-symbol interference) induced by the BPSK modulator block by using pulse-shaping filter.

II. METHODOLOGY

Since the advent of wireless communications such as 3G and 4G, software radio (SR) or software defined radio (SDR) becomes dominant due to its highly configurable hardware and software platforms, as compared to the sophisticated and complicated hardware platforms [1]. SDR performs various intermediate frequency (IF) and baseband signal processing functions by using Digital Signal Processing (DSP) and logic algorithms [2]. The commonly used silicon solutions for SDR implementation are field programmable gate arrays (FPGAs), digital signal processors (DSPs), general purpose processors (GPPs), and application-specific integrated circuits (ASICs). FPGA offers the best solution in IF stage and wideband (WB) modem processing because it provides high speed, high level of integration, high flexibility, and low development costs, though it may have high power consumption due to inefficient use of the FPGA logic elements (slices) [3].

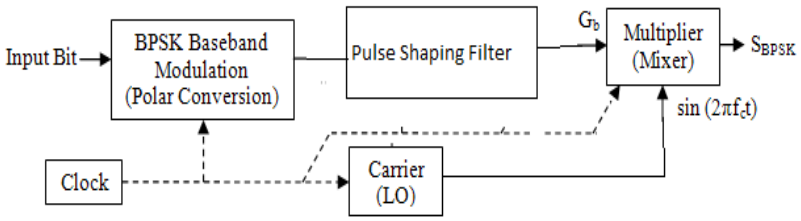

Fig. 1: BPSK transmitter using FPGA
BLOCK DIAGRAM

In SDR system, BPSK is a simple one-dimensional (1D) modulation scheme that the phase of carrier sinusoidal signal changes abruptly by 180^0 or π radian for every transition of modulating binary sequence (input bit) [4]. The block diagram of BPSK transmitter using FPGA is shown in Fig. 1. In BPSK baseband processing, the input bit with value of '0' or '1' is mapped to symbol with gain (G_b) of −1 or +1 respectively through polar conversion. At the same time, local oscillator (LO) generates carrier sinusoidal signal with frequency (f_c) to be mixed with G_b by multiplier to produce BPSK transmitted signal (S_{BPSK}). While clock with certain frequency (sampling rate) controls the timing of BPSK transmitter in FPGA.

Several researches on digital implementation of SDR-based BPSK have been done as in [5]-[8], but there still remain some critical issues of interfacing analog-to-digital converter (ADC) and digital-to-analog converter (DAC) with FPGA. This project does not only present design and implementation of DSP-based BPSK transmitter using FPGA, but also HDL (Hardware Description Language) module of configurations of expansion Analog Module (especially DAC) and clock synthesizer that controls FPGA system clock frequency. The implementation issues for integration of HDL netlist of BPSK transmitter and HDL module of setup configuration will also be addressed. Next, analysis reports for validating the timing and area constraints during processes of synthesis and FPGA implementation stage will be discussed. Lastly, the verification of real-time result (DAC output signal) is done via observation from oscilloscope.

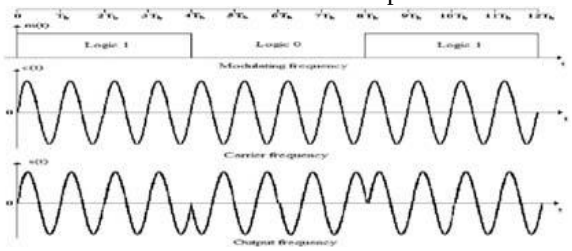

Fig. 2: BPSK waveforms

III. DESIGN OBJECTIVE

This project needs the conversion of explicit set of specifications two a bit stream which is given through design flow of FPGAs. Certain steps are followed to achieve this conversion

- Problem specification
- Validation of specifications
- Synthesis of design
- Indication of basic hardware design characteristics
- Bit stream generation

Once this flow is tested and verified, the design may be tested on a physical layer.

Next objective is to do HDL coding description of system
After validating the HDL code, BPSK transmitter is to be designed and validated using FPGA.

The project is divided into two phases:

1. SYSTEM LEVEL DESIGN AND SIMULATION
2. IMPLEMENTATIONS OF FPGA AND DAC & PULSE SHAPING FILTER.

Software Requirements:

- Xilinx ISE Design Suite 12.3_1

- ModelSim PE Student Edition 10.0c.
- Windows XP/Windows 7

IV. IMPLEMENTATION

The main aim of this project is to successfully implement the following design stages.

1. SYSTEM LEVEL DESIGN AND SIMULATION

1.1 Design and Simulation Using DSP Design Tools.

The DSP-based design of BPSK transmitter is developed in user-friendly DSP Design Tools i.e. Xilinx System Generator in VHDL/Matlab/ Simulink environment

1.2 HDL Design of Setup Configuration.

1.3 Integration of DSP Design and Setup Configuration.

The Verilog HDL module of setup configuration and Verilog HDL netlist of BPSK transmitter are verified firstly before combining both to become HDL module of integrated design

1.4 Synthesis of Integrated Design.

Although Xilinx ISE suite has its own synthesis tool Xilinx Synthesis Technology (XST), but it can only synthesize HDL netlist generated from System Generator.

2. IMPLEMENTATIONS OF FPGA AND DAC and Result

2.1 Software Implementation of FPGA Design.

The synthesis output files required by Xilinx ISE software are in EDIF (Electronic Design Interface File) and UCF (User Constraints File) formats.

The different equipment was used in accordance to a specific application or type of design entry and varied for different labs. For the most part we used two types of FPGA boards: DSP and Spartan-3E development board Starter kits.

2.2 Hardware Implementation and Result.

The DAC Channel output from LTC2624 Analog Module is connected to oscilloscope in order to display real-time result in analog domain. Observe the real-time result and simulated results of BPSK transmitted signal.

V. SPECIFICATIONS

Specifications are validated taking into account the available interfaces and features on FPGA evaluation board. Maximum clock source available on board is 50MHz. A Push-button is capable of driving logic-1 (high) when pressed. With this available property, a 'Reset' specification are frozen to Active-high assertion.

A DAC needed a SPI protocol based driving of output-digital data. With this into consideration the output driven through SPI protocol controller. And additional architectural module integrated.

VI. EXPECTED RESULT

This Project has presented a detailed guideline to design and implement the BPSK transmitter in Spartan-3E development board with DAC & pulse shaping filter. Two software packages namely Xilinx12.3_1 & ModelSim 10.0c used to implement and validate the results in terms of behavior, functionality, synthesis, timing, and area constraints. The similarity of empirical real-time and simulated results will show the success of FPGA and DAC implementations. On the other hand, timing issues such as sample rate, constraints, and matching should be analyzed in-depth if the input bit is coming from external source which not present on the FPGA board. By Inserting pulse-shaping filtering between polar conversion and mixer we can reduce inter-symbol interference (ISI) to enhance the receiver performance.

VII. CONCLUTION

Design & implementing hardware in FPGA is a formidable task. Based on the design specification, careful choice of implementation method and tools can save a lot of time and work. This paper has presented a guideline to design and implement the BPSK transmitter in Spartan3E FPGA development board with DAC in LTC2624 Analog Module& pulse-shaping filter. By inserting pulse-shaping filtering between polar conversion and mixer reduces ISI & enhance the performance. Precoding like source and channel coding can also be added in BPSK transmitter for error checking and control. This work can be extended for biomedical application such as Tele medicine, Biotelemetry & health medical care treatment for chronic diseases, implementation of CDMA Transmitter, Modified BPSK transmitter using FPGA for satellite communication.

REFERENCES

Journal Papers:

[1] J. Mitola, "The Software Radio Architecture," IEEE Commun. Mag., vol. 33, no. 5, pp. 26- 38, May 1995.
[2] J. E. Gunn, K. S. Barron, and W. Ruczczyk, "A Low-Power DSP Core Based Software Radio Architecture," IEEE J. Sel. Areas Commun., vol. 17, no. 4, Apr. 1999.
[3] M. S. Safadi and D. L. Ndzi, "Digital Hardware Choices for Software Radio (SDR) Baseband Implementation," in Proc. 2nd ICTTA'06, 2006, vol. 2, pp. 2623-2628.
[4] J. G. Proakis, Digital Communications, 5th ed., New York: McGraw-Hill, 2008.
[5] F. Ahamed and F. A. Scarpino, "An Educational Digital Communications Project Using FPGAs to Implement a BPSK Detector," IEEE Trans. Edu., vol. 48, no. 1, Feb 2005.
[6] K. E. Mohamed and B. M. Ali, "Digital Design of DS-CDMA Transmitter Using VHDL and FPGA," in Proc. Jointly Held with 7th MICC and 13th ICON, 2005, vol. 2, pp. 632-636.
[7] F. M. Demir, U. Kafadar, S. Dikmese, and H. Dincer, "FPGA Based Implementation of Communication Modulation," in Proc. 15th Signal Process. &Commun. Appl., 2007, pp. 1-4.
[8] Y. Tachwali and Hazem, "Implementation of a BPSK Transceiver on Hybrid Software Defined Radio Platforms," in Proc. 3rd ICTTA, 2008, pp.1-5.
[9] N. P. Cagigal and S. Bracho, "Algorithmic determination of linear feedback in a shift register for pseudorandom binary sequence generation," IEE Proc., vol. 133, Pt. G, No. 4, pp. 191-194, Aug. 1986.
[10] V. Oppenheim and R. W. Schafer, Discrete-time Signal Processing, 2nd ed., Upper Saddle River, New Jersey: Prentice-Hall, 1999.

Books:

[1] Digital Design Principles and Practices, Fourth edition. By john F. Wakerly.
[2] VHDL for Engineers by Kenneth L. Short (Pearson publication).