

Design of Low Power CMOS Ternary Logic Gates

¹Savitri Vanjol, ²Pradnya Pawar

^{1,2}Assistant Professor, ECE Dept, Dr.J.J.M.C.O.E., Jaysingpur, Kolhapur, Maharashtra, India

ABSTRACT— A novel low-power and high-performance Standard Ternary Inverter (STI) for CMOS technology is proposed in this paper. This inverter could be used as a fundamental block for designing other ternary basic logic gates. This circuit consists of only MOS transistors and capacitors without any area consuming resistors in its structure. Another great advantage of this design in comparison with the other designs, introduced before, is the leads to less power consumption. The proposed design has been simulated, using Tanner tool with 250nm CMOS technology. The simulation results demonstrate the superiority of the presented design with respect to other conventional designs in terms of power consumption and performance.

Keywords—Multivalued logic, ternary logic, Standard ternary inverter

I. INTRODUCTION

The intrinsic switching behavior of many electronic devices makes them appropriate for implementing binary digital integrated circuits. Powerful arithmetic components and tools have supported binary logic over the last two decades to obtain the present status [2]. The main disadvantages of the binary integrated circuits, which are the interconnection and pin-out problems, cause limitations on the number of connections inside and outside of the circuit [3]. With an increasing density of chips, the number of inter chip connections is greatly increased as more and more functions are put on the same chip; thus, the size and performance of the chip is mostly dominated by wiring rather than devices.

One of the most promising approaches to solve the interconnection problems is the use of multiple-valued logic (MVL) inside the VLSI chip. The number of interconnections can be directly reduced with multiple-valued signal representation. The reduced complexity of interconnections makes the chip area and the delay much smaller. MVL reduces the number of signals involved in the communication increasing their information content. In such a way, an interconnection-limited design can be realized with MVL in a smaller area and comparable performance than a classical binary design.

Among all MVL systems ternary logic has some advantages as given below

1. Since 3 is the smallest radix higher than binary, ternary functions and circuits have the simpler form and construction. They can be studied and discussed easily, yet they still display the characteristics of multivalued elements.
2. Since 3 is the digit nearest to $e = 2.718$, ternary circuits will be more economical according to this measure.
3. Since 3 is not an integral power of 2, research on ternary logic may disclose design techniques that are overlooked in the study of binary or quaternary logic.[4]

Inverter is the most fundamental part in any logic and most of the other basic operators such as NOR and NAND are realized according to its structure. This fact is valid even for higher radices especially for radix-3 (ternary). Hence, designing an efficient ternary inverter cell leads to enhancement of overall system performance. In addition to the inversion operation, the inverter is also a great driver and its driving capability is very important. Unlike binary logic, in ternary logic there are three ways to define the inverter.

Ternary Inverters are defined as follows:

$$\bar{x}^i = \begin{cases} i & \text{if } x=1 \\ 2-x & \text{if } x \neq 1 \end{cases} \quad (1)$$

By choosing the values 0, 1, 2 for i , the ternary inverter can be Negative (NTI), Standard (STI) and Positive (PTI), respectively. In this paper, logics "0", "1" and "2" are equivalent to 0, $1/2V_{DD}$ and V_{DD} voltages, respectively.

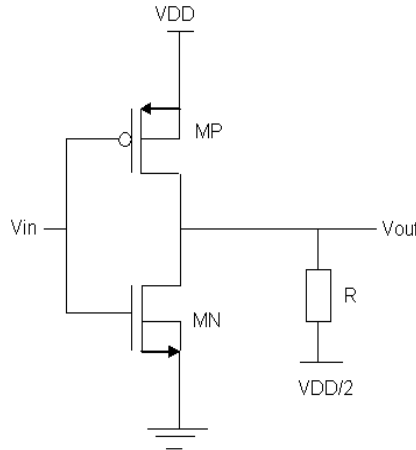


Figure 1. Different designs for STI with a single resistor.

II. PREVIOUS CMOS STI DESIGNS

Several types of CMOS STIs have been presented since the emerging of CMOS technology. However, they utilize large off-chip resistors and depletion transistors, which are not suitable in recent technologies. Some new structures for CMOS analog inverter have been presented, which could be considered as inverters for any arbitrary radix, including radix-3 [5-7]. However, an analog inverter may not be really used as a traditional STI, because of losing the noise immunity in comparison with real STI.

Fig. 1 shows conventional structures for STI in CMOS technology [8]. In this design, transistors are connected together in the same manner as for binary inverter. The output of the inverter is connected to a $VDD/2$ power supply by means of a resistor, which is considerably larger in comparison with the resistance of the turned on transistors. If the input logic becomes “0”, MP2 becomes turned on and MN2 becomes turned off. Hence, the output goes up to logic “2”. Contrariwise, if the input logic becomes “2”, MP2 becomes turned off and MN2 becomes turned on. Hence, the output goes down to logic “0”. Needing $VDD/2$ power supply and static power consumption, equals to $VDD^2/2R$, when the input logic is “0” or “2” are the disadvantages of this design.

III. PROPOSED DESIGN

Previously presented design has some major disadvantages such as extra power supply and use of large resistors, which are hard to implement and occupy large chip area and unfeasibility of implementation in standard CMOS technology.

To overcome these disadvantages, a new design for STI is proposed, which is shown in Fig. 2. The main idea of this design is based on weighting method, which adds output values of a PTI and a NTI cell by means of a capacitor divider. Two pairs of MOSFETs, which implement NTI and PTI, together with two capacitors, are the materials of this design. Transition points of PTI and NTI are adjusted by changing the aspect ratio of the transistors. The outputs of PTI and NTI gates are then connected together by means of two capacitors which could make a weighted sum of the relevant inputs. The voltage of the connection node of capacitors is as follows:

$$V_O = \frac{C_n V_{NTI} + C_p V_{PTI}}{C_n + C_p} \quad (2)$$

To have same weighting factor for two C_n and C_p capacitors, they should be identical. Hence the output voltage is as follows:

$$V_O = \frac{V_{NTI} + V_{PTI}}{2} \quad (3)$$

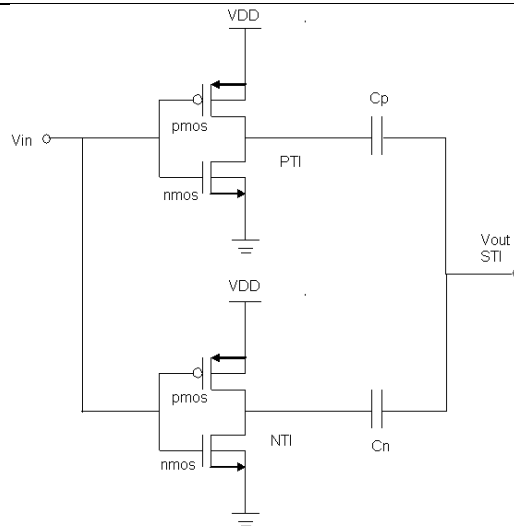


Figure 2. Schematic of proposed design for STI.

Thus, the output voltage of STI will be the mean value of the NTI and PTI output voltages. By utilizing the main structure, it is also possible to implement two other basic ternary gates, NAND and NOR.

Fig. 3. shows the ternary NAND gate and Fig.4. Shows the Ternary NOR gate. In Fig.3. The four upper transistors implement Positive Ternary NAND gate (PTNAND). The output of PTNAND goes down to “0” just when both inputs are in state “2”. Otherwise, output is in state “2”. Contrariwise, four downer transistors make Negative Ternary NAND gate (NTNAND). The output of NTNAND goes up to “2” just when both inputs are in state “0”. Otherwise; output is in state “0”.

Finally, connecting these local outputs by means of two capacitors make a Ternary NAND gate. In the same manner as for TNAND, the four upper transistors in Fig. 4 implement Positive Ternary NOR gate (PTNOR). The output of PTNOR goes up to “2” just when both inputs are in state “0”. Otherwise, output is in state “2”.

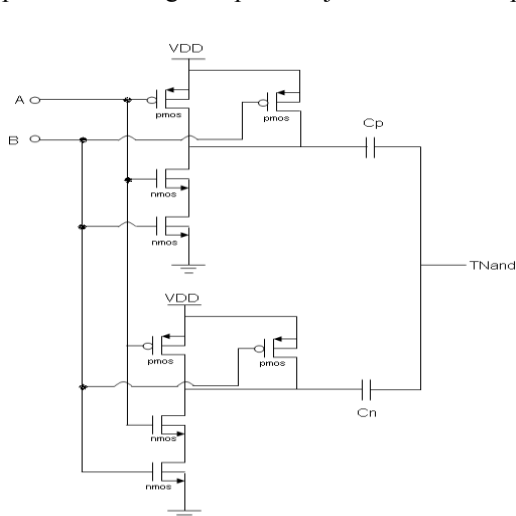


Figure 3. Ternary NAND gate

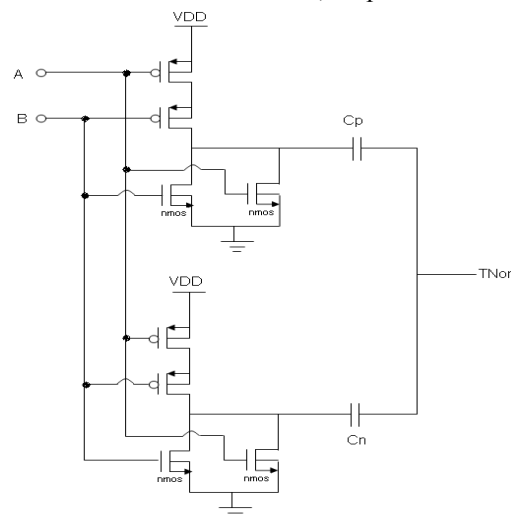


Figure 4. Ternary NOR Gate.

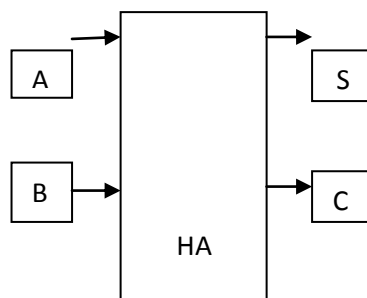


Figure 5. Ternary half adder.

Contrariwise four downer transistors make Negative Ternary NOR gate (NTNOR). The output of NTNOR goes down to “2” just when both inputs are in state “0”. Otherwise, output is in state “2”. At last, connecting these local outputs by means of two capacitors makes a Ternary NOR gate. It is also possible to implement the half adder using the basic gates. The schematic of half adder is same as that of the binary half adder. It makes use of an EXOR, AND and OR gates. The inputs to half adder are A and B and the outputs are sum(S) and carry(C). Fig 5 shows the symbolic representation of half adder. The block half adder (HA) has the EXOR (which is implemented using NAND gates), AND and OR gates.

IV. SIMULATION RESULTS

In this section the operation and performance of the proposed designs are examined. Simulations have been done using Synopsys Tanner tool with standard 250nm CMOS technology at 5V supply voltage. As the power supply Voltage is 5V, valid voltage levels are 0V, 2.5V and 5V. The input and output signals of the proposed STI, the proposed TNAND and TNOR gates, and half adder are shown in Fig.6, Fig.7, Fig.8 and Fig.9 respectively. The output signals prove the authenticity of the proposed designing method.

The proposed design is compared with the other conventional design in terms of performance and power consumption. Therefore, simulations are performed for all designs with the same 250nm CMOS technology. The resistors of the designs are adjusted such that leads to the best simulation results at the outputs

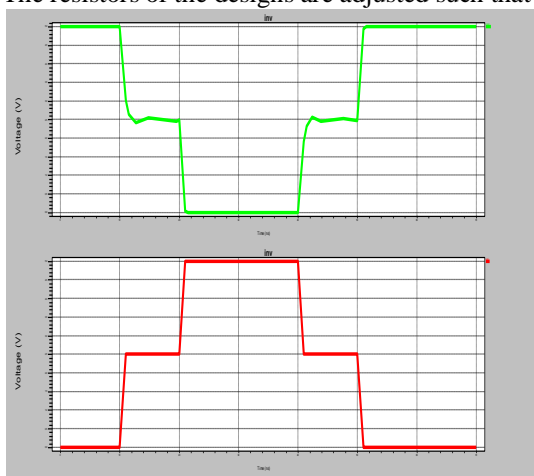


Figure 6. The output and input signals of proposed Ternary inverter

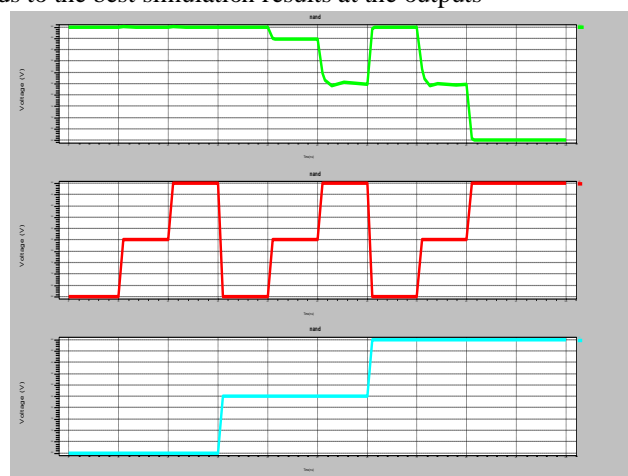


Figure 7. The output and input signals of proposed ternary NAND gate

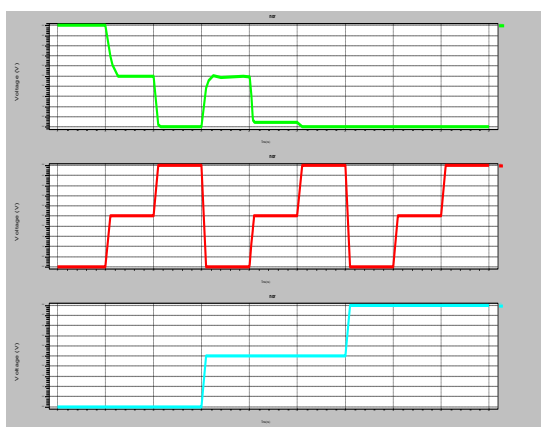


Figure 8. The output and input signals of proposed ternary NOR gate

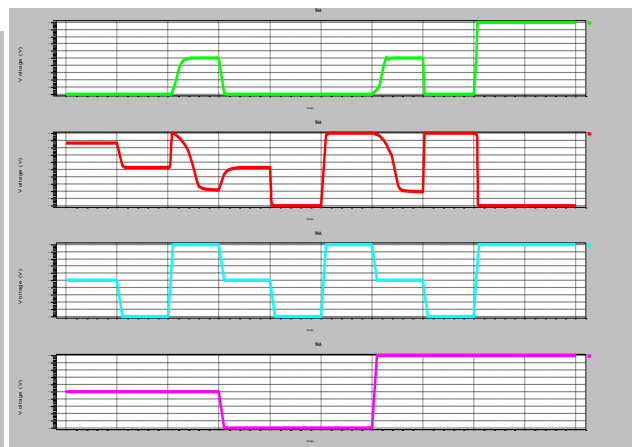


Figure 9.: The output and input signals of proposed ternary half adder

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The total power consumed due to the voltage sources is compared for both existing and the proposed ternary inverter. Table 1 gives the power consumed by the existing and proposed design. From the table it can be seen that the power consumed by the proposed design is very less compared to the resistor circuit.

Table 1: Power results of ternary inverter.

L=0.25 μm , V _{dd} =5V			
W _p =5.2 μm W _n =2.5 μm	power consumed due to 5V supply	power consumed due to 2.5V supply	Total power
Existing design R=100k	124.29016 μW	62.14471 μW	186.43487 μW
Proposed design C=0.01pF	1.47537nW		1.47537nW
W _p =2.13 μm W _n =1.0 μm			
Existing design R=100k	123.29177 μW	61.64560 μW	184.93737 μW
Proposed design C=0.01pF	1.16800nW		1.16800nW

V. CONCLUSION

A novel low-power design for Standard Ternary Inverter is proposed. This inverter structurally is capable of being used for implementing other standard ternary functions. Some of the main advantages of the proposed design compared with the previously proposed designs are as follows:

1. Containing no ohmic resistors and hence simpler implementation and very smaller area.
2. Capability of being implemented in standard CMOS technology.
3. Generation of all the possible ternary inverted outputs

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