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High Speed, Low power and Area Efficient Processor Design Using Square Root Carry Select Adder

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***Abstract**: Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. From the structure of the CSLA, it is clear that there is scope for reducing the area and power consumption in the CSLA. This work uses a simple and efficient gate-level modification to significantly reduce the area and power of the CSLA. Based on this modification 8-, 16-, 32-, and 64-b square-root CSLA (SQRT CSLA) architecture have been developed and compared with the regular SQRT CSLA architecture. The proposed design has reduced area and power as compared with the regular SQRT CSLA with only a slight increase in the delay. This work evaluates the performance of the proposed designs in terms of delay, area, power, and their products by hand with logical effort and through custom design . The results analysis shows that the proposed CSLA structure is better than the regular SQRT CSLA.*
***Index Terms: D**ata processing, processors, gate level modification. Delay, power, area, speed.*

I. Introduction

The saying goes that if you can count, you can control. Addition is a fundamental operation for any digital system, digital signal processing or control system. A fast and accurate operation of a digital system is greatly influenced by the performance of the resident adders. Adders are also very important component in digital systems because of their extensive use in other basic digital operations such as subtraction, multiplication and division. Hence, improving performance of the digital adder would greatly advance the execution of binary operations inside a circuit compromised of such blocks. The performance of a digital circuit block is gauged by analyzing its power dissipation, layout area and its operating speed.Generally in VLSI techniques we need to satisfy any two of the following criteria such as area, speed and power. The normal adders which we use are satisfying only one trade off but in this SQRT CSLA there is trade off in both area and power. Here we are using 6-Bit BEC(binary to excess-1 converter) to implement the adder element.

II. Literature Survey

In this work we will review the implementation technique of several types of adders and study their characteristics and performance. These are

1. Ripple carry adder, or carry propagate adder,
2. Carry look-ahead adder
3. Carry skip adder,
4. Manchester chain adder,
5. Carry select adders
6. Square root Carry select adders

For the same length of binary number, each of the above adders has different performance in terms of Delay, Area, and Power.

Parallel adders are digital circuits that compute the addition of variable binary strings of equivalent or different size in parallel.

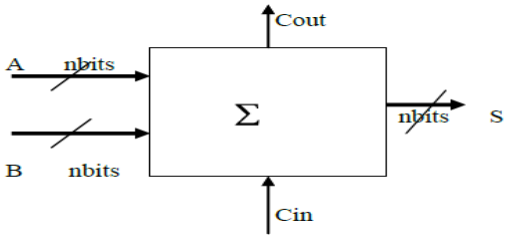


Fig. 1. Block Diagram Of Parallel adders

In ripple carry adders, the carry propagation time is the major speed limiting factorMost other arithmetic operations, e.g. multiplication and division are implemented using several add/subtract steps. Thus, improving the speed of addition will improve the speed of all other arithmetic operations. Accordingly, reducing the carry propagation delay of adders is of great importance. Different logic design approaches have been employed to overcome the carry propagation problem. One widely used approach employs the principle of carry look-ahead solves this problem by calculating the carry signals in advance, based on the input signals. This type of adder circuit is called as carry look-ahead adder (CLA adder).

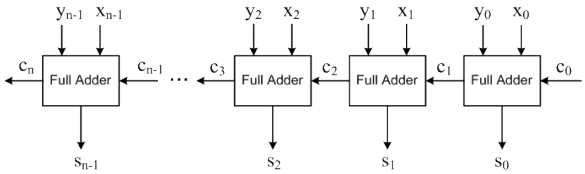


Fig. 2. Block Diagram Of Carry Look ahead adders

A carry-skip adder consists of a simple ripple carry-adder with a special speed up carry chain called a **skip chain**. This chain defines the distribution of ripple carry blocks, which compose the skip adder.

Carry Skip Mechanics

The addition of two binary digits at stage i, where i 0, of the ripple carry adder depends on the carry in, ***Ci*** , which in reality is the, in order to calculate the sum and the carry out, ***Ci+1*** , of stage i, it is imperative that the carry in, ***Ci***, be known in advance. It is interesting to note that in some cases ***Ci+1*** can be calculated without knowledge of ***Ci***.

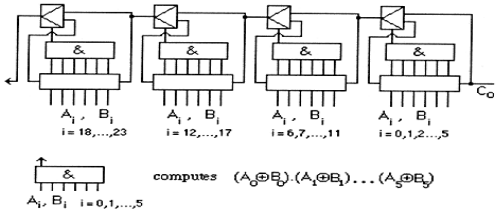


Fig. 3. Block Diagram Of Carry Skip adders

A ripple carry adder allows you to add two k-bit numbers. We use the half adders and full adders and add them a column at a time.Let's put the adder together one step at a time. Arithmetic operations like addition, subtraction, multiplication, division are basic operations to be implemented in digital computers using basic gates like AND, OR, NOR, NAND etc. Among all the arithmetic operations if we can implement addition then it is easy to perform multiplication (by repeated addition), subtraction (by negating one operand) or division (repeated subtraction).Half Adders can be used to add two one bit binary numbers. It is also possible to create a logical circuit using multiple full adders to add N-bit binary numbers.Each full adder inputs a Cin**,** which is the Cout of the previous adder. This kind of adder is a Ripple Carry Adder, since each carry bit "ripples" to the next full adder.

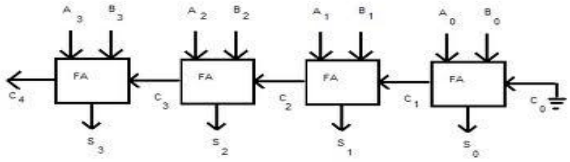


Fig. 4. Block Diagram Of Ripple Carry adders

The concept of the carry-select adder is to compute alternative results in parallel and subsequently selecting the correct result with single or multiple stage hierarchical techniques [8]. In order to enhance its speed performance, the carry-select adder increases its area requirements. In carry-select adders both sum and carry bits are calculated for the two alternatives: input carry “0” and “1”. Once the carry-in is delivered, the correct computation is chosen (using a MUX) to produce the desired output. Therefore instead of waiting for the carry-in to calculate the sum, the sum is correctly output as soon as the carry-in gets there. The time taken to compute the sum is then avoided which results in a good improvement in speed.

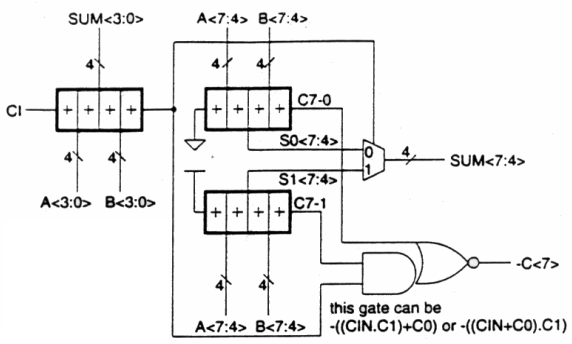


Fig. 5. Block Diagram Of Carry Select adders

The Manchester Carry-Chain Adder is a chain of pass-transistors that are used to implement the carry chain. During precharge, all intermediate nodes (e.g. $Cout_0$) are charged to Vdd. During the evaluation phase, Cout_k is discharged if there is an incoming carry Cin_0 and the previous propagate signals ($P_0...P_{k-1}$) are high. Only 4 diffusion capacitances are present at each node, but the distributed RC-nature of the chain results in a delay that is quadratic with the number of bits. Transistor sizing was performed to improve performance. The details are elaborated on in the design strategy section.

III. Proposed Algorithm

The basic idea of this work is to use Binary to Excess-1 Converter (BEC) instead of RCA with cin=1 in the regular CSLA to achieve lower area and power consumption [2]–[4]. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure. As stated above the main idea of this work is to use BEC instead of the RCA with Cin=1in order to reduce the area and power consumption of the regular CSLA. To replace the n-bit RCA, an n+1bit BEC is required. A structure and the function table of a 4-b BEC. Fig. 6 illustrates how the basic function of the CSLA is obtained by using the 4-bit BEC together with the mux. One input of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another input of the mux is the BEC output. This produces the two possible partial results in parallel and the mux is used to select either the BEC output or the direct inputs according to the control signal Cin. The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed. The Boolean expressions of the 4-bit BEC is listed as (note the functional symbols ~NOT, & AND, ^XOR). The Modified CSLA architecture has been developed using Binary to Excess -1 converter (BEC). This paper proposes an efficient method which replaces a BEC using common Boolean logic. The result analysis shows that the proposed architecture achieves the three folded advantages in terms of area, delay and power.

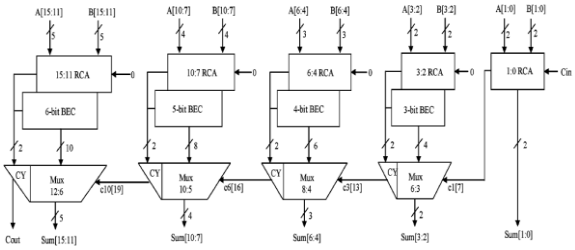


Fig. 6. Block Diagram Of proposed sqrt Carry Select adders

IV. 6-BIT BEC

A BEC(binary to excess-1 converter) is a converter which provides the excess 1 value of a corresponding code which is provided at the input.

B[3:0]	X[3:0]
0000	0001
0001	0010
⋮	⋮
1110	1111
1111	0000

Table.1. BEC input-output table

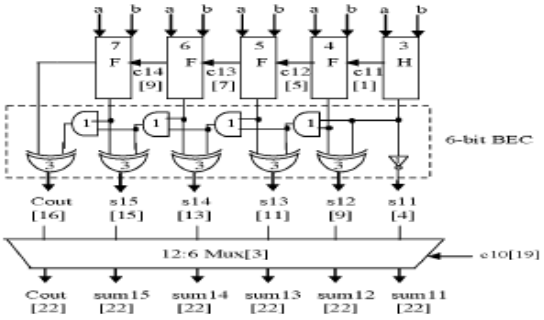


Fig. 7. Block Diagram Of 5 bit BEC

V. Simulation Results

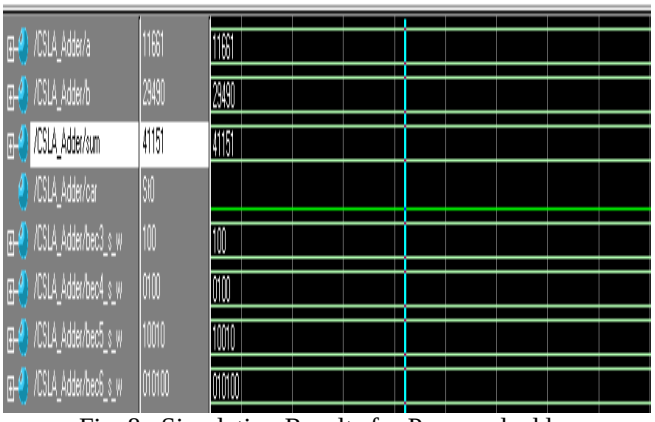


Fig. 8. Simulation Results for Proposed adder

VI. Rtl Schematic Layout & Floor Plan In Fpga

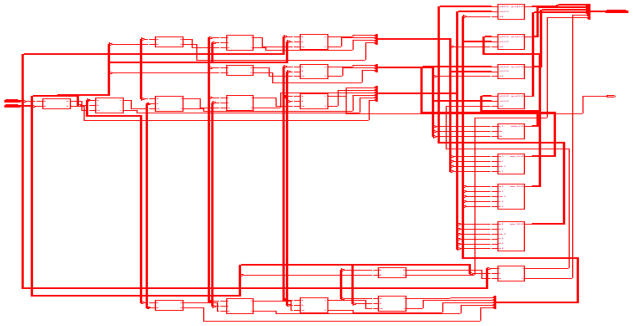


Fig. 9. RTL schematic layout

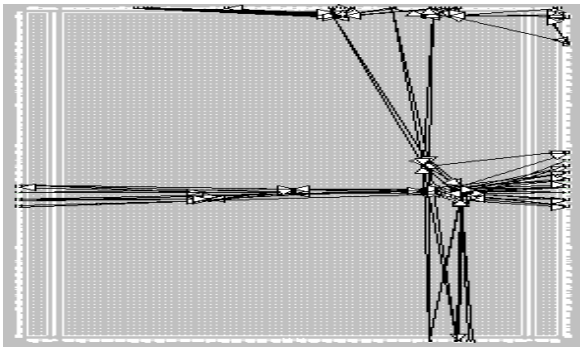
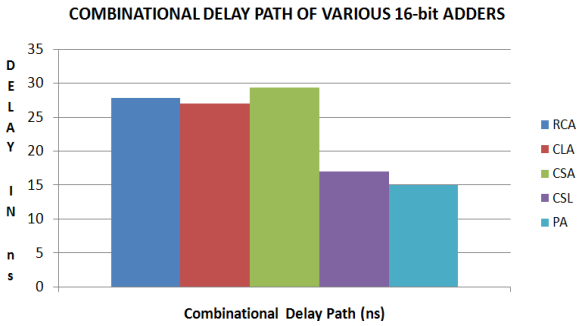
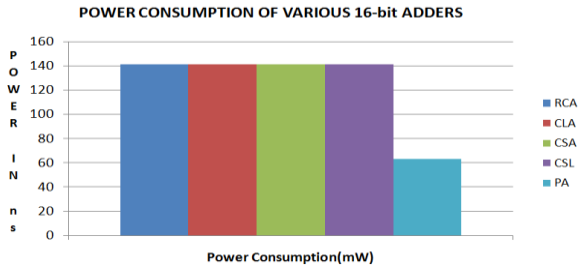


Fig. 10. Floor plan in FPGA

VII. Comparison of Area, Speed and Power

S.No	Parameters	RCA	CLA	CSA	CSL	PA
1	2 Input Xor Gate	32	32	-	-	-
2	3 Input Xor Gate	-	-	16	48	41
AFTER SYNTHESIS						
3	Number of Slices	19	18	22	18	25
4	4 input LUT	33	32	39	32	44
5	Bonded IOB	50	50	50	50	49
6	Combinational Delay Path (ns)	27.81	27.07	29.38	17.03	14.97
AFTER MAPPING						
7	4 Input LUT	33	32	39	32	44
8	Number of Slices	24	24	25	21	25
9	Gate Count	198	192	234	192	267
AFTER PLACE AND ROUTE						
10	External IOB	50	50	50	50	49
11	Number of Slices	24	24	25	21	25
POWER CONSUMPTION						
12	Power Consumption(mW)	141	141	141	141	63





VIII. Conclusion

The Proposed adder is very faster when compared to other conventional adders. The proposed adder consumes low power when compared to other conventional adders. Hence a high speed low power adders is proposed. In this proposed adder a set of 20 bits will be evaluated in just 8 clock pulses.

Acknowledgement

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