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Re-configurable Optimized Area Turbo Decoder for Wireless Applications

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Abstract: *Today, the wireless communication is an emanating requirement of day to day process. Due to the noisy environment in wireless communication there is a need of coding system, which can provide high data rate with error free communication. The turbo codes also known as Parallel Convolutional Concatenated Code (PCCC) provides high data rate with bit error rate performance improvement in communication system. With the advent demand of miniaturization, an area efficient turbo decoder of constraint length 3 is proposed in this paper. The turbo decoder used a single SISO (Soft Input Soft Output) decoder architecture in this paper to reduce the area consumption. The SOVA (Soft Output Viterbi Algorithm) is used as a decoding algorithm in SISO decoders. It is based on two step algorithm. The proposed design is simulated using Matlab and synthesized on Xilinx Virtex-2p (xc2vp30-ff896-5) FPGA. The performance of proposed Turbo decoder will be compared for FPGAs in terms of number of slice Flip-flops, LUTs and frequency. The Synthesis results show a 3% improvement in the utilized no. of slice flip-flop and 49% improvement in terms of frequency.*

Keywords: *PCCC, SOVA, Error Control Codes, Convolutional Code, FPGA, SISO*

I. Introduction

The Parallel Concatenated Convolutional Codes known as Turbo Codes are one of the error correcting code used in wireless communication system. These codes are preferable choice in various applications due to its inherent advantages such as high transmission rate, very high system throughput and BER (Bit Error Rate) improvement at low SNR etc. In mobile communication standards such as WiMAX, DVB-S2 (Digital Video Broadcasting) and CDMA2000 1x turbo codes are used. Turbo Codes are used for LTE (long term evolution) system for its good error correction ability and anti-interference ability. The analysis of various decoding algorithms such as MAP (Maximum a posteriori), LOG-MAP and MAX-LOG-MAP algorithm has been done for LTE system [1]. It has been done for different block length and iterations etc. Turbo codes are iteratively decoded by using trellis based soft-output decoding algorithm in SISO (Soft input soft output) decoders. The turbo code decoding algorithms are MAP, LOG-MAP, MAX-LOG-MAP and SOVA. A comparative performance analysis of LOG-MAP and SOVA and MAX-LOG-MAP and SOVA has been given in wireless communication and wireless OFDM system respectively [2] [3]. LOG MAP and MAX-LOG-MAP give better results in terms of performance as compared to SOVA but complexity increases simultaneously. There are various applications in which all the information do not require equal importance. By Unequal Error Protection (UEP) method the important message is more protected than the other message bits [4]. The BER performance of SOVA is improved by using unequal error protection method.

Several modifications over SOVA have been incurred to improve its performance. A modification over SOVA is presented to enable efficient hardware implementation [5]. The Battail rule (BR) in SOVA is simplified to approximate the concurrent path reliability values with the corresponding metric differences. It performs equivalent to MAX-LOG-MAP. Another modification over SOVA detector is to quasi reduced its state for magnetic recording read channel [6]. The states are reduced by the use of decision feedback, which maps the storage block of the trellis onto a reduced state trellis and keeps the trellis state metric computation on the original full-state trellis. A modification over SOVA has been done [7]. The FPGA implementation of turbo decoder using MSOVA (modified SOVA) for CDMA 2000 gives equivalent results to MAX-LOG-MAP in terms of performance. The complexity of MSOVA is equivalent to SOVA. A remedy is proposed for the exaggerated extrinsic information produced by SOVA [8]. The idea is to reduce the correlation between the intrinsic information and extrinsic information, so attenuators are applied to the immediate output of the SOVA and another applied to the extrinsic information. This modification results in performance improvement.
Power and area efficient turbo decoder for mobile application has been presented [9]. It is based on two step SOVA and used traceback algorithm. Due to the inherent demand of miniaturization in wireless communication, in this paper an area efficient turbo decoder design is proposed. The turbo decoder used SOVA algorithm as the decoding algorithm.

This work is organized as follows. Section II includes the Single input single output (SISO) processor used in turbo codes. The methodology of proposed turbo decoder is also discussed in this section. The

simulation results including graphs have been shown and discussed in section III. The hardware synthesis results using FPGA in terms of resource utilization has been shown in section IV. Finally, the conclusions are summarized in section V.

II. Turbo Decoder

A turbo decoder consists of soft input soft output (SISO) decoder. This SISO decoder can be mapped to any algorithm such as MAP, MAX-LOG-MAP and SOVA etc. The decoded bit sequences are iteratively decoded by SISO decoders, interleaver and deinterleaver respectively in turbo decoders. The SISO decoder [10] is shown in figure 1.

Fig. 1 SISO Decoder

As shown in the figure the decoder soft output is given by the equations 1 and 2.

$$L_{lr} = L_d + L_{ex} \quad (1)$$
$$L_d = L_c + L_{ap} \quad (2)$$

Where L_{lr} is the decoder soft output also called the log-likelihood ratio of the decoder. $L_{ex}$is the extrinsic information worked as an a priori information for next iteration. $L_d$is the posteriori value, which is equal to the sum of L_{ap} and L_c. $L_c$is the log-likelihood ratio of the channel output. It is scaled by the channel reliability. It is also known as the received systematic input to the decoder. $L_{ap}$is a priori information of the decoder retrieved by the previous iteration.

In this paper SOVA decoder is used as SISO decoder. Generally in turbo codes two or more than two SISO decoders are used. In the proposed decoder only one SISO decoder is used. If we observe the utilization efficiency of SISO decoders then at one time only one decoder will work and other one will be idle. So in this paper only one SISO decoder using SOVA algorithm is used. The single SISO turbo decoder is shown in figure 2.

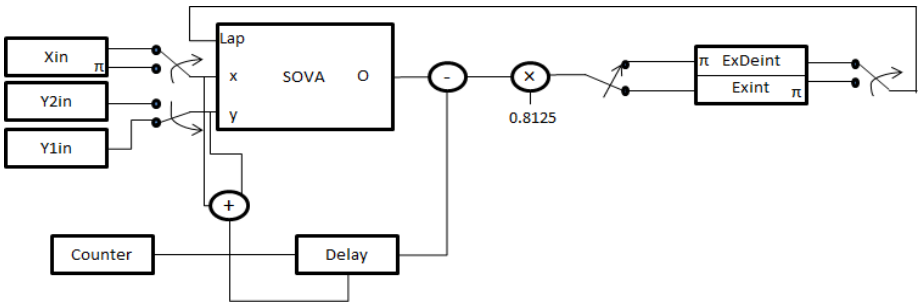

Fig. 2 Single SOVA Turbo Decoder

Where Xin is the noisy systematic bits, Y1in and Y2in are noisy parity bits 1 and 2 respectively. SOVA decoder is connected to Xin and Y1in at one time and at another time to interleaved value of Xin and Y2in. The extrinsic information is interleaved for first time and deinterleaved for the second time to generate the priori information for next iteration as shown. At both the times a posteriori value is subtracted from SISO output and with the help of delay and counter output is generated. The path metric calculation for SOVA is given by the equation 3 and 4.

$$M_{0k} = M_{k-1} - (1/2)L_{apk} + \frac{L_c}{2}(y_k x_k + z_k u_k) \quad (3)$$
$$M_{1k} = M_{k-1} + (1/2)L_{apk} + \frac{L_c}{2}(y_k x_k + z_k u_k) \quad (4)$$

Where M_{0k} and M_{1k} represents the path metric at stage k for binary 0 and 1 respectively. M_{k-1}represent the previous path metric. $L_{apk}$is a priori information at stage k. L_c is the channel reliability value. $y_k z_k$is systematic and parity bits received from the channel and $x_k u_k$ is the branch word associated with this edge. At each stage

M_{0k} and M_{1k} are compared and their difference represented by Δ with the highest value is stored for entire block.

The SOVA algorithm used in the proposed decoder are designed using the two step algorithm. The two step SOVA algorithm has been shown in figure 3.

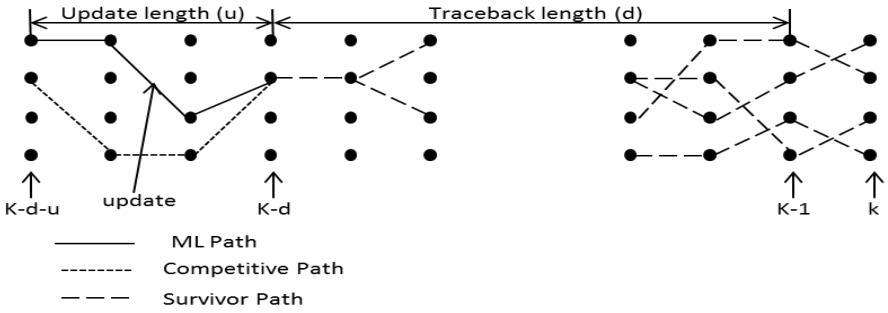

Fig. 3 Trellis Diagram for Two Step SOVA Decoding

The trellis diagram is divided into two paths: the traceback and the update process. The SOVA algorithm finds the maximum likelihood path during the traceback process. The traceback path is from k to k-d, where d is the traceback length. The Δ will be updated during the update process. The update path is from k-d to k-d-u, where u is the update length. The formula for updation of Δ is given in equation 5.

$$\Delta_t = \min_{v_{MLt} \neq v_{CMPt}} [(\Delta_{k-d}, \Delta_t)] \qquad for\ t = (k-d) \ldots\ldots (k-d-u) \qquad (5)$$

v_{ML} and v_{CMPt} are the decoded bits of Maximum Likelihood path and the competitive path at the trellis stage.

III. Proposed Decoder Simulations

The proposed turbo decoder is simulated using Matlab. The simulation graphs for various parameters have been shown in figure 4, 5, 6, 7and 8. The information signal is shown in figure 4. Then the channel signal and AWGN (Additive White Gaussian Noise) is shown in figure 5 and 6 respectively. The received bits to the decoder or decoder input are shown in figure 7. In figure 8 the received bits vs. noise graph has been shown.

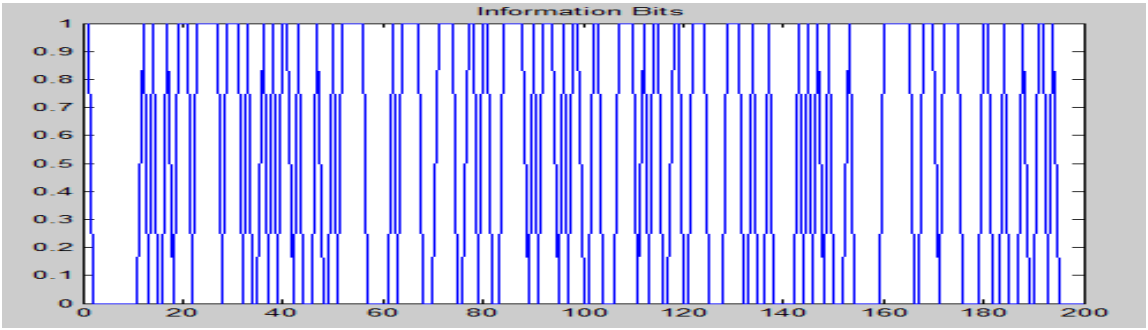

Fig. 4 Simulation Graph for Information Bits

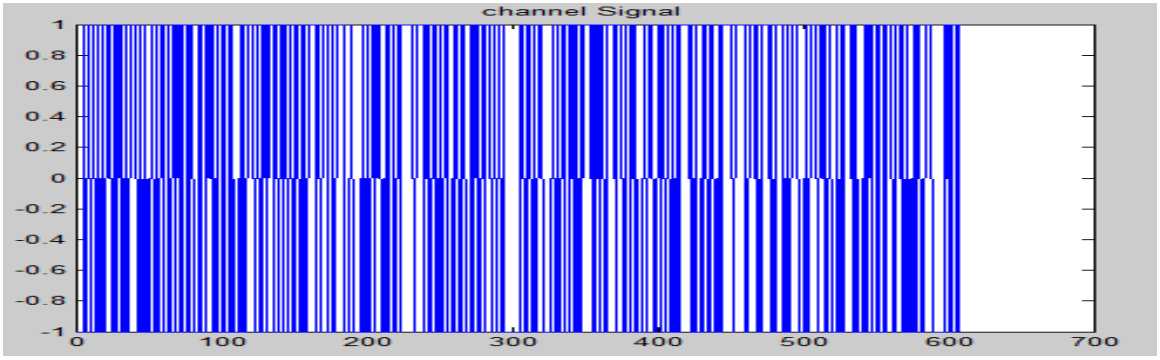

Fig. 5 Simulation Graph of Channel Signal

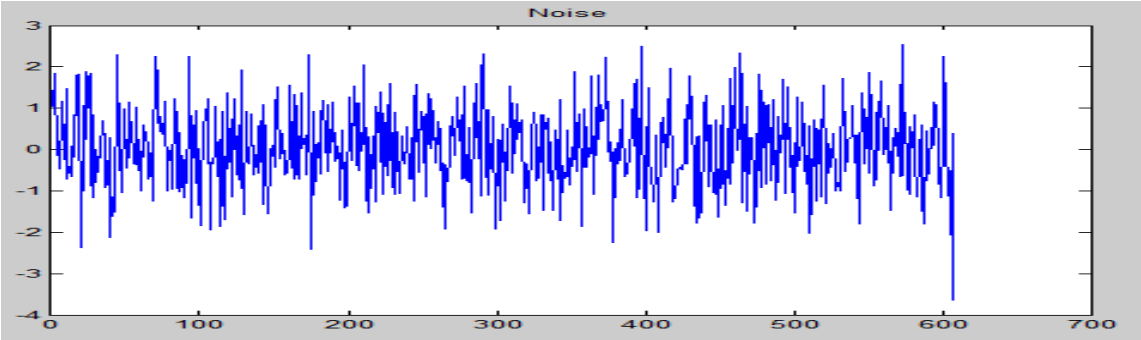

Fig. 6 Simulation Graph of AWGN Noise

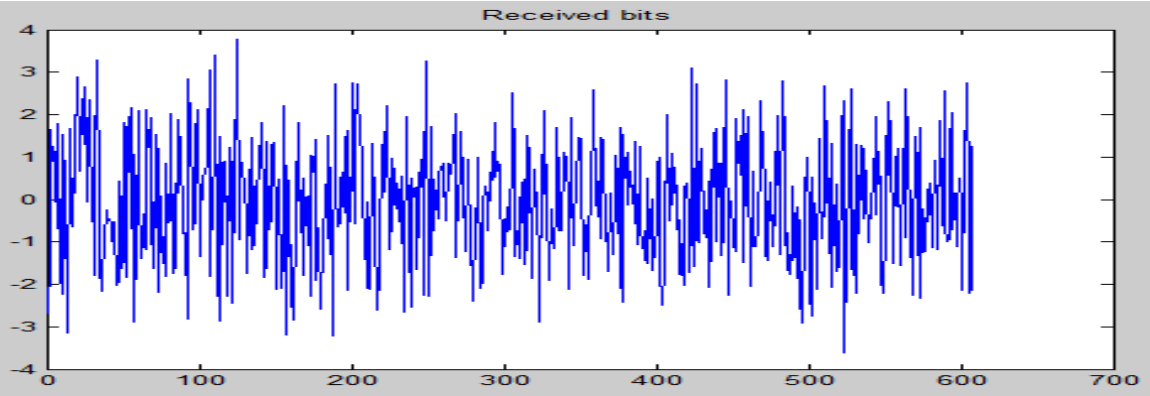

Fig. 7 Simulation Graph of Decoder Input

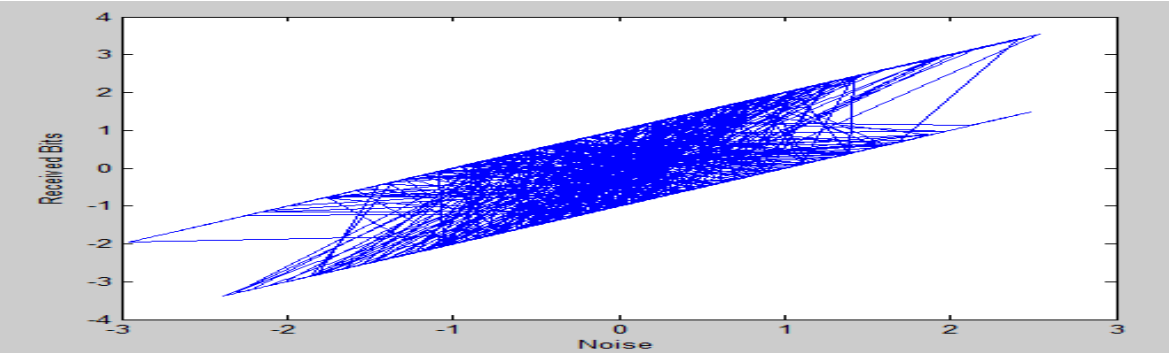

Fig. 8 Simulation Graph of Received Bits vs. Noise

IV. Hardware Analysis

The proposed Turbo Decoder was implemented using VHDL (VHSIC Hardware Description language), which offers high abstraction level during the implementation. The VHDL description is synthesized on Xilinx Virtex-2p (xc2vp30-ff896) FPGA with a speed grade of -5. FPGA (Field Programmable Gate Array) is a reconfigurable device has inherent advantages over ASIC (Application Specific Integrated Circuits). The synthesis tool used to measure the performance of proposed decoder is ISE 10.1. Synthesis is the process of converting the algorithm in the RTL code into a set of hardware realizable components like AND and OR gates The RTL view of Turbo decoder is shown in figure 9. The RTL (Register-transfer-level) abstraction is used to create the high level abstraction of the design by using HDL languages such as Verilog and VHDL. This high level abstraction can be converted into the lower level representation, where the wiring connection can be derived. The table 1 show the parameters used in the hardware implementation of the proposed decoder and the resource utilization summary is shown in table 2.

Fig. 9 RTL View

Table 1
List of Turbo Decoder Specifications

Constraint Length	3
Polynomial Generator in Octal Notation	$(7,5)_8$
Feedback Generator	7
Encoder Type	RSC
Input Bitwidth	5
Decoding Algorithm	SOVA
Survivor Memory	Register Traceback

Table 2
Resource Utilization Summary

xc2vp30ff896-5		
Logic Utilization	Used	Utilization
Number of slices	1022	7%
Number of slice flip-flop	1236	4%
Number of 4 I/p LUTs	1733	6%
Number of bonded IOBs	61	10%
Number of GCLKs	1	6%
Number of BRAM	26	19%
No. of adder & Subtractor	52	
No. of Counter	4	
No. of registers	1195	
Frequency	118.732MHz	

The parameters used in the resource utilization are number of slices, slice flip-flop, 4 I/P LUTs, counters and registers etc. The comparison between the proposed encoder and existing encoder has been shown in table 3 and the bar graph is presented in figure 10.

Table 3
Comparison between Proposed and Existing Decoder

	Proposed (Virtex2p)		**Existing (Virtex5)**	
Logic Utilization	Used	Utilization	Used	Utilization
Number of slices	1022	7%	3792	7.3%
Number of slice flip-flop	1236	4%	15168	7.3%
Number of 4 I/p LUTs	1733	6%	15114	7.2%
Frequency	118.732 MHz		60 MHz	

In [11], the turbo Decoder is synthesized using Virtex-5 FPGA. The frequency used in [11] is 60 MHz. The parameters for the comparison are no. of slices, slice FF, LUTs and frequency. As shown in the graph the utilized no. of slices, slice FF and LUT are less as compared to [11]. The proposed decoder results in an optimized area performance. The frequency of the proposed decoder is 118.73 MHz, which is very high as compared to existing decoder (60 MHz).

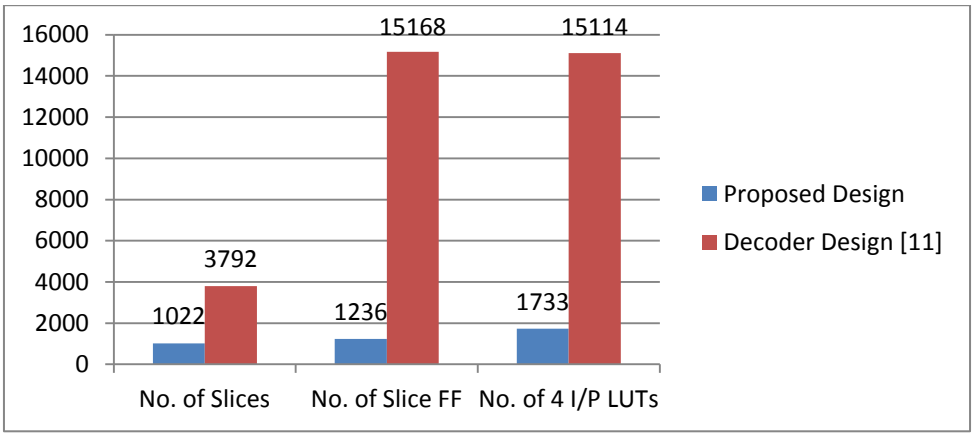

Fig. 10 Comparison Graph between proposed and existing [11] Decoder

V. Conclusion

Due to the highly error prone communication environment, there is a constant need of error control codes in wireless communication. The turbo codes are used as error correcting codes provide low BER and high throughput. The performance of any code depends on the decoding algorithm. In this paper a single SISO architecture using SOVA decoding algorithm is used. The area consumption is reduced by using a single SISO structure as compared to multiple in others. The SOVA decoder is based on the two step algorithm in which with the traceback process the Δ will be updated for the update length. The proposed decoder is synthesized using Xilinx virtex2p (xc2vp30-ff896-5). The synthesis tool used to measure the performance of proposed decoder is ISE 10.1. The comparison is made with existing encoders and it shows a remarkable improvement in the utilized frequency. The Synthesis results show a 3% improvement in the utilized no. of slice flip-flop and 49% improvement in terms of frequency. So an area efficient, cost effective Parallel Concatenated Convolutional Code Decoder has been proposed in this paper.

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