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Voltage Regulator Dc_Dc Converter Based On Filter for Low Power Analysis

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Abstract: *An active filter-based on-chip DC–DC voltage converter for application to distributed on-chip power supplies in multivoltage systems is described in this paper. No inductor or output capacitor is required in the proposed converter. The area of the voltage converter is therefore significantly less than that of a conventional low-dropout (LDO) regulator. Hence, the proposed circuit is appropriate for point-of-load voltage regulation for noise sensitive portions of an integrated circuit. The performance of the circuit has been verified with Cadence Spectre simulations and fabricated with a commercial 110 nm complimentary metal oxide semiconductor (CMOS) technology. The area of the voltage regulator is 0.015 mm2 and delivers up to 80 mA of output current. The transient response with no output capacitor ranges from 72 to 192 ns. The parameter sensitivity of the active*
filter is also described. The advantages and disadvantages of the active filter-based, conventional switching, linear, and switched capacitor voltage converters are compared. The proposed circuit is an alternative to classical LDO voltage regulators, providing a means for distributing multiple local power supplies across an integrated circuit while maintaining high current efficiency and fast response time within a small area.
Key points: *Hybrid regulator, low dropout regulator, on-chip voltage regulation, point-of-load voltage egulation.*

I. Introduction

The power supply voltage aggressively scales with each technology generation, making the delivery of a high quality supply voltage to noise sensitive circuit blocks highly challenging .The number of voltage domains within an integrated circuit is increasing to satisfy stringent power budgets. The increase in the number of voltage domains requires new techniques to generate these voltages close to the load circuitry while occupying a small area. The power savings is greater when the voltage regulators are close to the load devices (point-of-load voltage delivery), and size is therefore the primary issue for point-of-load voltage regulation. Classical power supplies occupy large on-chip area and are therefore not appropriate for point-of-load power delivery. Several topologies are commonly used to generate on-chip dc voltages. These DC–DC voltage converters are generally used as on-chip power supplies in high performance integrated circuits. Conventional DC–DC converters can be grouped into three primary categories: switching, switched capacitor (SC), and linear DC–DC converters .

Buck converters, which are step-down switching DC–DC converters, are popular because of their high power efficiency. A second order inductor–capacitor (LC) passive filter is commonly used in a buck converter. The passive LC components require significant on-chip area, therefore, the passive components have generally been implemented offchip. As a consequence of placing these components off-chip, significant voltage drop and bounce are produced at the package level due to the parasitic resistance and inductance between the off-chip components of the voltage converter and the integrated circuit. Additionally, the parasitic interconnect impedance between the discrete components of the voltage converter can produce significant power loss. Furthermore, with power supply scaling, analog and digital circuits are less tolerant to fluctuations in the supply voltage . The parasitic impedance of the interconnect between the discrete components degrades the speed and accuracy of the load regulation, causing slow response times and changing output voltage levels.

A more area efficient voltage converter structure is a lowdropout voltage regulator (LDO) . These regulators are implemented on-chip close to the load circuitry for fast and accurate load regulation. These regulators require a large output capacitance to achieve fast load regulation. This capacitor occupies significant on-chip area and is therefore generally implemented off-chip . The off-chip implementation of the output capacitor requires dedicated I/Os and produces higher parasitic losses. Alternatively, when the output capacitor is placed on-chip, the output capacitor dominates the total LDO regulator area . A high bias current of 6 mA is used in to deliver 100 mA current with a 600 pF output capacitor. This approach is not appropriate for low power applications and the output capacitor occupies a significant die area. Many techniques have been proposed to eliminate the need for the large off-chip capacitor without sacrificing the stability and performance

of an LDO regulator . Adaptively changing the bias current based on the output current demand is proposed . These techniques, however, do not completely eliminate the need for an output capacitor. Furthermore, compensation circuitry that produces a dominant pole requires additional area. Due to the large area requirement, LDO regulators are not appropriate for a system of distributed point-of-load voltage regulators.

Existing System:
Ldo Voltage Regulators

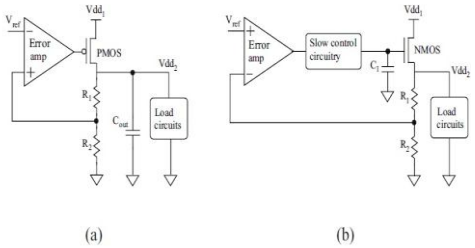


Fig.1. LDO voltage regulators with NMOS &PMOS

To produce a voltage regulator appropriate for distributed point-of-load voltage generation, the passive LC filter within a buck converter is replaced with a more area efficient active circuit . A switching input voltage is used to generate the desired output voltage, and the converter uses a filter structure to produce the desired output voltage. The current supplied to the output node, however, does not originate from the input switching signal, rather, it originates from the operational amplifier (Op Amp) output stage, similar to a linear voltage converter. The proposed voltage converter is therefore a hybrid combination of a switching and linear DC–DC converter. The on-chip area of the proposed hybrid regulator is 0.015 mm2, which is significantly smaller than state-of-the-art output capacitorless LDOs. The power efficiency, however, is limited to Vout/Vin, similar to an LDO.

II. Conventional Low Voltage Power Supplies

A linear voltage regulator utilizes a tunable resistive circuit,applying resistive voltage division to generate an output dc voltage from a higher dc voltage. The on-chip area of a linear regulator can be quite small, but the power efficiency is intrinsically low due to the resistive voltage divider. The resistive components are tuned for input voltage and output current variations to provide a stable output voltage. An LDO regulator is the most common type of linear regulator due to the LDO voltage which improves power efficiency. LDO regulators with PMOS and NMOS output stages are depicted, respectively, in Fig. 1(a) and (b). The primary advantage of linear regulators is the lower complexity and faster load regulation as compared to SC and switching voltage converters .

SC DC–DC converters utilize nonoverlapping switches to control the charge on the capacitors that transfer energy from the input to the output. When the switching frequency is sufficiently high, the output voltage is a multiple of the input voltage. The primary disadvantage of these converters is that the resistive switches dissipate high power. Additionally, thesensitivity of SC converters to changes in the output current is high and the feedback circuitry to maintain a stable dc outputvoltage is complex.

Switching DC–DC converters are the most commonly used type of power supplies due to the high power efficiency characteristics. A switching DC–DC converter generating an output voltage greater than the input supply voltage is called a boost converter. Alternatively, the converter is a buck converter if the output voltage is less than the input voltage. The passive inductor and capacitor are generally implemented off-chip due to the significant on-chip area required by these elements. The
PMOS and NMOS drive transistors generate a switching signal at Node1 . The low pass LC filter removes the high frequency harmonics of the switching signal, and generates

$$V_{dd2}(t) = V_{dd2} + V_r(t) \quad (1)$$

where Vdd2 is the output dc voltage and Vr is the output voltage ripple due to the nonideality of the low pass filter. Vdd2 is the average value of the switching voltage at Node1, which is

$$V_{dd2} = V_{dd1}(D - t_r - t_f/2T) \quad (2)$$

where D, tr , t f, and T are, respectively, the duty cycle, rise time, fall time, and period of the switching voltage . When the rise and fall times of the switching signal are the same, the output voltage is

$$V_{dd2} = DV_{dd1}. \quad (3)$$

The amplitude of the ripple voltage depends on both the filter characteristics and the variation of the output current demand. The amplitude of the ripple voltage becomes larger for a finite time when the output current demand changes abruptly. Additionally, the pulse width modulator (PWM), can be programmed to generate a different duty cycle to vary the output dc voltage.

III. Active Filter_Based Switching Dc_Dc Converter Design

In the proposed circuit, the bulky LC filter in a conventional buck converter is replaced with an active filter structure and the tapered buffers are replaced with smaller buffers, as shown The switching input signal generated at Node1 is filtered by the active filter structure, similar to a buck converter, and a dc voltage is generated at the output. Increasing the duty cycle D of the input switching signal at Node1 increases the generated dc voltage .

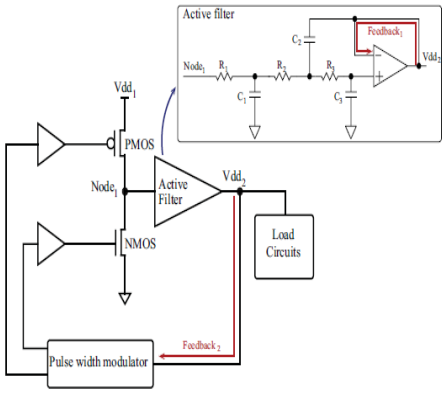


Fig. 2. DC_DC Converter

Large tapered buffers are required in a conventional buck converter to drive the large power transistors, PMOS and NMOS. The current delivered to the load circuitry is provided by these large power transistors. In the proposed circuit, however, the current delivered to the load circuitry is supplied by an Op Amp. Small buffers are therefore sufficient for driving the active filter. Replacing the tapered buffers with smaller buffers significantly decreases the power dissipated by the input stage. Alternatively, the output buffers within the Op Amp dissipate power within the regulator. Another characteristic of the regulator is that the feedback required for line and load regulation is satisfied with separate feedback paths. Feedback1 is generated by the active filter structure and provides load regulation, whereas feedback2 is optional and controls the duty cycle of the switching signal for line regulation. In most cases, feedback1 is sufficient to guarantee fast and accurate load regulation.When only one feedback path is used, the switching signal is generated by simpler circuitry (e.g., a ring oscillator) and the duty cycle of the switching signal is compensated by a local feedback circuit (a duty cycle adjustor). The primary advantage of a single feedback path is the smaller area since feedback1 is produced by the active filter and no additional circuitry is required for the compensation structure.

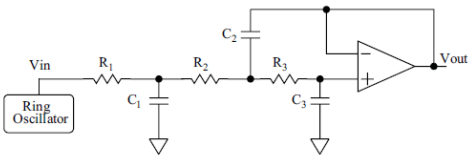


Fig. 3. Active low pass sallen_key filter

A.Active Filter Design

Active filter structures contain no passive inductors. The filtering function uses capacitors, resistors, and an active circuit (i.e., the Op Amp). Certain design considerations should be considered when utilizing an active filter as a voltage regulator since the appropriate active filter topology depends upon the application. For a voltage regulator, the on-chip area requirement, sensitivity of the active filter to component parameter variations (due to aging, temperature, and process variations), and the power dissipated by the active components should be low. Two topologies are popular for implementing an integrated low pass active filter, i.e., multiple feedback and Sallen–Key [20]. Multiple feedback low pass filters use capacitive and resistive components within the feedback path from the output to the input. A dc current path exists between the input and output nodes due to the resistive feedback. The dc current increases the power dissipated by the multiple feedback active filter. Multiple feedback active filters are therefore less suitable for an active filter-based on-

chip voltage regulator. Alternatively, Sallen–Key low pass filters use only capacitive feedback. Hence, the static power dissipation of the Sallen–Key topology is significantly less than that in the multiple feedback topology.

A third order low pass unity gain Sallen–Key filter topology. The first section, R1 and C1, forms a first order low pass RC filter. The remaining components, i.e., R2,
R3, C2, C3, and the Op Amp, form a second order Sallen–Key low pass filter. Note that no dc current path exists between the input and output. The gain of the active filter can be increased by inserting resistive feedback between the noninverting input and output nodes, forming a dc current path between the output and ground. Since low power dissipation is crucial to the proposed circuit, a unity gain topology is chosen.

The transfer function of the active filter shown
Vout/Vin= 1/ a1s3 + a2s2 + a3s + a4 (4)

where
a1 = R1R2R3C1C2C3
a2 = R1C1C3(R2 + R3) + R3C2C3(R1 + R2)
a3 = R1C1 + C3(R1 + R2 + R3)
a4 = 1

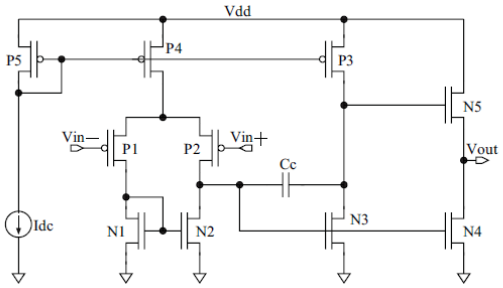
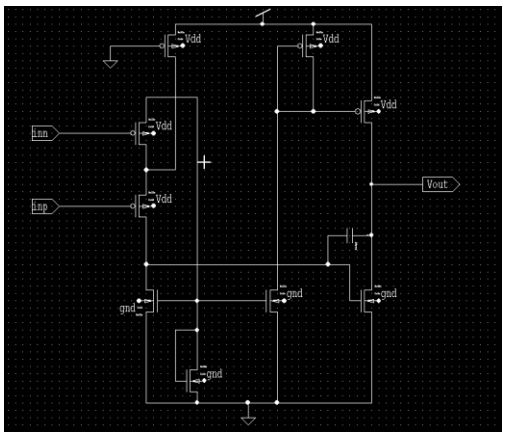


Fig.4. Three stage op amp with PMOS input transistors

B. Proposed Op Amp Design

The performance of an active filter depends strongly on the Op Amp. The gain bandwidth product of the Op Amp determines the bandwidth of the active filter. Most of the power loss takes place within the Op Amp structure, since the current provided to the output load is supplied by the Op Amp output stage. Hence, the Op Amp needs to provide tens of milliamps of current to the load devices while maintaining sufficient performance to reliably operate the active filter.

A three stage classical differential-input single-ended CMOS Op Amp structure is utilized in the proposed regulator. The size of transistors in the output stage is considerably larger than the first two stages to supply sufficient current to the load circuits. The first and second stages are gain stages which provide a cascade gain of greater than 50 dB. The third stage exhibits a gain close to unity, so the overall three stage gain is close to 50 dB with a phase margin of 51°.



IV. Conclusion

An active filter-based on-chip DC–DC power supply, appropriate for point-of-load voltage regulation, is proposed in this paper. The on-chip area for the proposed fully monolithic hybrid voltage regulator is 0.015 mm2 and provides up to 80 mA output current. The load regulation is 0.67 mV/mA, and the response time ranges from 72 to 192 ns. The area required for the proposed regulator is significantly less than that of previously proposed state-of-the-art buck converters, LDO, and SC voltage regulators despite using a mature 110 nm CMOS technology. The area of the proposed regulator will therefore be significantly smaller with more advanced technologies.

The need for an off-chip capacitor or advanced on-chip compensation techniques to satisfy stability and performance requirements is eliminated in the proposed circuit. This circuit therefore provides a means for distributing multiple power supplies close to the load to reduce P/G noise while enhancing circuit performance by delivering a high quality supply voltage to the load circuitry. With the proposed voltage regulator, onchip signal and power integrity will be significantly enhanced with the capability of distributing multiple power supplies.

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