

Analysis and Design of Low Voltage Low Noise LVDS Receiver

¹Bincy P Chacko, ²Christo Ananth M.E

¹M E Student, VLSI Design Francis Xavier Engineering College Tirunelveli, Tamil Nadu

²Assistant Professor, Dept. of ECE Francis Xavier Engineering College Tirunelveli, Tamil Nadu

Abstract: The relative advancement of technologies and availability of high frequency clocks and digital circuits, the operating frequencies of integrated circuits are increasing at a faster rate. But the rate at which different ICs communicate is not growing. So it requires an extremely high-performance solution that consumes a minimum power and is relatively immune to noise and inexpensive. Low Voltage Differential Signaling (LVDS) is a way to communicate data using a very low voltage swing (about 350mV) differentially over two PCB traces. It deals about the analysis and design of a low power, low noise and high speed comparator for a high performance Low Voltage Differential Signaling (LVDS) Receiver. The circuit of a Conventional Double Tail Latch Type Comparator is modified for the purpose of low-power and low noise operation even in small supply voltages. The circuit is simulated with 2V DC supply voltage, 350mV 500MHz sinusoidal input and 1GHz clock frequency. LVDS Receiver using comparator as its second stage is designed and simulated in Cadence Virtuoso Analog Design Environment using GPDK 180nm. By this design, the power dissipation, delay and noise can be reduced.

Index Terms: Double-tail comparator, Buffer, Differential Amplifier

I. Introduction

The past few decades have witnessed introduction of new technologies. The scaling of CMOS Technology and high level silicon integration tends to increase the on-chip data rates. But the rate at which different ICs can communicate is not growing.

Current-Mode Logic (CML) and Low-Voltage Positive-Emitter-Coupled Logic (LVPECL) are the commonly used techniques for high speed data transmission at a rate of 10Gbps. These techniques require an input signal swing of 800 mV and therefore consume more power during data transmission. Low voltage differential signaling (LVDS) is a technology-independent input-output standard used for data communications, telecommunications, etc. where high speed data transfer is necessary. LVDS is developed for low voltage, low power, low noise and high speed IO interfaces. It uses a small swing differential signal of 350mV for fast data transfer at significantly reduced power and excellent noise immunity. Differential data transmission uses two wires with opposite voltage swings to deliver the information. If common mode noise is coupled onto two wires is get rejected by the receiver which looks at only the difference between the two signals. Since the differential signal cancels the magnetic field, it radiates less noise. By using small swings power consumption is also reduced. Compared to other differential cable driving standards like RS422 and RS485, LVDS has the lowest differential swing.

An LVDS driver circuit, placed at one point, converts a digital logic signal into differential signal format. The receiver circuit placed at other point will convert this differential signal back into a single ended digital signal format. LVDS Receiver is two stage architecture with first stage being a rail-to-rail amplifier and the second stage is a cross coupled comparator. In [3] the design and the implementation of input/output (I/O) interface circuits for Gb/s-per-pin operation, compatible with low-voltage differential signaling (LVDS) standard was presented. It uses double-stage folded cascode architecture with minimum common-mode and differential input voltage. But this will support only the lower side of the rail. To support full rail input a supply voltage higher than 2.5v is required. In [4]-[5], LVDS receivers are designed which requires large supply voltage for high speed data transmission.

In this paper, an analysis of LVDS Receiver has been presented for various latch type comparators. Section I explain the operation and characteristics of Rail to Rail amplifier stage and comparator stage of LVDS Receiver. Section III discusses simulation results and followed by conclusions in Section IV.

II. Circuit Description

Low-voltage differential signaling (LVDS) technology is developed for low voltage and low power point to point communication by means of differential signaling and low voltage swing. To get a high performance LVDS receiver, a rail to rail amplifier followed by a comparator is used.

A. Rail To Rail Input Amplifier

The first stage of LVDS Receiver is a rail to rail input amplifier circuit.

The first stage maps the incoming signal to a level so that NMOS Common Drain Amplifier with a resistive load is sufficient after that circuit. NMOS Common Drain Amplifier is followed by a PMOS Differential pair, supports a high common mode voltages. In order to support low common mode voltage, a PMOS Differential pair is added in parallel. Current mirror circuit is added at the common source terminal of outer pair to stabilize current flowing through output nodes. When the inner differential pair is conducting outer pair is off and thus at any input common mode output is due to any one of the differential pair only.

Fig. 1 shows the schematic diagram of the rail to rail amplifier uses a load resistance of few kilo ohms. Transistor M10 and M6 in series with a 1KΩ resistor form a common drain amplifier. M5 and M9 transistors of PMOS differential amplifier support high common mode voltage. M3 and M4 transistors of PMOS differential amplifier support low common mode voltage. 1KΩ resistor was used as the load.

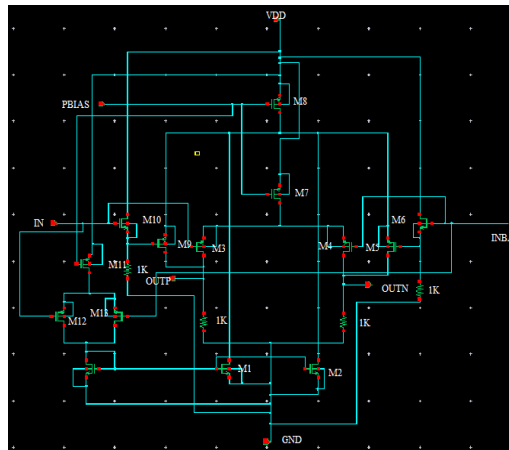


Fig. 1. Input Rail to rail amplifier used as the first stage of LVDS Receiver.

B. Comparator

Dynamic latch based comparators are used as the second stage of LVDS Receiver. These comparators can make fast decision because it uses positive feedback. In this section, analysis of dynamic latch based comparators are presented i.e., Conventional Double-Tail Latch Type Comparator and Modified Latch Type Double Tail Comparator are analyzed, based on which the proposed comparator will be presented.

Conventional Double-Tail Latch Type Comparator

A conventional double tail latch type comparator is shown in the Fig. 2. It uses two tails, one tail for input stage and other for latching stage. Since it uses two tails, stacking of transistors is avoided and therefore it can operate at low supply voltage. It allows large current flowing from the supply voltage.

The operation of conventional double-tail latch type comparator is as follows. During the reset phase when CLK=0, transistors M1 and M12 are off. Transistors M4 and M5 pulls FN and FP nodes to VDD results in output nodes discharge to ground. During decision making phase when CLK= VDD, M1 and M12 turn on and M4 and M5 turn off. This causes FN and FP node discharges towards ground.

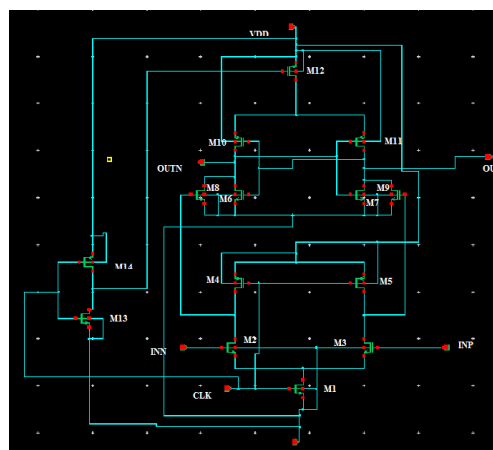


Fig. 2. Schematic diagram of the conventional double-tail latch type comparator.

It has the advantage of reduced kickback noise because transistors M8 and M9 isolate output stage of circuit from its input stage. This structure has less stacking and can operate in lower supply voltages. The disadvantage is, CLK and CLKBAR require high accuracy timing. During the decision making phase transistors M8 and M9 are off and therefore they do not play any role in improving the performance of circuit and also during the reset phase these nodes have to be charged to VDD from ground.

Modified Double-Tail Latch Type Comparator

The schematic diagram of modified double tail latch type comparator is shown in Fig. 3. To improve the latch regeneration speed in the proposed comparator two control transistors M4 and M5 are added to the conventional double tail latch type comparator in a cross coupled manner.

The operation is as follows. During reset phase when CLK= 0, M1 and M14 are off, M6 and M7 pulls nodes FN and FP to VDD and therefore M4 and M5 are off. The transistors M8 and M11 discharges both output nodes to ground. During decision making phase when CLK=VDD, M1 and M14 are on and M6 and M7 are off. Depending on input voltages INN and INP, FN and FP nodes discharges with different discharging rates. If Voltage (INP) > Voltage (INN) output node FN discharges faster than FP. Transistor M4 starts to turn on, pulling FP node to VDD, correspondingly other control transistor M5 remains off make FN to discharge completely to ground.

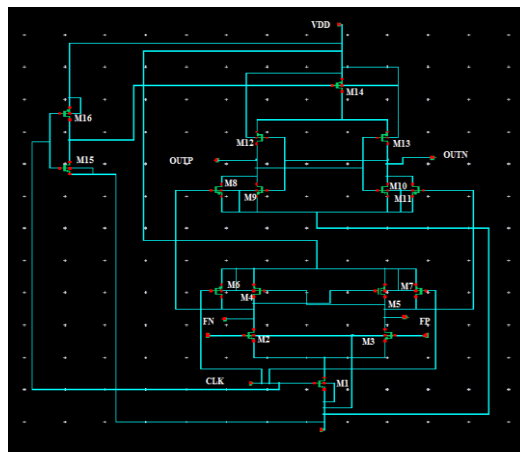


Fig. 3. Schematic diagram of Modified Double Tail Latch Type Comparator

When the control transistor M4 turns on the other node FP returns to VDD and therefore the difference between FN and FP increasing in an exponential manner, results in reduced regeneration time. This structure requires less power because one of the output nodes was not discharge completely. The disadvantage is that the circuit may susceptible to kickback noise because fastest comparators produce more kickback noise.

III. Proposed Lvds Receiver

The LVDS receivers using existing comparators that we analyzed above are subjected to environmental noise and output is getting fluctuated with clock transition. The main idea of the proposed LVDS receiver is to design a multi GBPS low noise LVDS receiver. Due to the better performance of LVDS receiver using modified double tail latch type comparator, the proposed comparator is designed based on the LVDS receiver using modified double tail latch type comparator.

C. Proposed Latch Type Comparator Circuit Description

In the circuit of LVDS Receiver using proposed latch type comparator in Fig. 4, back to back inverter in the latch stage of comparator is replaced by back to back single output differential amplifier. Differential amplifier has following advantages over back to back inverter: high immunity to environment noise and common mode noise, having better common mode rejection ratio. The main aim of the project is to minimize the noise present in the latch stage of the comparator due to the fluctuation produced at the output during clock transition.

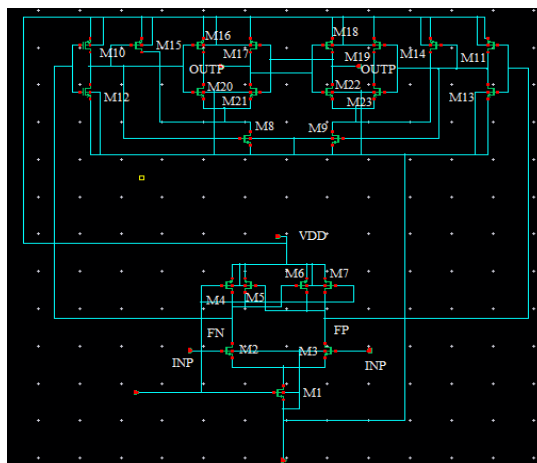


Fig. 4 Schematic diagram of Proposed Double Tail Latch Type Comparator

The operation of proposed latch type comparator is as follows. During the reset phase, when $clk = 0$, transistors M4 and M6 turn on and charge FP to VDD. The transistors M12 and M13 turn on and discharge FN node to GND. Transistors M14, M15 and PMOS transistors of differential amplifier blocks M16 and M19 turns on, NMOS transistors of differential amplifier block M21, M22 and M8, M9 turns off. Then the output nodes OUTN and OUTP charged to VDD. During decision making phase, when $clk = VDD$, the FP node discharges from VDD to GND depending on the rate of change of input voltages. At a certain voltage of FP nodes, the inverter pairs M10/M12 and M11/M13 invert the FP node signal into a regenerated signal. These regenerated signals turn PMOS transistors M15, M16, M19, and M14 off. And eventually M8, M9, M20, M23 turns on. Hence the back-to-back differential pair again regenerates the FN node signals and because of M10 and M12 being on, the positive feedback, latch stage converts the small voltage difference transmitted from FN node into a rail to rail digital level output. When the control transistor M5 turns on the other node FP returns to VDD and therefore the difference between FN and FP increasing in an exponential manner, results in reduced regeneration time. This structure requires less power because one of the output nodes was not discharge completely.

IV. Simulation Results

This section analyzes the performance of LVDS Receiver with various comparators that were discussed in the previous section. Comparison is made based on their advantages and disadvantages with respect to their speed, delay, power dissipation and noise. Cadence Virtuoso® Analog Design Environment, Virtuoso® XL Layout Editing Software is used for analyzing the circuits.

Table 1 Input Characteristics

SUPPLY VOLTAGE (VDD)	2V
TECHNOLOGY	CADENCE GPDK 180 nm
INPUT VOLTAGE	0-350mV
INPUT FREQUENCY	500MHz
CLOCK VOLTAGE RANGE	0 – 1.5V
CLOCK FREQUENCY	1GHz
CLOCK RISE TIME	100ps
CLOCK FALL TIME	100ps
CLOCK PULSE WIDTH	500ps

LVDS Receiver consists of two stages, rail to rail input amplifier stage and comparator stage. Fig. 1 shows the Circuit Diagram (designed in Cadence) of Rail to Rail Input Amplifier. The supply voltage of this comparator is 2V and sinusoidal input voltage is 350mV, 100MHz. Input Specifications are given in Table 1. Fig. 5 shows the transient response of the rail to rail amplifier circuit. A level shifted differential voltage swing is produced at the output corresponding to the input given.

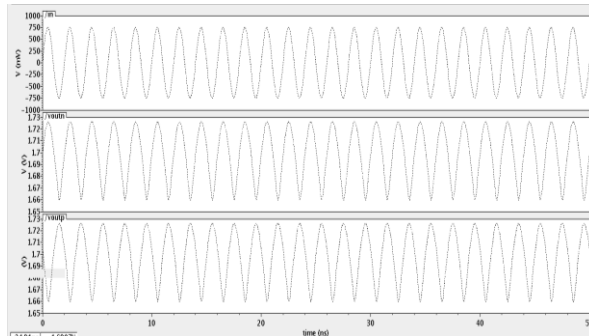


Fig. 5 Transient response of the Rail to Rail Amplifier circuit.

The comparator stage comprises of a latch circuit followed by buffer circuit (a self biased differential amplifier followed by an inverter). The circuit diagram of buffer is shown in the Fig. 6. The test setup for latch type comparator used in LVDS Receiver circuit is shown in Fig. 8 which is the same for other comparators too.

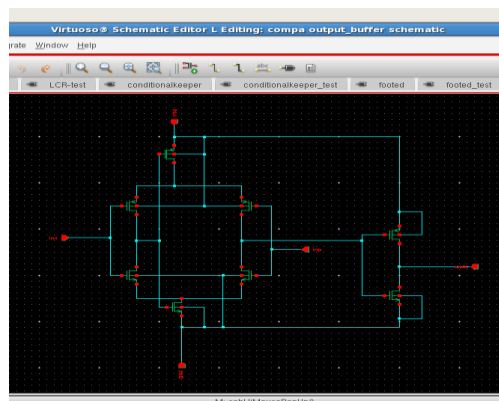


Fig. 6 Schematic Diagram of Output buffer

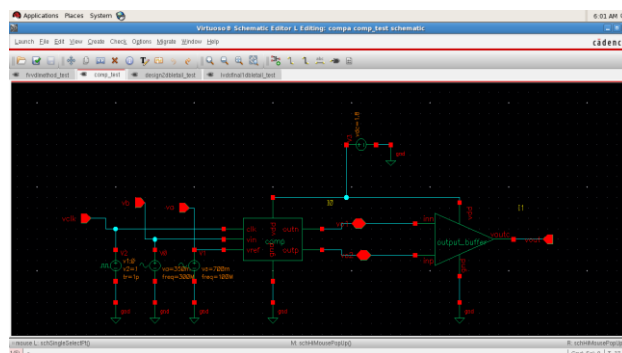


Fig. 7 Test setup for Conventional Latch Type Comparator

Fig. 2 shows the circuit diagram of conventional double tail latch type comparator and Fig. 8 shows the transient analysis of the conventional double tail latch type comparator. For the transient analysis we have taken sinusoidal voltage source as the input.

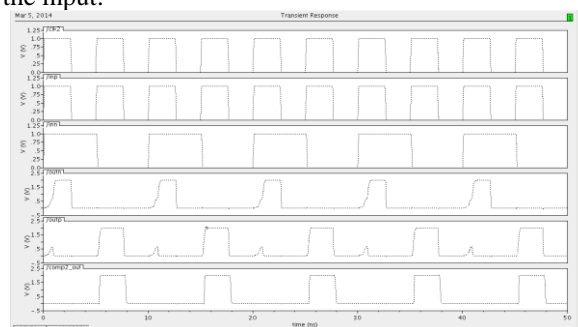


Fig. 8 Transient Response of Conventional Double Tail latch type Comparator

Fig. 3 shows the schematic diagram of modified double tail latch type comparator. Fig. 9 shows the transient analysis of the circuit. Compared to conventional double tail latch type comparator, the output node of the latch stage is less affected by delay. But its output is fluctuating with the clock. Fig. 4 shows the schematic diagram of the proposed latch type comparator and transient analysis is given in Fig.10. Transient analysis concludes that the output node in latch stage is less affected by noise and not fluctuating with the clock transition. When the common mode signal appears at the two inputs outp node at the proposed latch type comparator goes to a high value, therefore the proposed structure has high common mode rejection ratio.

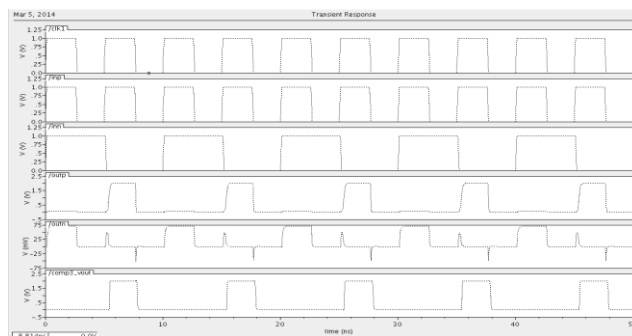


Fig. 9 Transient response of Modified Double Tail Comparator.

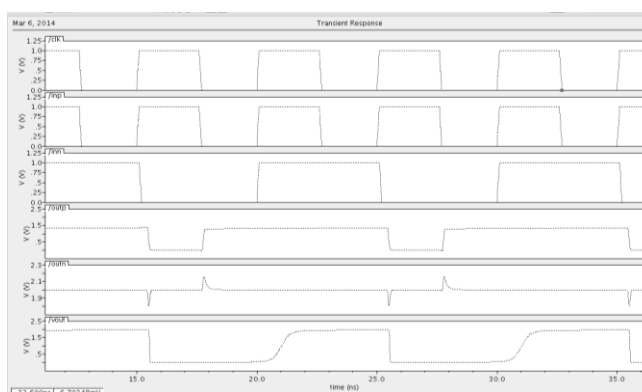


Fig. 10 Transient response of Proposed Latch Type Comparator

Then the analysis of LVDS Receiver with above said latch type comparators are presented. The test setup for LVDS Receiver using Conventional Double Tail Latch Type Comparator is shown in Fig. 11. In this circuit rail to rail input amplifier is followed by Conventional Latch Type Comparator. Fig. 12 shows the transient response of LVDS Receiver when a sinusoidal input signal of 350mV amplitude, 500 MHz is applied. Output is a digital waveform of amplitude 2V.

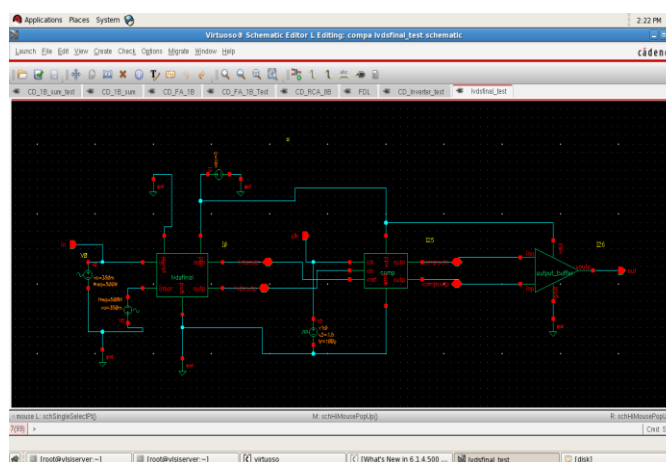


Fig. 11 Test Setup for LVDS Receiver using Conventional Latch Type Comparator

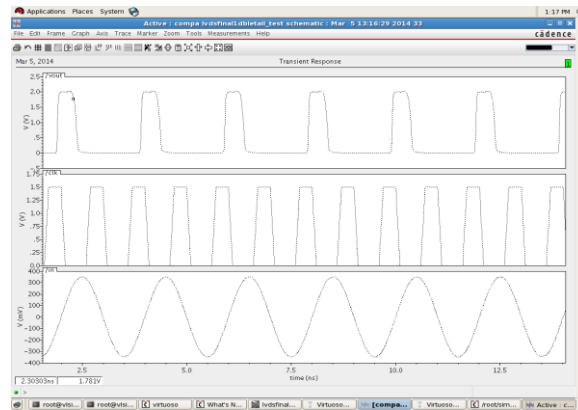


Fig. 12 Transient response for LVDS Receiver using Conventional Double Tail Latch Type Comparator

The test setup for LVDS Receiver using Modified Double Tail Latch Type Comparator is same as Fig. 11. In this circuit rail to rail input amplifier is followed by Modified Double Tail Latch Type Comparator. Fig. 13 shows the transient response of LVDS Receiver when a sinusoidal input signal of 350mV amplitude, 500 MHz is applied. Output is a digital waveform of amplitude 2V.

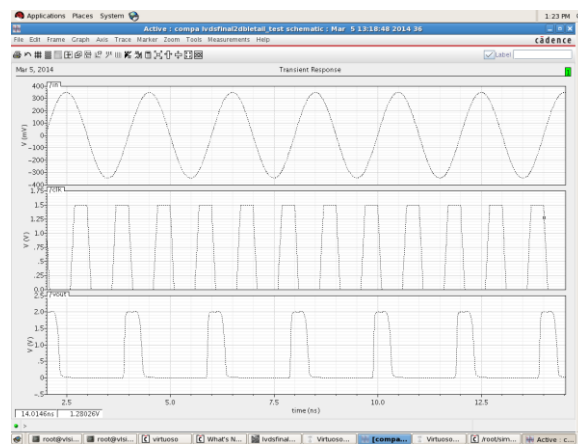


Fig. 13 Transient Response of LVDS Receiver using Modified Double Tail Latch Type Comparator

The test setup for LVDS Receiver using Proposed Latch Type Comparator is same as in Fig. 11. In this circuit rail to rail input amplifier is followed by Modified Proposed Latch Type Comparator. Fig. 14 shows the transient response of LVDS Receiver when a sinusoidal input signal of 350mV amplitude, 500 MHz is applied. Output is a digital waveform of amplitude 2V.

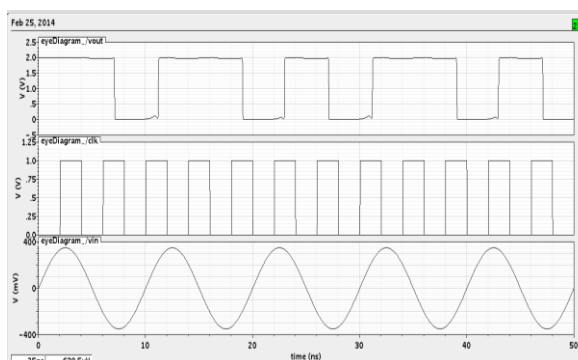


Fig. 14 Transient Response of LVDS Receiver using Proposed Latch Type Comparator

To compare the performance of the LVDS Receiver with the existing comparators, each circuit was simulated in Cadence® virtuoso analog design environment. Technology used is GPDK 180nm technology with VDD=2V as supply voltage. Table 2 shows the result summary after simulation.

Table 2 Result summary after simulation when supply voltage is 2V

PARAMETERS	LVDS RECEIVER WITH FOLLOWING COMPARATORS		
	CONVENTIONAL DOUBLE TAIL COMPARATOR	MODIFIED DOUBLE TAIL COMPARATOR	PROPOSED LATCH TYPE COMPARATOR
AVERAGE POWER(mW)	28.39	28.77	28.61
DELAY(ns)	0.864	2.856	2.504
NOISE(10^{-14} Hz)	3.8459	3.2002	.0025984
SPEED(GHz)	1.157	0.3501	0.399361

From Fig. 15 it implies that though LVDS Receiver with Proposed Latch Type Comparator has highest transistor count but it still consumes less power than LVDS Receiver with Modified Double Tail Latch Type Comparator. In Fig. 16 shows, LVDS Receiver with Proposed Latch Type Comparator has less delay compared to Modified Double Tail Latch Type Comparator but greater delay compared Conventional Double Tail Latch Type Comparator. From Fig. 17 it can say that LVDS Receiver with Modified Double Tail Latch Type Comparator has less noise compared to LVDS Receivers using other Latch Type Comparator.

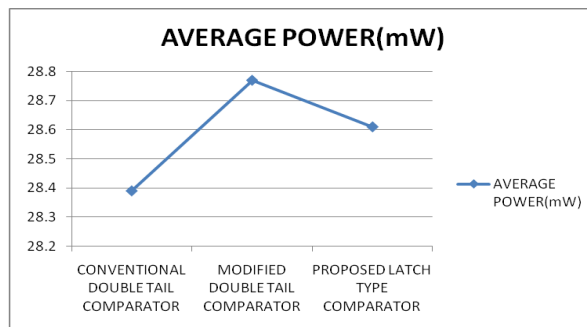


Fig. 15 Average Power Dissipation of the LVDS Receiver using above comparators

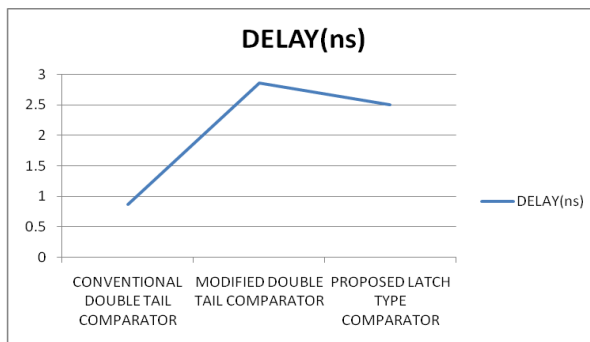


Fig. 16 Delay of the LVDS Receiver using above comparators versus supply voltage

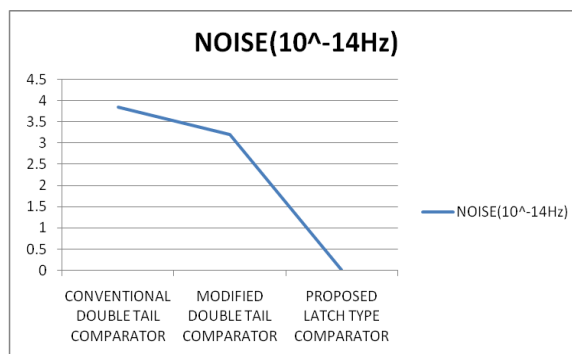


Fig. 17 Noise of the LVDS Receiver using above comparators versus supply voltage

V. Conclusion

The performances of the LVDS Receiver with the existing comparators were simulated in Cadence® virtuoso analog design environment. GPDK 180nm technology is used with VDD=2V as supply voltage. From the simulation results LVDS Receiver with Proposed Latch Type Comparator have highest transistor but it still consumes less power than LVDS Receiver with Modified Double Tail Latch Type Comparator. The speed of the Modified Double Tail Comparator is improved with respect to LVDS Receiver with Modified Double Tail Comparator. From the analyses it is concluded that LVDS Receiver with Modified Double Tail Comparator is superior than the LVDS Receiver using other comparators.

References

- [1] S. Babayan-Mashhadi and R. Lotfi, "Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator" *Int. J. very large scale integration (vlsi) systems*, Sept. 2013.
- [2] Boni, A.; Pierazzi, A.; Vecchi, D., "LVDS I/O interface for Gb/s-per-pin operation in 0.35- μ m CMOS," *Solid-State Circuits, IEEE Journal of*, vol.36, no.4, pp.706-711, Apr 2001
- [3] Boni, A.; Pierazzi, A.; Vecchi, D., "LVDS I/O interface for Gb/s-per-pin operation in 0.35- μ m CMOS," *Solid-State Circuits, IEEE Journal of*, vol.36, no.4, pp.706-711, Apr 2001
- [4] Mandal, G.; Mandal, P., "Low-power LVDS receiver for 1.3Gbps physical layer (PHY) interface," *Circuits and Systems*, 2005.
- [5] Zhao, F., Xu, Y., Li, M., Shen, C., and Tang, L. 2008. A LVDS Transceiver Chip Design in 0.5 μ m CMOS Technology. In *Proceedings of the 2008 Congress on Image and Signal Processing*, Vol. 1 - Volume 01 (May 27 - 30, 2008).
- [6] P. M. Figueiredo and J. C. Vital, "Kickback noise reduction technique for CMOS latched comparators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 7, pp. 541–545, Jul. 2006.
- [7] B. Goll and H. Zimmermann, "Low-power 600MHz comparator for 0.5 V supply voltage in 0.12 μ m CMOS," *IEEE Electron. Lett.*, vol. 43, no. 7, pp. 388–390, Mar. 2007.
- [8] B. Goll and H. Zimmermann, "A 65nm CMOS comparator with modified latch to achieve 7GHz/1.3mW at 1.2V and 700MHz/47 μ W at 0.6V," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2009
- [9] B. Goll and H. Zimmermann, "A comparator with reduced delay time in 65-nm CMOS for supply voltages down to 0.65," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 11, pp. 810–814, Nov. 2009.
- [10] T. Kobayashi, K. Nogami, T. Shirotori and Y. Fujimoto, "A current-controlled latch sense amplifier and a static power-saving input buffer for low-power architecture," *IEEE J. Solid-State Circuits*, vol. 28, pp. 523-52, April 1993.