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Distortion Analysis of Differential Amplifier

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Abstract: *The linearity of the CMOS is of major concern in the design of many analog circuits. In this paper the nonlinearity behavior of CMOS analog integrated circuits is investigated.The basic building block of analog integrated circuits such as differential amplifier with current mirror load have been chosen for harmonic distortion analysis.A mechanism to analyze the distortion of CMOS circuits in deep submicron technology that can be easily used to detect the distortion is built.The MOSFET model used for simulation is TSMC BSIM3 SPICE model from 0.13-µm CMOS process technology. HSPICE circuit simulator tool is used for distortion analysis of CMOS circuits. The MOS model used in this paper includes short-channel effects and gate-source capacitance, gate-drain capacitance, output resistance of MOS transistor. Analytical results are compared with simulation results and the influences of circuit parameters on circuit linearity are discussed.*

Keywords*: Analog Integrated Circuits, CMOSanalog integrated circuits, harmonic distortion, HSPICE, Short-channel effects, small signal analysis, transient analysis.*

I. Introduction

The rise in use of MOS devices in analog circuit design is because of its high linearity feature i.e. low distortion behaviour. But, distortion is a key measure of performance for CMOS circuits, because in saturated MOS transistors the drain current approximately depends on the square of the gate-source voltage. Therefore, circuits made up with MOS transistors or, more generally, with real active components exhibit a certain amount of nonlinearity, and this means that the relationship between their input and the output variables is not so ideally linear. Distortion is one of the most important undesired effects that appear in analog circuits due to non-linearities in the characteristics of the transistors or from the influence of the associated circuit (coupling component or load). The main goal of this project is to build a mechanism to analyze the distortion of CMOS circuits in deep submicron technology that can be easily used to detect the distortion. In analog integrating circuits, replacing the bipolar transistors with MOS transistors, the problem of relatively large values of the input bias, input offset currents and of the small value of the input impedance was solved, with the disadvantage of reducing the voltage gain caused by the quadratic characteristic of the MOS transistor working in saturation region. This fact reveals the problem of applied input voltage levels. As the technology is now shrink to nanometer range, there are some additional problems arise due to short channel effects such as body effects, channel-length modulations, signal-dependent capacitive effects and frequency-dependent distortions arising from the capacitive load in the CMOS circuits.

The first step is to select the CMOS circuits on which distortion analysis will be performed and determine the parameters responsible for distortion in the circuits. This step has been completed in literature survey process. The next step is to check the applicability of MOSFET models, which are compatible in deep submicron technology. This issue has been also solved by choosing the TSMC MOSFET models. The next step is to do correct coding of CMOS circuits by considering different parameters such as input biasing voltage, supply voltage, operating frequency range, load value, working temperature etc. and simulate the circuits on the required tools. The simulated results should be validated with theoretical one

The proposed CMOS circuit on which distortion analysis will be performed is CMOS Differential Amplifier Circuit.

The MOSFET model used for simulation is TSMC BSIM3 SPICE model from 0.13-μm CMOS process technology. HSPICE circuit simulator tool is used for distortion analysis of CMOS circuits.

II. Literature Review

As the technology is shrinking to nanometer range, different techniques have been proposed by different designers for distortion analysis of CMOS circuits and for finding linearization techniques based on the same. To minimize the distortion, a linearization technique for CMOS differential amplifiers based on the compensation of the quadratic characteristic of the MOS transistor is proposed in [1]. The non-linearity of the circuit has been evaluated by using an expansion in Taylor series of the amplifier transfer function. This technique reduces the distortion only up to 8dB. The harmonic distortion of the conventional NMOS source follower and PMOS source follower are thoroughly analyzed using a simplified large-signal model in

conjunction with Level49 BSIM3 model equations and assumptions in [2]. Based on this analysis, a new linearization technique of the cascade-complementary source follower is proposed. Comparative study of three different current mirror circuits has been done in [3]. Performance parameter including total harmonic distortion was calculated. Results are validated in 90nm CMOS technology. In [4], a high frequency low voltage low power tunable highly linear transconductor is presented. Shift level biasing is used at the inputs of both the amplifiers of a cross coupled differential pair for tuning. Bias currents of cross coupled differential amplifiers are adjusted to cancel third harmonic distortion. Author simulated the proposed circuit in Cadence VIRTUOSO with 0.18-μm CMOS process technology.

III. Theory of Amplifiers

Conventionally passive loads such resistors are used in amplifier circuits, but it have some drawback. The main drawback is to achieve large voltage gain, $I_D R_D$ product must be made large, which in turn requires a large power-supply voltage. Furthermore, large values of resistors are required when low current is used to limit the power dissipation. As a result, the required die area for the resistors can be large, which is practically very difficult to implement in nanometer technology range. To overcome this problem and provide large gain a transistor is used as load element which is also called as active load.

There are mainly three types of active load configurations used in amplifiers:

1.Complementary load or current source/sink active load,

2. Depletion load,

3. Diode connected load.

CMOS current mirror circuits are as complementary load, n-channel or p-channel depletion type transistors are used as depletion load and NMOS or PMOS transistors with gate is shorted to drain terminal is used as diode connected load. Amplifiers with current source/sink active loads tend to achieve higher gain due to the high output impedance, but at the expense of bandwidth. Amplifiers with gate-drain connected active loads tend to achieve large frequency bandwidths but low gain due to their relatively low output impedance.

IV. Cmos Differential Amplifier With Current Mirror Load

An active load acts as a current source. Thus it must be biased such that their currents add up exactly to I_{bias}. In practice this is quite difficult. Thus a feedback circuit is required to ensure this equality. This is achieved by using a current mirror circuit as load, as in Fig1.

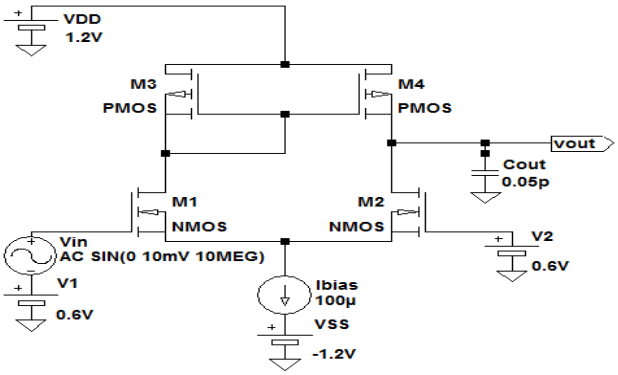

Figure 1. Schematic of Differential Amplifier with current mirror load

The current mirror consists of transistor M3 and M4. One transistor (M3) is always connected as diode and drives the other transistor (M4). Since $V_{GS3}=V_{GS4}$, if both transistors have the same β, then the current I_{D3} is mirrored to I_{D4}, i.e., $I_{D3}=I_{D4}$. The advantage of this configuration is that the differential output signal is converted to a single ended output signal with no extra components required. In this circuit, the output voltage or current is taken from the drains of M2 and M4. The operation of this circuit is as follows:

Small Signal Analysis

The small signal analysis of differential amplifier can be accomplished with the assistance of the model shown in Fig2, which is only appropriate for differential analysis when both sides of the amplifier are assumed to be perfectly matched. If this condition is satisfied, then the point where the sources of M1 and M2 are connected can be considered at AC ground. The body effect is neglected.

Output Resistance (r_{out})

The evaluation of the output resistance, r_{out}, is determined by using the small-signal equivalent circuit and applying a voltage to the output node, as seen in Fig. 2. Note that the T model was used for both M1 and M2, whereas M3 was replaced by an equivalent resistance (since it is diode-connected), and the hybrid-π model was used for M4.

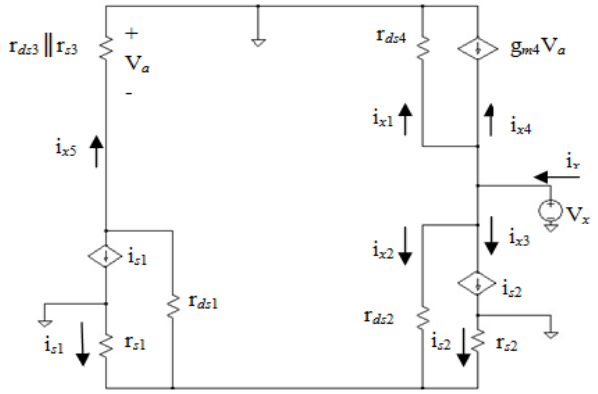

Figure 2. Small-signal model for the calculation of output resistance

As usual, r_{out} is defined as the ratio V_x/i_x, where i_x is given by the sum $i_x = i_{x1} + i_{x2} + i_{x3} + i_{x4}$. Clearly,

$$i_{x1} = \frac{V_x}{r_{ds4}} \quad (1)$$

Implying that the resistance seen in the path taken by i_{xl} is equal to r_{ds4}. Now, assuming that the effect of r_{dsl} can be ignored (since it-is much larger than r_{s1}), we see that the current i_{x2} is given by

$$i_{x2} \cong \frac{V_x}{r_{ds2} + (r_{s1} \| r_{s2})} \cong \frac{V_x}{r_{ds2}} \quad (2)$$

where the second approximation is valid, since r_{ds2} is typically much greater than $r_{s1} \| r_{s2}$. This i_{x2} current splits equally between $i_{s1}$and i_{s2} (assuming $r_{s1} = r_{s2}$ and once again ignoring r_{ds1}), resulting in

$$i_{s1} = i_{s2} = \frac{-V_x}{2r_{ds2}} \quad (3)$$

However, since the current mirror realized by M3 and M4 results in $i_{x4} = i_{x5}$ (assuming $g_{m4} = l/r_{s4} = 1/r_{s3}$ and r_{ds3} is much larger than r_{s3}), the current i_{x4} is given by

$$i_{x4} = -i_{s1} = -i_{s2} = -i_{x3} \quad (4)$$

In other words, when the current splits equally between r_{s1} and r_{s2}, the current mirror of M3 and M4 causes the two currents i_{x3} and i_{x4} to cancel each other. Finally, the output resistance, r_{out}, is given by

$$r_{out} = \frac{V_x}{i_{x1} + i_{x2} + i_{x3} + i_{x4}} = \frac{V_x}{V_x/r_{ds4} + V_x/r_{ds2}}$$

which results in the simple relationship

$$r_{out} = (r_{ds2} \parallel r_{ds4}) \quad (5)$$

Low frequency voltage gain (A_v)

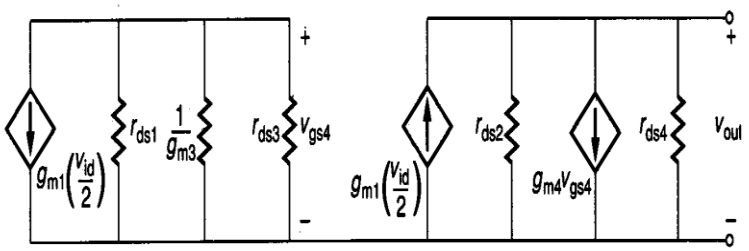

Figure 3. Small signal model of differential pair with current mirror load

Since, $v_{gs3} = v_{gs4}$

The voltage v_{gs4} can be calculated from above small signal model as

$$v_{gs4} = -g_{m1}\left(\frac{v_{id}}{2}\right)\left(\frac{1}{g_{m3}} \| r_{ds1} \| r_{ds3}\right) \quad (6)$$

Since, r_{ds1} and$r_{ds3} \gg \frac{1}{g_{m3}}$

Therefore the above equation reduces to

$$v_{gs4} = -\left(\frac{g_{m1}}{g_{m3}}\right)\left(\frac{v_{id}}{2}\right) \quad (7)$$

This voltage controls the drain current of M4 resulting in a current of $g_{m4}v_{gs4}$.

Thus the output current i_{out} will be

$$i_{out} = -g_{m4}v_{gs4} + g_{m2}\left(\frac{v_{id}}{2}\right) \quad (8)$$

Substituting for v_{gs4} from equation (7) gives

$$i_{out} = g_{m1}\left(\frac{g_{m4}}{g_{m3}}\right)\left(\frac{v_{id}}{2}\right) + g_{m2}\left(\frac{v_{id}}{2}\right) \quad (9)$$

Now, since $g_{m3} = g_{m4}$and$g_{m1} = g_{m2} = g_m$,the current i_{out} becomes

$$i_{out} = g_m v_{id} \quad (10)$$

Now the small signal output voltage is simply:

$$v_{out} = i_{out} \cdot r_{out}$$

$$v_{out} = g_m v_{id} \cdot (r_{ds2} \parallel r_{ds4}) \quad (11)$$

Therefore, the voltage gain will be

$$A_v = \frac{v_{out}}{v_{id}} = g_m \cdot (r_{ds2} \parallel r_{ds4}) \quad (12)$$

This result assumes that the output impedance is purely resistive. If there is also a capacitive load, C_L, then the gain is given by

$$A_v = \frac{v_{out}}{v_{id}} = g_m \cdot z_{out} \quad (13)$$

where $z_{out} = r_{out} \parallel 1/sC_L$.

DC Analysis-Large signal model

The differential pair in Fig. 3 is biased with a current source so that

$$I_{bias} = I_{d1} + I_{d2} \quad (14)$$

If we label the input voltages at the gates of Ml and M2 as $V_{i1}$and V_{i2}, we can write the input difference as

$$V_{di} = V_{i1} - V_{i2} = V_{gs1} - V_{gs2}$$

or in terms of the AC and DC components of the differential input voltage,V_{di},

$$V_{di} = V_{GS1} + v_{gs1} - V_{GS2} - v_{gs2} \quad (15)$$

When the gate potentials of Ml and M2 are equal, then (assuming both are operating in the saturation region)

$$I_{D1} = I_{D2} = I_{bias}/2 \quad (16)$$

Maximum and Minimum Differential Input Voltage

Since we know that a saturated MOSFET follows the relation

$$I_d = \frac{\beta_n}{2}(V_{gs} - V_{thn})^2 \quad (17)$$

The difference in the input voltages may be written as

$$V_{di} = \sqrt{\frac{2}{\beta_n}}\left(\sqrt{I_{d1}} - \sqrt{I_{d2}}\right) \quad (18)$$

The maximum difference in the input voltages, V_{dimax} (maximum differential input voltage), is found by setting $I_{d1}$to I_{bias} (Ml conducting all of the tail bias current) and $I_{d2}$to 0 (M2 off)

$$V_{dimax} < V_{i1} - V_{i2} = \sqrt{\frac{2 \cdot L \cdot I_{bias}}{k' \cdot W}} \quad (19)$$

The minimum differential input voltage, V_{dimin} , is found by setting $I_{d2}$to I_{bias} and $I_{d1}$to 0

$$V_{dimin} = -V_{dimax} = -(V_{i1} - V_{i2}) = -\sqrt{\frac{2 \cdot L \cdot I_{bias}}{k' \cdot W}} \quad (20)$$

Maximum and Minimum Differential Output Voltage

The large signal swing limitations of the output are also of interest. In this case, the swing limitations will be based on keeping both M2 and M4 in saturation.When V_{GS1} is taken above V_{GS2}, the output voltage, V_{OUT}, increases. Therefore,

$$\begin{aligned} V_{OUT(max)} &= V_{DD} - V_{SD4,sat} \\ &= V_{DD} - \left(V_{SG3} - V_{thp,4}\right) \\ &= V_{DD} - \left(\sqrt{\frac{2I_{D1}}{k' \cdot \frac{W}{L}}} + V_{thp,3}\right) + V_{thp,4} \end{aligned}$$

$$V_{OUT\,(max)} = V_{DD} - \sqrt{\frac{I_{bias}}{k'\cdot\frac{W}{L}}} \quad (21)$$

The minimum output voltage is determined by the voltage on the gate of M2 (M2 must remain in saturation).

$$V_{OUT\,(min)} = V_{I2} - V_{thn,2} \quad (22)$$

HarmonicDistortion in CMOS Differential Amplifier

Differential circuits exhibit an odd-symmetric input/output characteristics, i.e., f(-*x*) =-f(*x*). For the Taylor expansion to be an odd function, all of the even-order terms must be zero:

$$y(t) = \alpha_1 x(t) + \alpha_3 x^3(t) + \cdots \quad (23)$$

The above equation indicates that a differential circuit driven by a differential signal produces no even harmonics. This is very important property of differential operation.

The most common approach of a differential amplifier in CMOS technology is based on strong-inverted MOS transistors (usually working in the saturation region). As a result of the quadratic characteristic of a MOS transistor operating in saturation, the transfer characteristic of the classical CMOS differential amplifier will be strongly nonlinear, its linearity being in reasonable limits only for a very limited range of the

V. Result &Conclusion

The design parameters are given as follows:
Positive supply voltage = +1.2V,
Negative supply voltage = -1.2V
W/L ratio of driver transistors (M1 & M2) = 25,
W/L ratio of load transistors (M3 & M4) = 25,
Input bias voltage = 0.6V,
Input voltage signal level = 10mV,
Biasing current source = 100µA,
Load capacitance = 0.05pF,
Operating frequency = 10MHz.

1. Transient Analysis:

The transient analysis of CMOS differential amplifier with current mirror load shows that output voltage signal is in same phase and amplified version of input voltage signal.

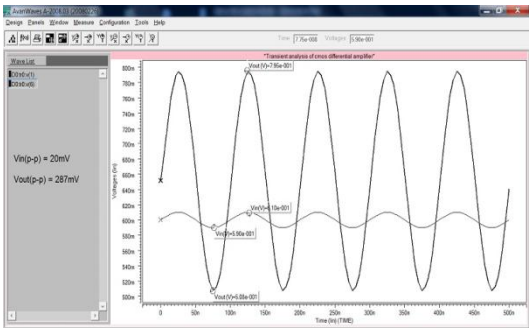

Figure 4. Transient response waveform of CMOS differential amplifier with current mirror load

2. FFT Analysis:

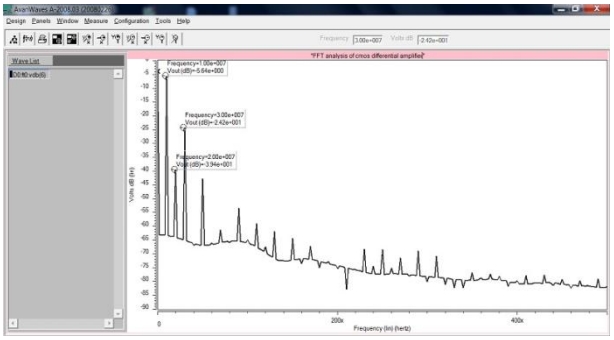

Figure 5. Output voltage (dB) vs. Frequency (MHz) curve of CMOS differential amplifier

This analysis shows the value of output voltage signal at fundamental frequency and its harmonics at the multiple of fundamental frequency. The waveform of FFT analysis shows that the value of 3rd harmonic is greater than the 2nd harmonic, which means 3rd harmonic is dominated in CMOS differential amplifier. The 3rd harmonic term is mainly responsible for distortion in CMOS differential amplifier.

3. AC Analysis:

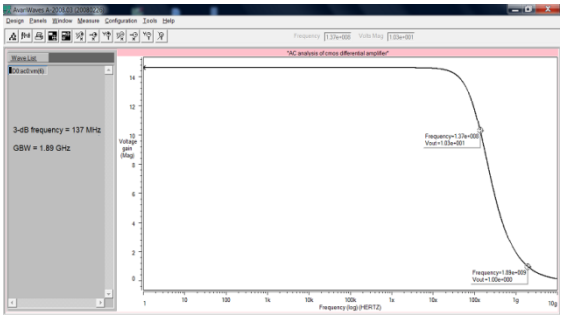

Figure 6. Voltage gain vs. Frequency waveform of CMOS differential amplifier

Table 1. Summary of results obtained from AC analysis

S.No.	Parameters	Calculated	Simulated
1.	Small Signal Voltage Gain	14.73 or 23.36 dB	14.61 or 23.29 dB
2.	3-dB Cut-off Frequency	143.47 MHz	137 MHz
3.	Unity Gain Frequency (GBW)	2.11 GHz	1.89 GHz

4. Harmonic Distortion Analysis:

Table 2. Total harmonic distortion vs. Peak to peak input voltage signal level

S.NO.	Peak to peak input voltage signal level (mV)	THD(dB) Calculated	THD(dB) Simulated
1.	10	-56.38	-45.31
2.	20	-44.34	-44.26
3.	30	-37.30	-43.87
4.	40	-32.30	-37.85
5.	50	-28.42	-33.15
6.	60	-25.25	-28.33
7.	70	-22.58	-24.66
8.	80	-20.26	-21.98
9.	90	-18.21	-19.95
10.	100	-16.38	-18.40

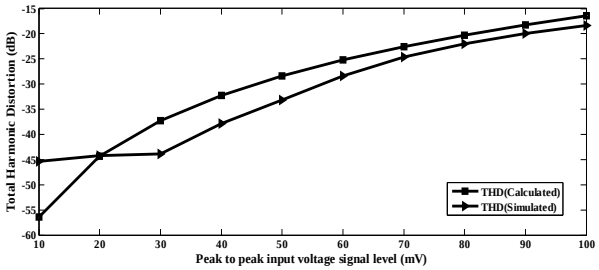

Figure 7.Total harmonic distortion vs. Peak to peak input voltage signal level

The allowable input voltage signal level for CMOS Differential Amplifier using above design parameters is 20mV (Calculated) and 30mV (Simulated) for which THD is below the 1%.

Table 3. Simulated Results for Total harmonic distortion vs. Frequency

S.NO.	FREQUENCY (MHz)	Total Harmonic Distortion (dB)
1.	0.1	-51.9094
2.	0.5	-51.8886
3.	1	-51.806
4.	2	-51.4863
5.	3	-51.0261
6.	4	-50.4915
7.	5	-49.9296
8.	6	-49.3693
9.	7	-48.8277

10.	8	-48.312
11.	9	-47.8264
12.	10	-47.3711
13.	20	-44.1371
14.	30	-42.2842
15.	40	-41.0659
16.	50	-40.1891
17.	60	-39.5234
18.	70	-38.9815
19.	80	-38.5403
20.	90	-38.1673
21.	100	-37.8456

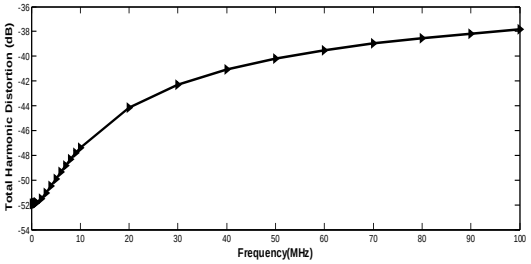

Figure 8. Total harmonic distortion vs. Frequency graph of CMOS differential amplifier

The frequency range for which Total Harmonic Distortion is below the 1% is 50MHz for CMOS Differential Amplifier designed using above parameters.

VI. Future Scope

This project is mainly concentrated on harmonic distortion analysis. So, future work should be put into investigating the effect of inter-modulation and phase distortion.The downscaling of transistor sizes to submicron regions continues and modifies the square-law I-V characteristic of MOS devices. Short channel effects, such as body-effect, channel length modulation, velocitysaturation and mobility reduction, arise and change the square-law relation to a morelinear characteristic.This will affect the nonlinear behavior of analog integrated circuits. In this project, body-effect is considered on hand calculation of the measurement of distortion. Thus it is recommended that another short channel effects should be include in measurement so that a more clear picture of distortion analysis should be develop and the difference between calculated results and simulated results will be minimized.The more complicated analog circuits such as operational amplifier, analog to digital converter, mixers and low noise amplifier should be choose for distortion analysis. The presented circuit topology was implemented in a 130nm CMOS process. It is also of great interest to investigate the nonlinear behavior in different processtechnologies, such as 90nm, 45nm and even belowCMOS process, silicon-germanium BiCMOS process,gallium-arsenide or a process using silicon-on-insulator technology.

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