

All optical single module phase encoded half-adder and half-subtractor exploiting four wave mixing in semiconductor optical amplifier

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Abstract: The development of all optical super fast arithmetic logic unit (ALU) is one of the most important requirement for construction of super fast all optical processor. All optical half-adder and half-subtractor have performed most of the essential functions of the arithmetic logic unit. Here in this paper the author has proposed a scheme of single module for phase encoded simultaneous operation of half-addition and half-subtraction for the same input bits using four wave mixing (FWM) in semiconductor optical amplifier (SOA). This type of single module for simultaneous operations using phase encoding based on the difference of phase with the reference signal one through FWM in SOA will gives fast response to accomplish the demand of super fast all optical processing.

Keywords - ALU, FWM, SOA, half-adder and half-subtractor.

I. INTRODUCTION

To counter everyday increasing challenges of super fast signal processing, optics comes with novel interest with strong potentiality over electronics in last few decades [1]-[3]. The introduction of non-linear properties of semiconductor enhances the prospect for the development of all optical processor in a very suitable and attractive manner. Optical processing has required diverse arithmetic logic operation ability for implementing the different types of computation. Half-adder and half-subtractor performs a very important role in this operation to achieve this demand. Several types of encoding procedures have been already proposed and demonstrated for the realization of all optical binary half-adder and half-subtractor by various groups of scientists using different optical non-linear properties of the material [3]-[7]. Phase encoding technique drew more attention in last few years as it shows higher receiver sensitivity and extended tolerance limit in long-haul fiber transmission systems [8]-[9]. Thus phase encoding in optical computing gives higher spectral efficiency. Four wave mixing (FWM) in SOA requires a very short scattering time because it is an intra-band process. Therefore to accomplish high speed of processing it will be better to choose FWM in SOA with phase encoding procedure. In this communication the author has proposed a new scheme for the realization of all optical phase encoded binary input/output format based simultaneous half-adder and half-subtractor using FWM in SOA. So this type of unit can perform the binary addition and subtraction at the same time for the same inputs with very high speed.

II. PROCEDURE OF ENCODING

In this phase encoding procedure a signal can be called a '0' bit if it has no phase difference with respect to a reference signal whereas a signal can be called '1' bit if it ensures a ' π ' phase change with respect to the same reference signal. Due to stability in periodicity of phases in this encoding scheme, at the output the phase difference value 2π and $-\pi$ are equivalent to 0 and π phase difference respectively. Here this type of input bit is produced by placing the π phase modulator over the reference light beam and the output also can be detected through interferometric actions.

III. SIMULTANEOUS OPERATION OF HALF-ADDER AND HALF-SUBTRACTOR

The half-adder and half-subtractor both is combinational logic unit which performs a simple addition and subtraction of two binary digits respectively. In this combined single logic unit has three outputs, one of them have given SUM and DIFFERENCE both and the other two give CARRY and BORROW of the addition and subtraction of the two binary digits. The output of the unit SUM and DIFFERENCE represents the least significant bits of the two bits as a result of binary addition and subtraction process respectively and the CARRY and BORROW outputs corresponds to the carry and borrow of the binary summation and the subtraction respectively. The SUM and DIFFERENCE of the binary addition and subtraction are represented by the following same Boolean functions given by

$$\text{SUM} = S = \overline{A}\overline{B} + \overline{A}B + A\overline{B} + AB = A \oplus B, \text{ DIFFERENCE} = D = \overline{A}\overline{B} + \overline{A}B = A \oplus B$$

and the CARRY and BORROW of the binary addition and subtraction method are given by

$$\text{CARRY} = C = A \cdot B \quad \text{and} \quad \text{BORROW} = \beta = \bar{A} \cdot B.$$

The logic of the SUM and DIFFERENCE functions of the binary half-adder and half-subtractor have directly bear a resemblance to the same logic of XOR and the CARRY and BORROW both also correspondence to the AND gate but in case of borrow output before AND logic operation the first input must be inverted by NOT gate and it is given by the arrangement shown in the fig-1.

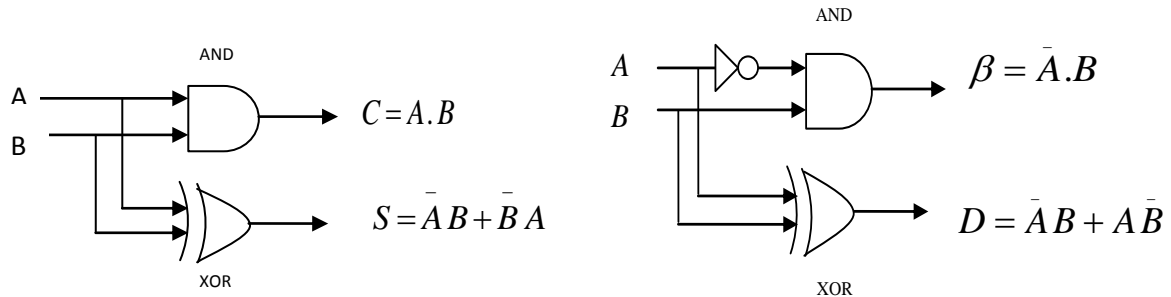


Fig-1:- Construction of Half adder and subtractor by the logic gates.

All optical phase encoded one XOR and two AND logic gates are required to implement this combined single unit of all optical half-adder and half-subtractor shown in the fig-2. In this single unit only three logic gates are necessary instead of four for the simultaneous operation of binary addition and subtraction of the same binary inputs.

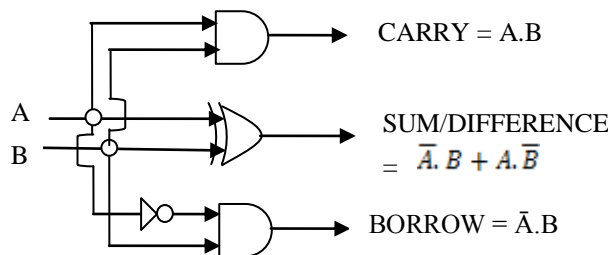


Fig-2:- Development of single module of half-adder and half- subtractor.

IV. PRINCIPLE OF FWM IN SOA

The Four Wave Mixing is a nonlinear intra-band process in a semiconductor optical amplifier. The phenomena of FWM occurs inside SOA when more than one light waves with different frequency inserted into it and as a result of FWM in SOA it will produce many idler signal light waves of different amplitudes, frequencies and phases based on the third order non linearity of it [10]-[14]. In case of FWM in SOA, if the three waves interact with one another, then two of them act as a pump waves and the other as probe generates different idler components with the unmodified inputs also are given by

$$E_{FWM} = E_1 E_2 E_3 \eta(i, j) \text{Cos}[(\kappa_1 \pm \kappa_2 \pm \kappa_3)x - (\omega_1 \pm \omega_2 \pm \omega_3) + (\phi_1 \pm \phi_2 \pm \phi_3)]$$

where E_i , K_i , ω_i and ϕ_i represents the amplitudes, wave vectors, frequencies and phases of the three input light waves ($i=1,2,3$).After FWM in SOA the different idler components come out with different frequencies $\omega_{FWM} = \omega_1 \pm \omega_2 \pm \omega_3$ and phases $\phi_{FWM} = \phi_1 \pm \phi_2 \pm \phi_3$.

But when two beam incident over SOA instead of three, then the input signal also act as pump waves. This is known as self pumped FWM and its output has the form given by,

$$E_{4,3(FWM)} = \kappa E_{1,2} E_{2,1}^2 \text{Cos}[(2\kappa_{2,1} - \kappa_{1,2})x - (2\omega_{2,1} - \omega_{1,2}) + (2\phi_{2,1} - \phi_{1,2})],$$

The two idler components of these FWM outputs with phases $\phi_{FWM} = \phi_1 + \phi_2 - \phi_3$ and $2\phi_1 - \phi_2$ in the two cases have used here for implementing the XOR and AND logic gates for the construction of half-adder and half-subtractor. We have already proposed and demonstrated this concept for implementing the different logic gates using phase encoded binary inputs/outputs [15]-[17].

V. PROPOSED SCHEME OF COMBINED SINGLE MODULE HALF- ADDER AND HALF- SUBTRACTOR

In this arrangement of single unit half-adder and half-subtractor shown in the fig-3, phase modulator1 and 2 are used to generate the phase inputs A (ϕ_1) and B (ϕ_2) by placing the phase modulators over two pump beams with frequency ω_1 and ω_2 and the third probe beam with frequency ω_3 is always maintain the same phase with the reference, i.e. $\phi_3 = 0$.

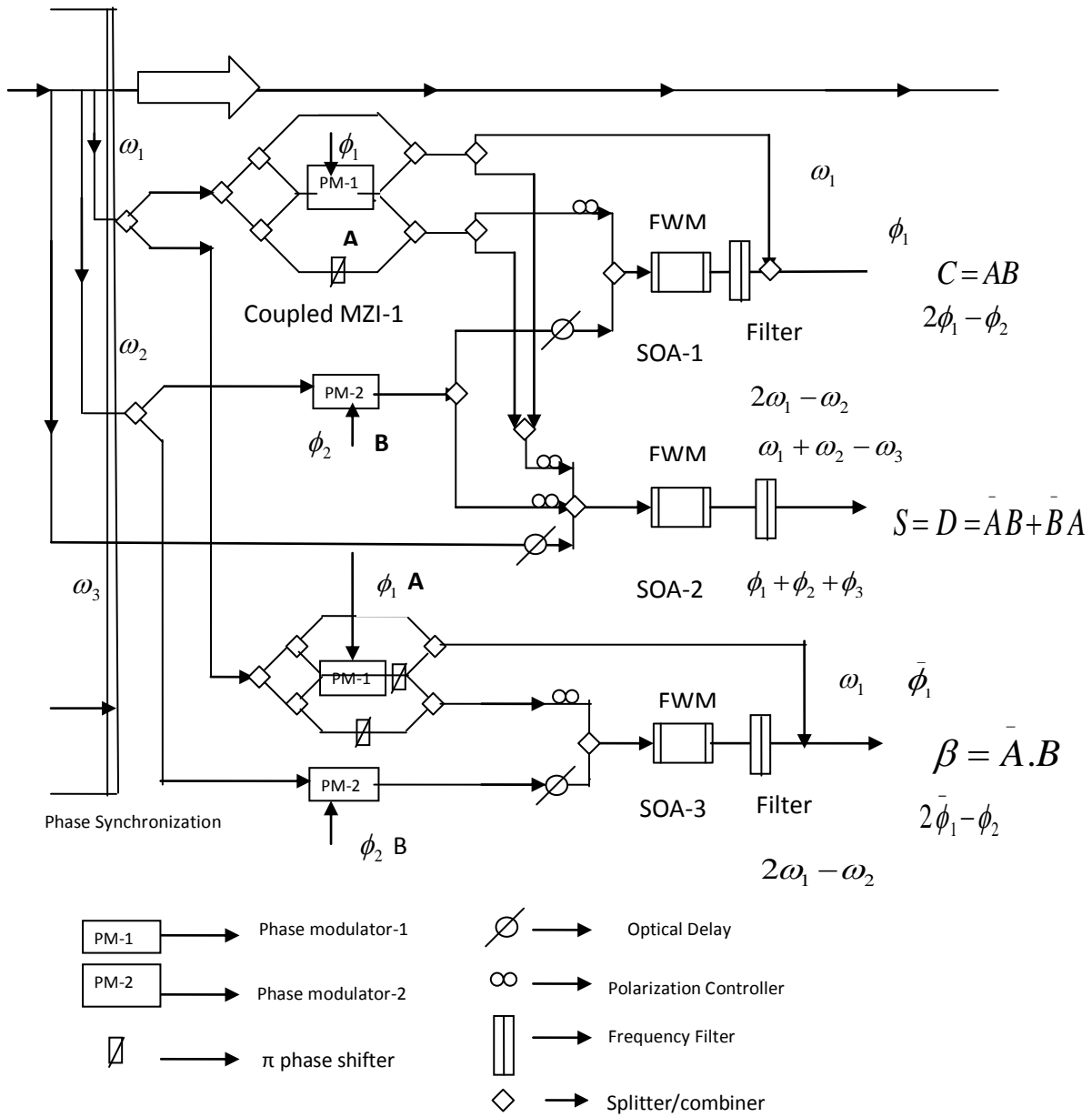


Fig-3:-Schematic diagram of proposed all optical phase encoded Half-adder

In this scheme of half-adder and half-subtractor in a single unit shown in the fig-3, basically after demultiplexing from the reference wave stream into three waves with frequency ω_1 , ω_2 and ω_3 , the light wave with frequency ω_1 is split equally into two beams and these two equally intense streams entered into the coupled MZI for proper operation through interferometric action at the outputs of the coupler. The preferred phase of the input signal is produced by inserting a phase modulator over the stream path. The input A of

preferred initial phase ϕ_1 is placed simultaneously in the common arm of coupled MZI using phase modulator-1 (PM-1) and the other input **B** of initial phase ϕ_2 is also placed over the stream with frequency ω_2 at a proper position by phase modulator-2 (PM-2). The phase modulators will create a relative phase difference π or 0 according to the data given for operation. For proper action a π phase shifter is inserted in the lower arm of the coupled MZI. Both the outputs of the combiner of coupled MZI after interference is divided first and then combine the one split stream from each output to supply the one pump beam with frequency ω_1 for FWM in SOA. In this scheme three SOA are required for the simultaneous addition and subtraction of the same phase encoded bits in a single module. The XOR logic realization is required for both the SUM and DIFFERENCE outputs of binary addition and subtraction respectively. The three stream of waves of three different frequencies ω_1, ω_2 and ω_3 with phases ϕ_1, ϕ_2 and ϕ_3 respectively entered inside SOA-2 for four wave mixing. The FWM idler component with phase $\phi_{FWM} = \phi_1 + \phi_2 - \phi_3$ is employed for the realization of XOR logic in case of phase encoded bits. This concept of XOR logic realization based on phase encoded inputs has already reported. A band pass filter centered at frequency $\omega_1 + \omega_2 - \omega_3$ is used to take out only the light wave with phase $\phi_{FWM} = \phi_1 + \phi_2 - \phi_3$ after FWM in SOA-2. To execute the CARRY and BORROW outputs two optical AND gates are necessary. The self pumped FWM in SOA is employed in this purpose for the realization of AND logic of phase encoded bits. The one of the idler component of the self pumped FWM with phase $2\phi_1 - \phi_2$ and the stream appear with phase ϕ_1 at the output in the absence of FWM are exploited for the realization of AND logic. We have already proposed this concept of AND logic operation using phase encoded bits. The interferometric action of this coupled MZI-1 and the self pump FWM in SOA-1 are applied in the purpose of operation to find out CARRY output between the phase encoded bits incase of binary addition. In this scheme another coupled MZI and SOA-3 for FWM is utilized in case of find out the BORROW output of binary subtraction between the phase encoded bits. The phase modulators are now placed over the same proper position over the stream ω_1, ω_2 to generate the preferred phase encoded bits. But with the same arrangement an extra π phase shifter is inserted in the middle arm of the lower coupled MZI just after the P.M-1 to invert the phase of the inputs instantaneously. Therefore the idler with phase $2\bar{\phi}_1 - \phi_2$ after FWM and the wave appears with phase $\bar{\phi}_1$ in the absence of FWM are used for the BORROW output in case of binary subtraction. The truth table of this simultaneous binary addition and subtraction is shown in the table-1.

For efficient FWM the three or two wave streams must be co-polarized using polarization controllers before entering the SOA. Phase adjustment will be required for the three waves of frequency ω_1, ω_2 and ω_3 after de-multiplexed from the reference stream. To get the successful operation the inputs phase encoded information must be reached properly at the inputs of the SOA for FWM. For this restriction the optical attenuator and the tunable optical delay must be included in the appropriate position over the single mode fiber. Both the P.M-1s and P.M-2s for the CARRY and BORROW output are synchronized properly according to the given data bits.

TABLE-1:- TRUTH TABLE OF HALF-ADDER AND HALF-SUBTRACTOR

Phase of input (A) ϕ_1	Phase of input (B) ϕ_2	Phase of output (S) and (D) $\phi_{out} = \phi_1 + \phi_2 - \phi_3$	Phase of output (C) $\phi_{out} = \phi_1 = 0$ when $\phi_1 = 0$ instead of any value of ϕ_2 and $\phi_{out} = 2\pi - \phi_2$ when $\phi_1 = \pi$	Phase of output (β) $\phi_{out} = \bar{\phi}_1 = 0$ when $\phi_1 = \pi$ instead of any value of ϕ_2 and $\phi_{out} = 2\pi - \phi_2$ when $\phi_1 = 0$
0(0)	0(0)	0(0)	0(0)	0(2 π)
0(0)	1(π)	1(π)	0(0)	1(π)
1(π)	0(0)	1(π)	0(2 π)	0(0)
1(π)	1(π)	0(2 π)	1(π)	0(0)

VI. CONCLUSION

In this proposed design the operation of binary addition and subtraction for the same inputs are executed simultaneously. Here in this scheme of the half adder and subtractor in a single module is required less active and passive components both and as a result of it will needed smaller area in the photonic integrated circuits. Thus it should be operates in a very fast mode due to both lesser components and area. Phase encoding inputs with the swift action of FWM in SOA makes the operation in a rapid way which is the requirement of super fast all optical processor.

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