*IOSR Journal of Electronics and Communication Engineering (IOSR-JECE)*
*e-ISSN: 2278-2834,p- ISSN: 2278-8735.Volume 6, Issue 2 (May. - Jun. 2013), PP 51-55*
*www.iosrjournals.org*

# Design of Adjustable Reconfigurable Wireless Single Core

Marianne M. Kamal
*Renewable Energy Department, Arab Organization for Industrialization, Egypt*

***Abstract :*** *In wireless communication system transmitted signals are subjected to multiple reflections, diffractions and attenuation caused by obstacles such as buildings and hills, etc. At the receiver end, multiple copies of the transmitted signal are received that arrive at clearly distinguishable time instants and are faded by signal cancellation. Rake receiver is a technique to combine these so called multi-paths [2] by utilizing multiple correlation receivers allocated to those delay positions on which the significant energy arrives which achieves a significant improvement in the SNR of the output signal. This paper shows how the rake, including dispreading and descrambling could be replaced by a receiver that can be implemented on a CORDIC based hardware architecture. The performance in conjunction with the computational requirements of the receiver is widely adjustable which is significantly better than that of the conventional rake receiver.*

***Keywords -*** *Rake receiver, Multi-paths, CORDIC*

## I. INTRODUCTION

WCDMA offers variable spreading factor and multiple codes per user to enable features like high data rates and multiple services for the same connections. To do so rake receiver architecture for W-CDMA should be configurable such that the hardware is utilized optimally at varying requirements.

One of the main features of W-CDMA is bandwidth on demand (BOD) which means that it offers variable user data rates. This is achieved by adopting variable spreading factors and multi-code connections for a user. More information bits are transmitted if a lower spreading factor is used for the same chip rate and parallel channels are offered by having multiple codes per user. So the receiver should be adjustable meaning to adjust the receiver performance in a wide range depending on the channel impulse response [4].

The receiver computes the symbols (representing the users) by an array of CORDIC processors; CORDIC (Coordinate Rotation DIgital Computer) is one of the efficient hardware algorithms for hardware signal processing [3]. When the processing power needed exceeds that of the soft core processor, co-processor elements can be added. It is possible to use the processor array for other tasks (in addition to symbol computation) due to its design as a coprocessor element.

The implementation on FPGA has the advantage of reconfigurable computing. A lot of modern signal processing applications require such a high computational power that only ASIC's can fulfill the technical demands. ASIC's are inflexible, costly (development and debugging) and only economical for mass productions. Due to the fact that even the most commonly used programmable devices (DSP) often lack the required processing power, one tries to develop a solution that lays somewhere in between the two extremes; a programmable processing and dedicated hardware, the effort in this area is summarized under the term reconfigurable computing.

## II. CORDIC RAKE RECEIVER

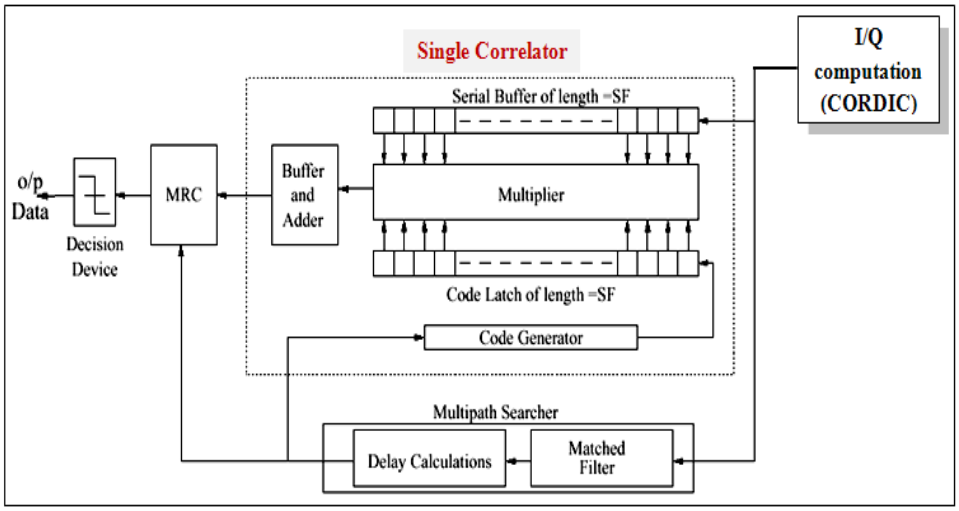
### 2.1 CORDIC Algorithm

A set of shift-add algorithms collectively known as CORDIC for computing a wide range of functions including trigonometric, hyperbolic, linear and logarithmic functions [3]. Since the last two decades, the application of CORDIC arithmetic for efficient implementation of signal processing algorithms continues to receive wide attention because of its numerical stability, efficiency in evaluating trigonometric and hyperbolic functions, hardware compactness and inherent pipelinability at the micro-level.

Compared to other approaches, CORDIC is a clear winner when a hardware multiplier is unavailable, e.g. in a microcontroller, or when you want to save the gates required to implement one, e.g. in an FPGA. On the other hand, when a hardware multiplier is available, e.g. in a DSP microprocessor, table-lookup methods and good old-fashioned power series are generally faster than CORDIC. The CORDIC algorithm is used to compute the sine and cosine values which are required to calculate the In-phase and Quadrature phase components of the received signals of the RAKE receiver [3].

## 2.2 Architecture

In the proposed single correlator Fig.1, the spreading sequence is latched in a fixed register to eliminate the need of multiple code generators running continuously as in conventional RAKE receiver [1]. A serial shift buffer of length equal to that of sequence is used to hold the received chips. As a new chip is received the buffer shifts and drops the oldest chip to accommodate the newest chip in the buffer. Multipath searcher detects the multipath in the channel and provides the same to the code generator and maximal ratio combiner. Each chip of the serial shift buffer is connected through a multiplier with the corresponding chip of the code latch. These multipliers multiply the corresponding chips in the serial shift buffer and fixed register whenever multipath are detected by the multipath searcher. Each multiplier output is buffered in its dedicated buffers and they are integrated by the adder.




Maximal-Ratio Combining is the optimal form of diversity combining because it yields the maximum achievable SNR. Multipath searcher passes the multipath information to the MRC. Maximal ratio combiner (MRC) collects all the integration results of a sequence and its multipath to combine them for a bit decision. For the Maximum Ratio Combining RAKE receiver, a simple alpha tracker is used since it requires a short time window to form an estimate.

The RAKE receiver uses several baseband correlators to individually process several signal multipath components. The In-phase (I) and Quadrature (Q) samples r(i) to each correlator are given by:

$$r(i)_I = \sum_{k=0}^{K-1} a_k(i)\, s(i-k) \cos(\theta_k(i)) \tag{1}$$

$$r(i)_Q = \sum_{k=0}^{K-1} a_k(i)\, s(i-k) \sin(\theta_k(i)) \tag{2}$$

where $a_k$ is the amplitude of the $k^{th}$ multipath signal
$\theta_k$ is the phase of the $k^{th}$ multipath signal
s is the transmitted spread spectrum signal

The spread-spectrum receiver then correlates these baseband signals with the PN code sequence used in the transmitter. This gives the post correlation signal x(i) given by:

$$x(i)_I = \sum_{m=0}^{M-1} r(i+m)_I C_m \tag{3}$$

$$x(i)_Q = \sum_{m=0}^{M-1} r(i+m)_Q C_m \tag{4}$$

The correlator outputs are combined to achieve improved communications reliability and performance. In a RAKE receiver, if the output from one correlator is corrupted by fading, the others may not be, and the corrupted signal may be discounted through the weighting process. Impulse response measurements of the multipath channel profile are executed through a matched filter to make a successful despreading (IIR filter). The alpha tracker can be thought of as IIR low pass filter. The difference equation describing the alpha tracker is:

$$Y(n) = (1-\alpha) \,.\, X(n-1) + \alpha \,.\, y(n-1) \tag{5}$$

Impulse response measurements of the multipath channel profile are executed through a matched filter to make a successful dispreading.

The **I** & Q components of the channel impulse response are given by

$$h_k(n)_I = (1-\alpha)\cdot d_{n-1}\cdot x_k(n-1)_I + \alpha \cdot h_k(n-1)_I \tag{6}$$

$$h_k(n)_Q = (1-\alpha)\cdot d_{n-1}\cdot x_k(n-1)_Q + \alpha \cdot h_k(n-1)_Q \tag{7}$$

Where Xk(n) is the kth post correlation received sample for bit n. The real and imaginary parts of the RAKE output, y(n), are given by the complex multiplication of the post correlation signal with the complex conjugate of the channel estimate signal, at each of the K multipath delays.

$$y(n)_I = \sum_{k=0}^{K-1}\left[h_k(n)_I \cdot x_k(n)_I + h_k(n)_Q \cdot x_k(n)_Q\right] \tag{8}$$

$$y(n)_Q = \sum_{k=0}^{K-1}\left[h_k(n)_Q \cdot x_k(n)_I - h_k(n)_I \cdot x_k(n)_Q\right] \tag{9}$$

The data decision is then made using (5)

$$d_n = \operatorname{sgn}\left\{y(n)_I\right\} \tag{10}$$

### 2.3 Implementation

The algorithm can be implemented using Altera Nios II board. FPGA uses SRAM cells to store configuration data. The NIOS II system built using SOPC builder tool [5].

#### 2.3.1 Software implementation

The CORDIC algorithm is used to compute the sine and cosine values which are required to calculate the In-phase and Quadrature phase components of the received signals of the RAKE receiver. The CORDIC algorithm is developed as a custom instruction to the NIOS processor.

NIOS II processor custom instructions are custom logic blocks adjacent to the ALU in the CPU data path. With custom instructions we can reduce a complex sequence of standard instructions to a single instruction implemented in hardware. The custom instruction logic connects directly to the NIOS II processor ALU.

#### 2.3.2 Hardware implementation

IIR filter can be implemented as hardware component since parallel processing is required for fast computing the filter output. IIR filter for channel impulse response estimation. Alpha tracker for maximum ratio combiner as shown in Fig. 2.

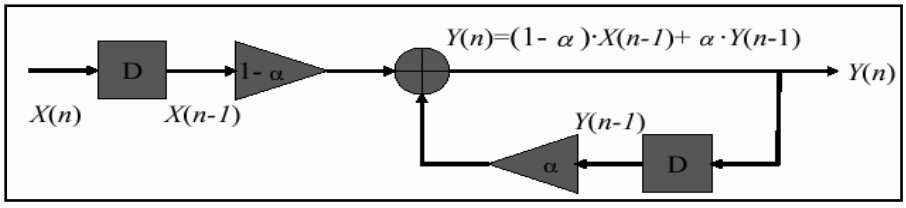



Figure2: Alpha tracker

#### 2.3.3 Implementation steps for the CDMA RAKE receiver

i. Compute the (I) and (Q) components of inputs to each RAKE finger. For each chip symbol:
a. Compute the sine and cosine values of the delay spread angle.
b. Calculate the In-phase component by multiplying the transmitted spread spectrum signal with the calculated cosine value.
c. Calculate the Quadrature phase component by multiplying the transmitted spread spectrum signal with the calculated sine value.
ii. Calculate the Post correlation signal, for each bit:
a. De-spread the signal obtained from step i by multiplying it with the spreading sequence.

b. Integrate all the chips (number equal to spreading factor) into a single bit.
iii. Estimate the (I) and (Q) components of channel impulse response.
a. Use an IIR filter of order equal to the number of fingers.
b. The impulse response of the channel is given by the transfer function of the filter.
iv. Calculate the real and imaginary parts of the RAKE output
a. At each of the K multipath delays, perform complex multiplication of the post correlation signal with the complex conjugate of the channel estimate signal.
b. Separate real and imaginary parts of the above multiplied result to get real and imaginary parts of the RAKE output.
v. The RAKE output is given to a decision device to obtain the received bits. The decision device is a simple Signum function which takes the real part of the RAKE output as input and gives the output bits.

## III. RESULTS

In the 3G Standard the Chip rate = 64 chip / bit, Spreading factor = 16, I/Q data word size = 8 bits and the clock = 15.36 MHZ. Digitized input samples are received from RF front end and converted to the form of complex I & Q branches. The computation is done by using CORDIC algorithm, Fig.3, with I & Q word size is 8 bits. The serial buffer of length equals to the spreading factor in the UTMS standard spreading factor (SF) = 16. The code latch is also a serial buffer of length equals to 16. The code generator is implemented using linear feedback shift register (LFSR). This block consists of 16 D-type Flip Flop and XOR gate

For the matched filter is the Cross correlation of the received signal with pilot bits (16 zero bits), the impulse response of the matched filter- implemented as raised cosine filter- is shown Fig. 4. The bit error rate was found to be 0.0018 and the received signal before and after filtering is shown in Fig. 5.

The alpha tracker filter was implemented as a low pass butterworth filter of first order, pass-band equals to 1.2 MHz. The coefficients are: a[0] = 1, a[1] = 1, b[0] =1 and b[1] = -1.

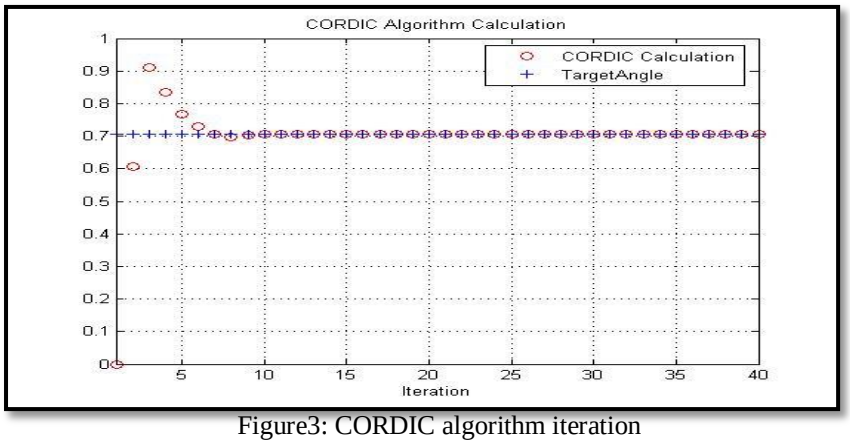
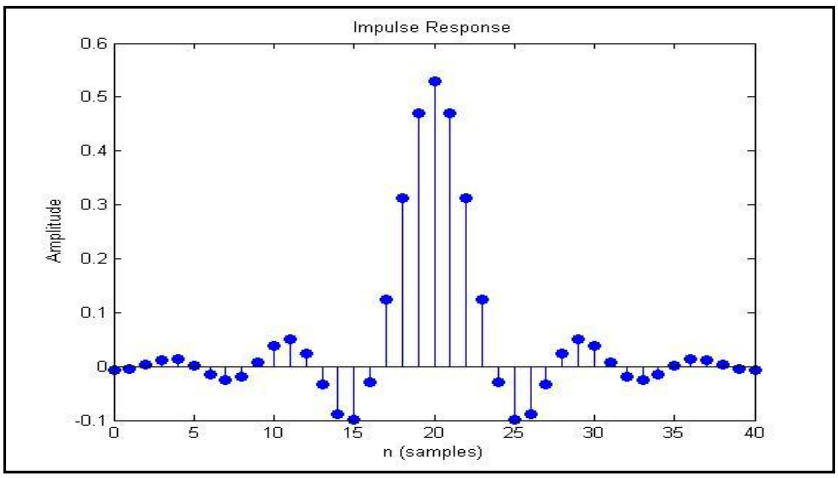



Figure3: CORDIC algorithm iteration



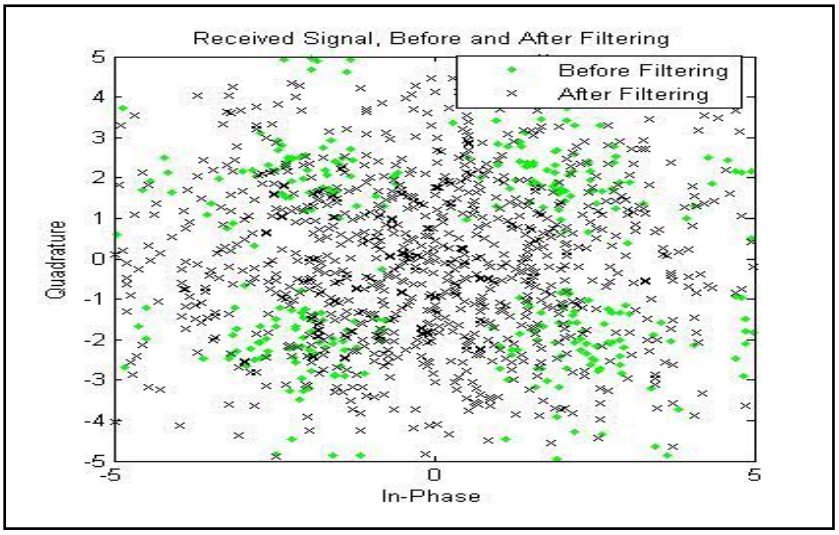



Figure 5: Received signal

## IV. CONCLUSION

W-CDMA has emerged as the most widely adopted 3G air interface. W-CDMA offers variable spreading factor and multiple codes per user to enable features like high data rates and multiple services for the same connection. To enable W-CDMA features, architectures for rake receiver should be configurable for varying data rate requirement at a particular time and should support processing of multiple codes. It should consume less power in order to be suitable for downlink purpose. The conventional rake receiver architecture provides dedicated hardware for each multipath per code. Such a rigid architecture is not suitable for varying requirements (of number of codes and multi-paths) in W-CDMA [2].

A single correlator RAKE receiver with MWH codes as the spreading codes has been introduced. The presented single correlator RAKE receiver gives considerable better operation in comparison with the conventional RAKE receiver in terms of circuit complexity, power consumption and BER performance.

## REFERENCES

[1] M. Uzzafer, "Single Correlator Receiver for Wideband MultiPath Channel," in Proc. IEEE 6th CAS Symp., Shanghai, vol. 2, June 2004, pp. 421-424.
[2] R. Price and P. E. Green, "A Communication Technique for Multipath Channels," Proc. IRE, vol. 27, pp. 555-570, Mar. 1958.
[3] Ray Andraka, "A survey of CORDIC algorithms for FPGA based computers", ACM 0-89791- 978-5/98/01, 1998.
[4] Tero Ojanperä, Ramjee Prasad, "Wideband CDMA for Third Generation Mobile Communications", Norwood MA, USA, Artect House Inc., 1998, 439 pp.
[5] "Introduction to the Altera SOPC Builder", Altera Corporation, San Jose C.A., 2006.