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FPGA Based System Login Security Lock Design Using Finite State Machine

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Abstract : *Field Programmable Gate Array (FPGA) delivers breakout performance capacity and system integration while optimizing to develop FPGA devices based on CAD tools in the Hardware Description Language (HDL), which illustrate the logic, function and behaviors of system hardware. VHDL (very high speed integrated circuit HDL) is one of the important hardware description language which is used in this research paper to design SYSTEM LOGIN SECURITY LOCK. This research paper introduces the security technology for machines or objects. In this we design an automatic Security System Login Lock using FSM based on FPGA. This can be done with the help of XILINX software. In this the lock can only opened when the desired code (password) is entered or the given sequence is detected by the system.*
Keywords - *FPGA, SYSTEM SECURITY, FSM, VHDL, XILINX CAD*

I. INTRODUCTION

In this paper we implement a system security lock because at present time security system to be one of the most important technologies in this global world [1]. Security refers to technique for ensuring that data stored in a computer cannot be read or used by anyone without authorization. A system cannot have high assurance if it has poor security and requirements. For high assurance, systems will logically include security requirement as well as availability, reliability and robustness requirements [2]. When the information and material /object are seem to be much more important than system has to be mightily strong to protect it against hackers/thief or others. Due to the proper security controls in the system we are able to either prevent or minimize the negative impact of the hackers attack and due to this it increases the reliability, gaining trust and satisfaction of the people [1].

Security has become an increasingly growing concern at the internet age [3] and Nowadays, mobile phones are used for multiple purposes like internet-access, e-mails, calendar, mobile banking and so on. This results in a large amount of personal information stored on these devices such as addresses, appointments and business details in addition to phone numbers [4].All the Electronic business processes connect many systems and applications, to cope with the growing complexity of the electronic business processes, the application of security models are used [5]. Security needs of a system depend highly on the environment in which the system is deployed [6].

Security methods for these devices are typically one of three forms.

1. A password or code.
2. A key or token.
3. A biometric user authentication system.

These security measures are intended to protect the device against unauthorized access [7].

Security system has various implementation methods like- Automatic gesture recognition systems using computer vision techniques [8], using persona concept: it is intended to support end-user, enterprises privacy and authentication in a wireless /wire line networked environment [9].

1.1 Field Programmable Gate Array (FPGA)

In this paper, we develop the FPGA based system to implement the safety in many applications like defense, medical and social life etc [10]. A FPGA programmable gate array (FPGA) is an integrated circuit. Its configurations are generally specified using a hardware description language (HDLS) such as VHDL [10]. Many current models of FPGAs not only support traditional hardware design, but also have the ability to run many types of software [11]. FPGAs today come with high speed interfaces and serial communication protocols. These are more capable technically, they allow user to develop complex products and designs that were not possible before. FPGA are frequently used to implement system interfaces and glue logic. It can integrate large amounts of random logic, simple data paths and can be easily reprogrammed to reflect changes in system components [12]. The reprogrammable devices like field programmable gate arrays are highly alterative options for hardware implementations of algorithms. The FPGA may reconfigure at irregular intervals or upon interrupt, when configuration is reloaded into the FPGA, its state must be restored so it can resume operation as if it had never been removed [13].

FPGA–accelerated software applications are a growing demand in fields ranging from communications and image processing to biomedical and scientific computing. It can describe some of the main features of the approach including hierarchical, decomposition, multi-level timing specifications and flexible con currency and synchronization capabilities [14].

1.2 Finite State Machine

Finite state machines have been one of the main formalisms underlying the prevailing approaches to hardware description and synthesis [14]. The design of a FSM might be the ultimate objective of particular efforts more often; a FSM is described as a component used to perform control functions in a large system to synthesize a FSM description that uses enumerated states, each states name must be replaced with a unique binary code.

A Finite State Machine is also a mathematical model of computation used to designing both computer programs and sequential logic circuits. A Finite State Machine is one that has a limit or finite number of possible states. It can be used both as a development tool for approaching and solving problems. We can model finite state machine with state flow and integrate them into a Simulink model.

Simulink is a block diagram environment for multi domain simulation and model based design. It supports system level design, simulation, automatic code generation and continuous test and verification of systems.

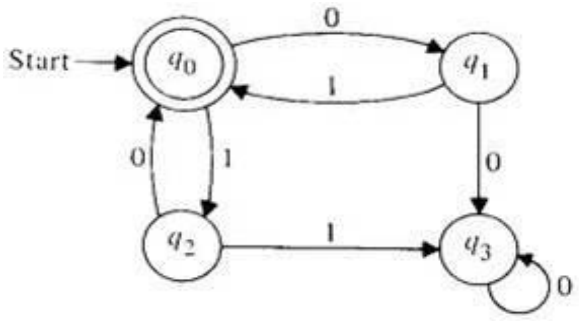

Fig.1 Finite State Machine

It is a model of a computational system, consisting of a set status and a transition function that maps each state to another state for any given input symbol.

It's Easy to use graphical languages Powerful algorithms for synthesis and verification but number of states can be unmanageable and numerical computation cannot be specified capacity. A finite state machine contains a finite number of states and produces outputs on state transitions after receiving inputs [15].

II. OVERVIEW OF STATE MACHINE

State machine are an integral part of software programming .It make code more efficient, easier to debug and help organize the program flow. State machines of sequential circuit can be classified as: Moore machine Outputs are a function of current state. The Outputs changes synchronously with states changes and Mealy machine Outputs depends on state and inputs.

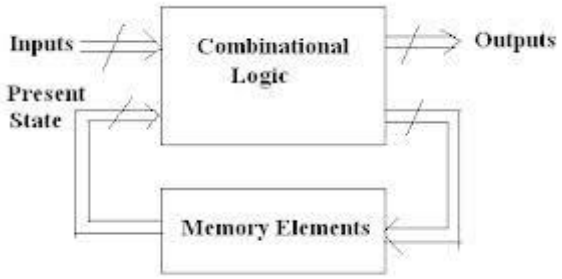

Fig2. Mealy Machine

In Figure2 the output depends on current input and state. In Mealy machine a deterministic finite state transducer for each state and input, at most one transition is possible. A Mealy machine can be converted to a Moore machine by adding states. In this output are unstable unit, current input achieve steady state. Mealy machine required less hardware than Moore circuit and inputs can affect outputs in current clock period.

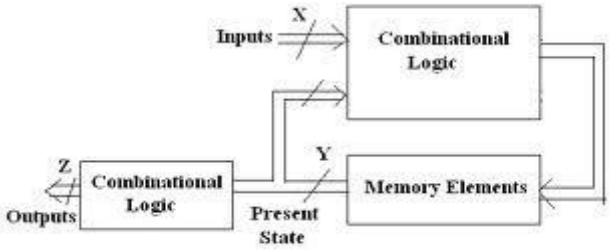

Fig.3 Moore Machine

In Figure3 the output depends only on current state. In this the current outputs are affected by the current state only and output are always stable, but it requires more hardware than Mealy circuits and the input can affect outputs in next clock period only. Sequential system has memory so output depends on the present and the previous inputs.

The Mealy model is usually more compact than the Moore model. Indeed the transformation from mealy to Moore involves a state splitting procedure that may significantly increases the number of states and state transition [16].

Two types of sequential system are: Synchronous Sequential System: Its behavior depends on the inputs and outputs at discrete instants of time. In this the memory holds a systems state. These changes occur in state at specific times like a periodic signal times or clocks changes the state. E.G.: State changes occur at rising edge of the clock. Asynchronous Sequential System: Its behavior depends on inputs at any instant of time.

2.1 State Diagram

A state diagram allows the conceptualization of the FSMs operation to be separated from its implementation. It represents a finite state machine (FSM) which contains circles; circles are used to represent the states of FSM which are labeled with a binary encoded number. Directed Arcs represents the transitions between states and labeled with input/output for that state transition. FSM can only be in one state at a time and the state transitions are followed only on clock cycles (for synchronous only).

2.2 Xilinx State Cad Tool

Xilinx is the leading innovator of complete programmable logic solutions including advanced integrated circuits, software design tools. State CAD has been designed for digital design, documentation and error analysis. State CAD include state bench (test bench generation and behavioral verification), the HDL Browser. After validating a diagram, state CAD automatically generates simulation and synthesizable HDL code directly from the diagram. The HDL is valid, consistent, maintainable and accurately implements the graphical diagram. State CAD enhances productivity, reduces product development cost and accelerates time to market. State bench is used to view the result waveforms and finally generated HDL file is downloaded on the FPGA board for verification of the design.

III. PRACTICAL IMPLEMENTATION OF STATE MACHINE

The FPGA based FSM design flow for the security system lock is as follows. The logic of the system is developed in the form of state diagram with the help of Xilinx state CAD tool. An FSM can be represented by a state transition diagram, a directed graph whose vertices correspond to the states of the machine and whose edges correspond to the state transitions [15]. FPGA based system give fast response and also show the low power consumption [17].

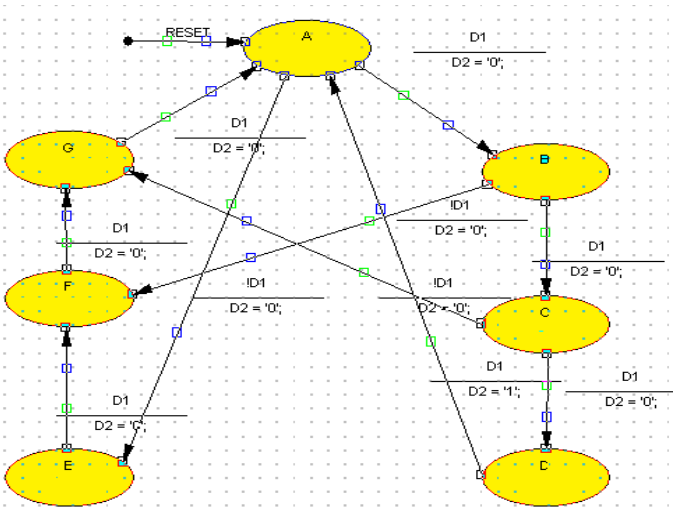

Fig.4 State Diagram for Lock

There are multiple numbers of security systems are available to protect our computer/resources. Among them, password based systems are the most commonly used system due to its simplicity, applicability and cost effectiveness [18]. In this figure the following states are used. The basic principle of the this lock is that it open only when it detect the given sequence .eg-111100001101010101011

The state diagram in figure4 is simulated using Xilinx ISE simulator.

IV. SIMULATION RESULTS

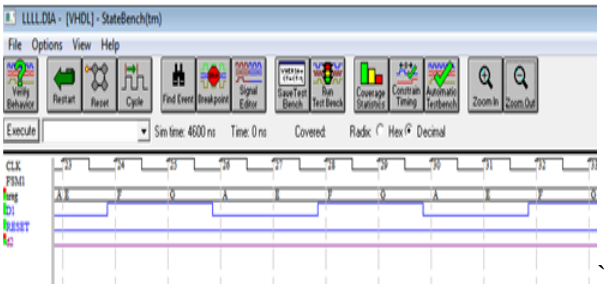

Fig.5 Output Waveform

Figure5 represent the simulation waveform for the given code sequence and these simulation waveforms shows that when the sequence is matched then output becomes one and only then the lock can open and if it does not then it remain locked.

V. IMPLEMENTATION ON FPGA

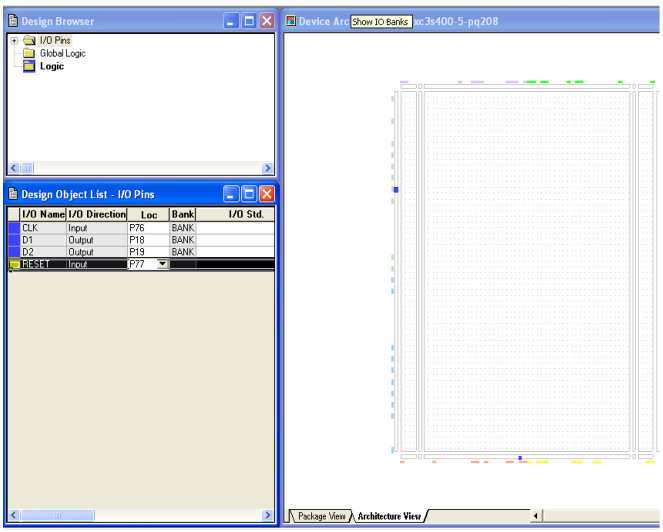

Fig.6 Pin Configuration on FPGA

Figure6 shows that pin no.76 and pin no.77 are used as input pins of FPGA and pin no.18 and pin no.19 are used as output pins of FPGA.

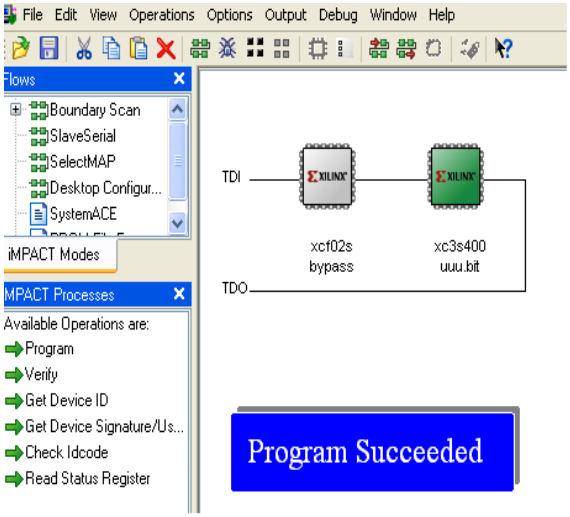

Fig.7 After Loading

Figure7 shows the loading of the program on FPGA. The JTAG cable must be connected to parallel part of pc and it configure using slave serial mode and power supply to the main board must be on position [19].

Fig.8 Result

Figure8. Shows the output, D2 is glowing. The Design, Simulation, Verification and Implementation of system login security Based on FPGA have been demonstrated and completed successfully [20].

VI. CONCLUSION

Security is the art of restricting admittance to certain entities and is a huge concern for our global society. So in this paper we present the FPGA based system security lock using with the help of Xilinx ISE design 14.4.The design is verified or tested on the FPGA SPARTAN3 Board [21]. This design has been used in numerous applications like in Military, Medical Equipments, Home security system, Car security etc. Due to this security System we can protected our system or documents. The next stage of this study is to convert this model into hardware and used for useful purposes.

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