*IOSR Journal of Electronics and Communication Engineering (IOSR-JECE)*
*e-ISSN: 2278-2834,p- ISSN: 2278-8735. Volume 5, Issue 3 (Mar. - Apr. 2013), PP 07-14*
*www.iosrjournals.org*

# FPGA Implementation of MB-OFDM Using Biorthogonal Encoder

[1]Palaniappan.T [2]Veluchamy.S
[1] *Electronics and Communication Engineering, PG Scholar, Anna University Chennai, Regional centre, Madurai*
[2] *Electronics and Communication Engineering, Faculty, Anna University Chennai, Regional centre, Madurai*

***Abstract****: UWB is a high data rate, short range technology .It transmits the information over a minimum bandwidth of 500 MHZ. Modern UWB systems use Modulation techniques such as OFDM (Orthogonal Frequency Division Multiplexing). The MB-OFDM proposal is selected for UWB system model. Multiband OFDM (MB-OFDM) is a short-range wireless technology that permits data transfers at very high rates, between 53.3 and 480 Mbps. For the requirement of Multiband-OFDM system, the processor should work on a few hundred MHz, which makes it difficult to implement. And since the system targets for the wireless portable devices, small area and low power consumption are also imperative. Therefore a 8-way parallel architecture based on bi-orthogonal encoder is proposed in this paper. In order to satisfy the performance requirement, the proposed architecture reduces the power consumption and utilizes more bandwidth and also detects and corrects both random and burst errors. It is used for multiuser transmission scheme and also works at high speed. The detailed analysis shows that the proposed technique could reduce the gate count by 32.47% on average. With 0.18-µm CMOS process, clock rate of the entire baseband modem was about 66 MHz and BER was 5.57e-138.*

***Index terms-*** *multi-band orthogonal frequency division multiplexing (MB-OFDM), parallel architecture, ultra wide band (UWB), resource optimization.*

## I. Introduction

The design of an MB-OFDM ultra-wideband receiver is challenging when we target power consumption minimization while providing enough robustness against the nearby wireless interference. **U**ltrawideband (UWB) communication technology is emerging as a leading standard for high-data-rate applications over wireless networks. Due to its use of a high-frequency bandwidth, UWB can achieve very high data rates over the wireless connections of multiple devices at a low transmission power level close to the noise floor. Since the power level allowed for UWB transmissions is considerably low, UWB devices will not cause significantly harmful interference to other communication standards. The IEEE 802.15.3a has established a High Rate Alternative Physical Layer (PHY) Task Group (TG3a) for Wireless Personal Area Networks (WPAN) to standardize the development of UWB devices. Different proposals for the PHY are under consideration. The orthogonal frequency-division multiplexing (OFDM)-based physical layer is one of the most promising options for the PHY due to its capability to capture multipath energy and eliminate intersymbol interference

There are two competing UWB radios under consideration: the direct-sequence impulse radio and the Multi-Band Orthogonal Frequency Division Multiplexing (MB-OFDM) radio. One of the promising ultra-wide band (UWB) technologies is multi-band orthogonal frequency division multiplexing (MB-OFDM) which has been proposed for the IEEE 802.15.3a. OFDM is a relatively mature technology and has been adopted in digital broadcasting, wireless LAN standards. OFDM has several advantages such as low complexity equalization in dispersive channels and the spectral scalability/adaptability. In OFDM system, single high rate dataflow is divided into the several low rate flows. Every flow is then mapped to the orthogonal frequencies using the inverse fast Fourier transform (IFFT). MB-OFDM is a multi-band technology, using orthogonal frequency division multiplexing. The total bandwidth that could be occupied, as defined by FCC, is from 3.1 GHz to 10.6 GHz. This covers a total span of 7.5 GHz. MB-OFDM divides the available spectrum into 14 bands of 528 MHz In the each subband, orthogonal frequency division multiplexing (OFDM) is applied. The transmitted symbols are time interleaved across the subbands to utilize the spectral diversity to improve the transmission reliability. Such high frequency is problematic and it consumes too much power and very difficult to implement. Therefore parallel architectures has been proposed to reduce the power consumption as well as to reduce the timing constraints [2],[3].The parallel architecture can run at reduced voltages and consequently consume less power[4]. Narrower sub-band bandwidth also relaxes the requirement on sampling rates of ADCs consequently enhancing digital processing capability.

This paper presents a resource efficient (gate count reduction) implementation techniques for the highly parallel MB-OFDM baseband system with low power consumption. Here a 8-way parallel architecture which uses 8 times lower clock frequency for saving power consumption has been proposed. The previous literature showed that resource optimization was obtained by the use of convolutional encoder with code rate 1/3and constraint length 7.Convolutional encoder produces $2^n$ output for n-input. The proposed novel architecture makes use of biorthogonal encoder instead of convolutional encoder. But biorthogonal encoder produces $2^{n-1}$ output for n+1 input. Also bandwidth utilization is high for biorthogonal encoder compared to convolutional encoder. This encoder reduces both random errors and burst of errors. So interleaver and puncturer is not required in the proposed architecture whereas convolutional encoder makes use of puncturer and interleaver.

The puncturer omits some of coded bits in order to support different code rates with one convolutional encoder. Puncturing is a procedure for omitting some of the encoded bits at the transmitter and inserting dummy "zeros" into the decoder at the receiver, in place of the omitted bits. It is used to utilize the bandwidth effectively in convolution encoder. Compared to convolutional encoder, biorthogonal encoder produces $2^{n-1}$ output from n+1 input. So puncturer is not required in biorthogonal encoder. The coded bit stream is interleaved in order to provide robustness against burst errors. Since biorthogonal encoder removed both types of errors, it does not make use of interleaver. Thus resource efficient implementation is obtained by reducing the number of gates in the proposed architecture.

For the resource efficient implementation, the following novel optimization techniques was designed: 1) in a packet synchronizer, a small amount of shared pre-computation among multiple data paths allows the data paths to eliminate about a half of their computations without significant input-multiplexing costs that offset the benefit of the adder elimination, thus reduces resource usage like [5]; 2) in a carrier frequency offset compensator which involves inter-tracking compensation, algorithm reconstruction enables sharing a single set of complex multipliers for both offset tracking and compensation without increasing the processing latency and buffer memory. In addition, it is described how to efficiently design several other components: in an equalizer, eliminating pre-computation of equalization coefficients reduces computational resource and buffer storage costs. By detailed analysis it can be shown that the gate count could be reduced by 32.47%.

The rest of the paper is organized as follows: section II provides an overview of the design and section III gives detailed description of the resource optimization technique. Section IV evaluates the implementation in terms of the power consumption. Finally conclusion is done in section V.

## II. DESIGN

Fig.1shows the overall architecture of the MB-OFDM that supports both transmitter and receiver. The proposed architecture is designed to process eight complex numbers of at one time with 8-way parallel data paths. By having the high degree of parallel data paths, the baseband modem can operate at 66MHz.The components of the baseband modem in fig 1 are described in the following.

- UWB band (3432, 3960, and 4488 MHz) radio frequency (RF) signals are up/down-converted from/to baseband analog signals through RF/analog circuits .And the analog signals are converted from/to digital signals by DAC and ADC at the sampling frequency of 528 MHz The DAC and ADC drivers, which are interface logics for the converters, are basically parallel-to-serial and serial-to-parallel data converters between 66 and 528 MHz clock domains.
- The preamble ROM contains complex numbers of preamble sequences to be transmitted. Based on the preamble sequence, the packet synchronizer detects a received packet.
- The inverse fast Fourier transform (FFT) module is used to convert the frequency domain signal to time domain. It supports orthogonally. The IFFT block computes the inverse fast Fourier transform (IFFT) of each channel of a P-by-N or length-P input, u. The IFFT implementation is carried out by simply swapping the real and imaginary parts of the incoming data, performing the forward FFT and finally by swapping once again the real and imaginary parts of the data output.
- Modulator is used to convert the bits in to symbols. The carrier frequency is 47MHZ.BPSK supports less B.E.R but also having lower Bandwidth Utilization. QPSK and QAM support Higher Bandwidth Utilization.
- The proposed novel architecture makes use of biorthogonal encoder instead of convolutional encoder. But biorthogonal encoder produces $2^n$-1 output for n+1 input. Also bandwidth utilization is high for biorthogonal encoder. To decode the codes ,a biorthogonal decoder is used.

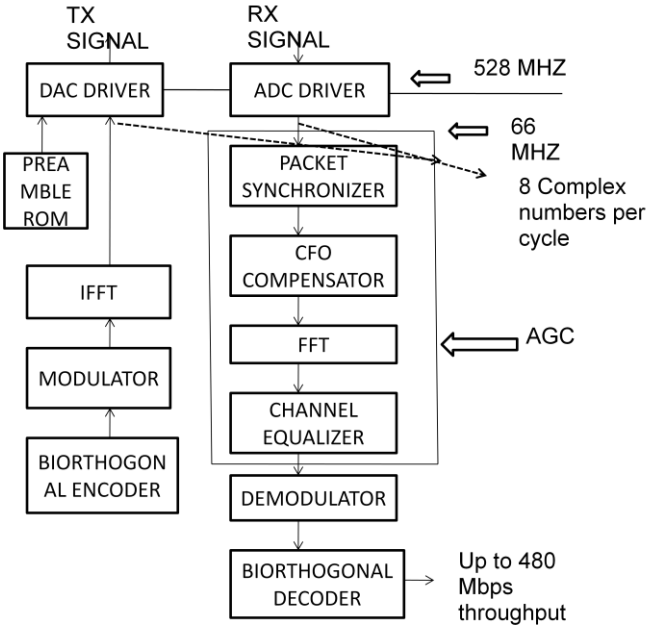


Fig 1: Overall architecture of MB-OFDM baseband to use 8-way parallel data-paths.

## III . Design Optimization

The resource optimization is obtained by using biorthogonal encoder, packet synchronizer, CFO compensator and channel equalizer in the proposed architecture. By using this biorthogonal encoder, the puncture and deinterleaver can be removed and thus the number of gates can be reduced.

***A .Biorthogonal encoder***

Proposed biorthogonal interleaved OFDMA system is used in Multiuser and multicarrier technique that has been recognized as an excellent method for high speed bi directional wireless mobile communication. In conventional interleaved OFDM system, convolution encoder is used as the channel encoder, but it leads to Bandwidth inefficiency and also reduces the throughput of the transmission and reception. The proposed bi orthogonal interleaved OFDM system is having the baud rate of 9600 kbps. This system is ultimately designed for the Bandwidth optimization and also it supports the Multi user transmission and reception of interleaved OFDM system**.**

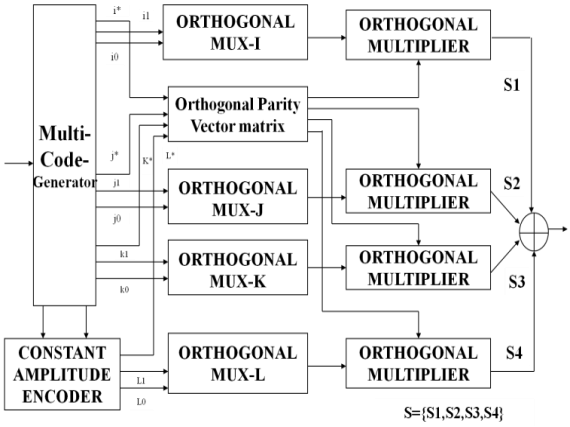


Figure 2.Biorthogonal Encoder

*Multi-code generator*

A multi code generator consists of Serial-to-Parallel Converter and gold convertor. The S/P Converter converts the data bits in to number of branches according to the length of Gold Sequence.

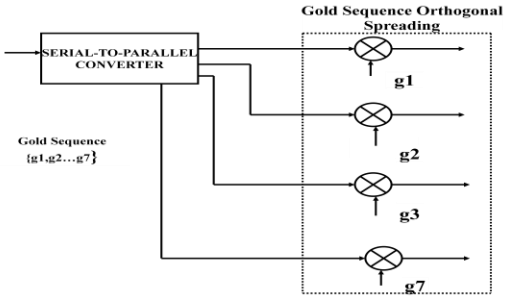


Figure.3 Multicode Generator

A Gold code, also known as Gold sequence, is a type of binary sequence .A set of Gold code sequences consists of (2^n)-1 sequences each one with a period of (2n)-1. It is generated by the exclusive-or of the two maximum length sequences of the same length in their various phases. The output of the multicode generator consists of the (2n)-1output of the gold code sequence and n-1 dummy bits.

***Constant Amplitude Encoder***

The constant amplitude transmission can be realized by the combination of the conventional orthogonal multi-code CDMA and the constant amplitude coding. In this encoder three parity bits ( L*,L1,L0) are generated from three groups of parallel bits (I*,i1,i0),(j*,j1,j0),(k*,k1,k0) according to the following equation

$L_0 = i_0 \ \hat{} \ j_0 \ \hat{} \ k_0$ (1)

$L_1 = i_1 \ \hat{} j_1 \ \hat{} \ k_1$ (2)

` $L_2 = i_2 \ \hat{} j_2 \ \hat{} k_2$ (3)

- The orthogonal multiplexer i output is

I=(0,0,i1,i0)=(0,0,1,0)

- The orthogonal multiplexer j output is J=(0,1,j1,j0)=(0,1,0,0)
- The orthogonal multiplexer k output is K=(1,0,k1,k0)=(1,0,0,0)
- The orthogonal multiplexer l output is l=(1,1,l1,l0)=(1,1,1,0)

*Orthogonal Multiplier*

The Orthogonal Multiplier multiplies the outputs of Orthogonal MUX and Orthogonal parity vector matrix as shown in below. The matrix for orthogonal matrix selector s_1 is given by

$s\_1 = i * . ci + j * . cj + l * . cl$ (4)

$$S_1 = b \begin{bmatrix} C_i \\ C_j \\ C_k \\ C_l \end{bmatrix} = [i^* j^* k^* l^*] \begin{bmatrix} c_i \\ c_j \\ c_k \\ c_l \end{bmatrix} \quad (5)$$

***B. Packet Synchronizer***

There are two classifications of packet synchronization methods by correlation schemes: auto-correlation and cross correlation. To alleviate the high implementation cost of the cross-correlation scheme, 1-bit (sign) reference sequence has been used. It was reported that using that reference incurs just 0.778 dB loss in the cross correlation results. To implement -way parallel packet synchronizer, a conventional approach is to simply duplicate a serial version of the correlator times by making each correlator have a different input window. But the number of adders can be reduced by using the properties of union and intersection of sets. But the adder reduction results in increase in the number of input port to the multiplexer.

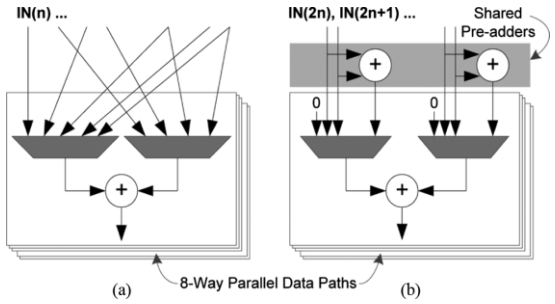


Figure 4. Correlator designs for a packet synchronizer. (a) Wide-input multiplexer based design. (b) Shared pre-adder-based design.

In designing 8-way parallel packet synchronizer, this wide-input multiplexer cost is alleviated by introducing shared pre-adders for eight independent data paths as shown in fig.4 (b). The shared pre-adders consist of 64 adders to add 64 pairs of signals. One of the four inputs is just zero, so the resulting multiplexer is quite less complex. Along with the pre-adders, each multiplexer provides all possible four combinations of summation with two input signals. In consequence, adding all 64 multiplexer outputs can accomplish any combination of summation with 128 input signals.

***C. Carrier Frequency Offset compensator.***

RF signal is transmitted on a carrier frequency of 3432,
3960, and 4488 MHz In the high carrier frequencies, carrier frequency offset (CFO) compensation is crucial for the receiver performance. Compensation for the phase errors is done by iteratively tracking the phase errors of four synchronization symbols. Since intervals between these symbols are different in an increasing order, the compensation is done by multi-level tracking. Both the phase tracking and the compensation require complex multiplications.

There are several slack time slots before each compensation and after each tracking. In this paper an approach has been described to share complex multipliers as well as to minimize the latency by exploiting the slack time slots effectively. Fig. 5 shows the hardware structure of our CFO compensator that is implemented. This deploys a single set of shared complex multipliers without introducing either additional buffer memory or latency

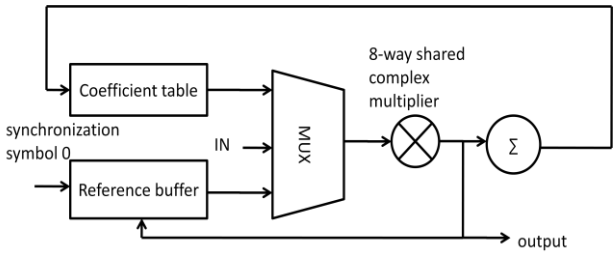


Figure.5. CFO compensator structure.

***D. Channel Equalizer.***

Channel equalization is essential to mitigate signal distortions and plays an important role in improving receiver performance. In MB-OFDM systems, it is sufficient to use a single-tap (zero forcing) frequency domain equalizer in order to undo multipath channel effects. A preamble in MB-OFDM contains six channel estimation sequence (CES) symbols which can be used for channel equalization directly in frequency domain without interpolation processes from time domain. The equalizer algorithm of our system is expressed in the following equations. Because subcarriers except for data subcarriers are no longer used after the equalization, we compute these equations for only data subcarriers. It allows us to implement a channel equalizer with less parallel data paths than 4-way.

$$\boldsymbol{CES_{SUM}(n) = \sum CES_{IN}\,(n)} \qquad \textbf{(6)}$$

$$\boldsymbol{CES_{AVG}\,(n) = \frac{CES_{SUM}(n)}{n}} \qquad \textbf{(7)}$$

$$\boldsymbol{COEFF(n) = \frac{CES_{REF}\,(n)}{CES_{AVG}(n)}} \qquad \textbf{(8)}$$

$$\boldsymbol{OUT(N) = IN(n).COEFF(n)} \qquad \textbf{(9)}$$

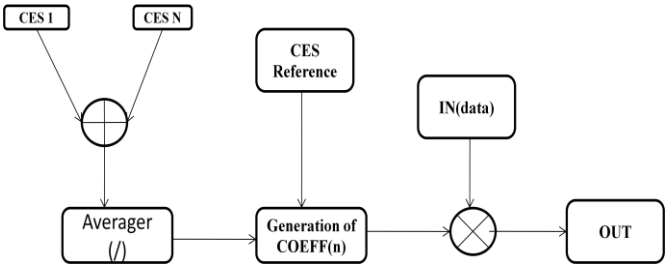


Fig.6. Channel equalizer structure.

Fig.6. depicts the structure of the channel equalizer. The current channel is estimated by averaging all N-received channel estimation sequence (CES) symbols from the FFT module. The channel equalization coefficients are computed to removes effects of the channel using equation (8); they are inverted values of channel estimation results. The output coefficients are obtained by multiplying the input data with the channel estimation results.

***E. Biorthogonal decoder.***

Fig.7. illustrates the block diagram of the biorthogonal decoder.

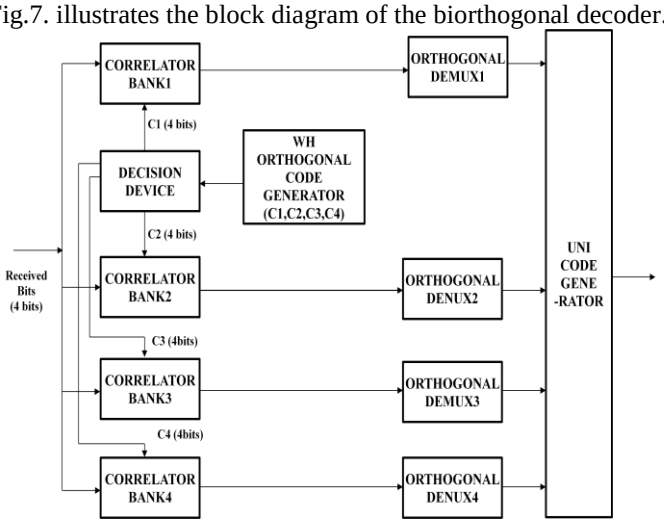


Fig.7. Biorthogonal decoder.

A decoder is a device which does the reverse operation of an encoder. It performs the reverse operation of the biorthogonal encoder. Unicode generator performs the reverse operation of the multicode generator.

## IV. Simulation Results

To evaluate the overall system performance, we performed both floating-point and fixed-point simulations. Throughout this evaluation, we simulated reception of packets with 1kB frame payloads and standard preamble at the highest data rate, i.e., 480 Mbps. The proposed technique could achieve a gate count reduction of 32.47% without any degradation in system performance.

Table I compares the previous implementation using convolutional with that of the implementation with biorthogonal encoder .From the table, it's clear that the number of gates, LUT, Slice, non clock net and path delay required for OFDM using biorthogonal is less as compared to OFDM using convolutional . Convolutional encoder makes use of puncturer and deinterleaver. Puncturing is a procedure for omitting some of the encoded bits at the transmitter and inserting dummy "zeros" into the decoder at the receiver, in place of the omitted bits.

Table 1: Comparison between biorthogonal and convolutional encoder

| COMPONENTS | OFDM USING CONVOLUTIONAL | OFDM USING BIORTHOGONAL |
|---|---|---|
| LUT | 100 | 20 |
| SLICE | 60 | 10 |
| GATE | 11700 | 7900 |
| NON-CLOCKNET | 3.50ns | 3.13ns |
| PATH DELAY | 6.959ns | 6.263ns |
| POWER | 79.81µw | 39.52µw |

In addition to the above comparison, it is also interesting to find that implementation using biorthogonal does not double the number of resources required to implement it. The number of adders/subtractors required for implementation using biorthogonal encoder is 5 whereas that required for implementation using convolutional is 9. When the number of buffers required is compared, biorthogonal implementation requires lesser number of buffers as compared to that of convolutional implementation. The number of buffers required for biorthogonal implementation is 16 as compared to covolutional which requires 46 buffers. As a result of this large difference in the number of buffers, propagation delay for convolutional implementation is high as compared to the biorthogonal implementation. The total CPU time for the biorthogonal implementation is 5.23 seconds which is 5.77s for the convolutional implementation. Also the number of IOs required for biorthogonal is 22 as compared to 46 which is for convolutional implementation.

Also biorthogonal encoder produces $2^n$-1 output from n+1 input. So puncturer is not required in biorthogonal encoder. Also biorthogonal encoder removed both types of errors, so it does not make use of interleaver. By the above analysis it is shown that the gate count could be reduced by 32.47%..

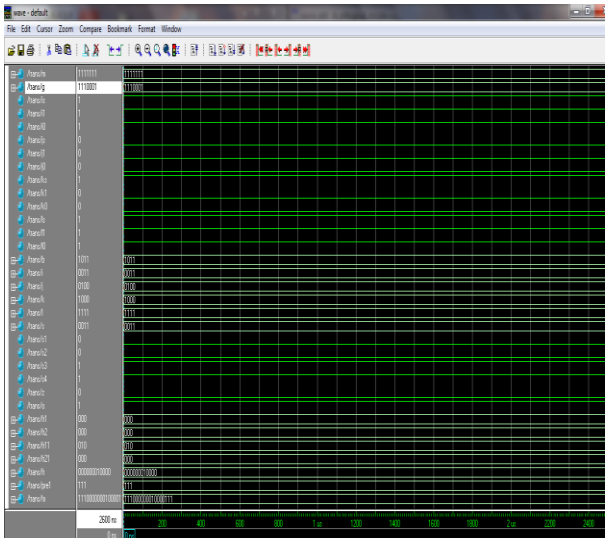

Figure.8.wave default signal for OFDM transmitter using biorthogonal encoder

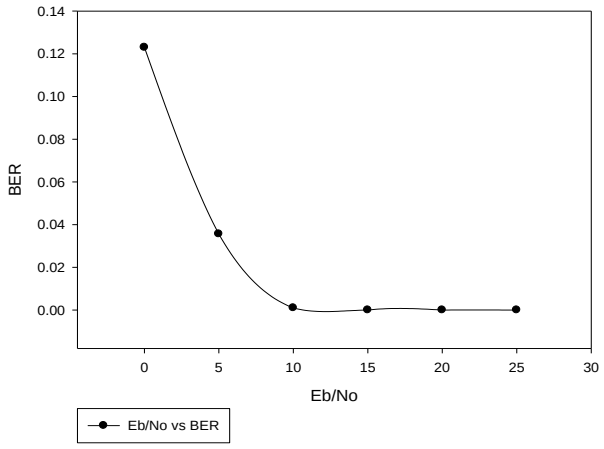


Figure 9. SNR vs BER of proposed system.

Figure.8 shows the simulated modelsim output for OFDM transmitter using biorthogonal encoder. Also, the functionality of the proposed design can be verified by implementing a prototype system based on FPGA. The proposed architecture is to be implemented in hardware kit Xilinx Sparton 3-E. Table 2 shows the comparison between convolutional encoder and biorthogonal encoder. In biorthogonal encoder the BER is between 0.5dB and 0.28dB for the SNR 0-25dB, data rate is improved and also the power consumption is reduced from 5.5v to 3v. Bandwidth utilization is also maximum compared to convolutional encoder.Figure.9.shows the SNR vs BER plot.

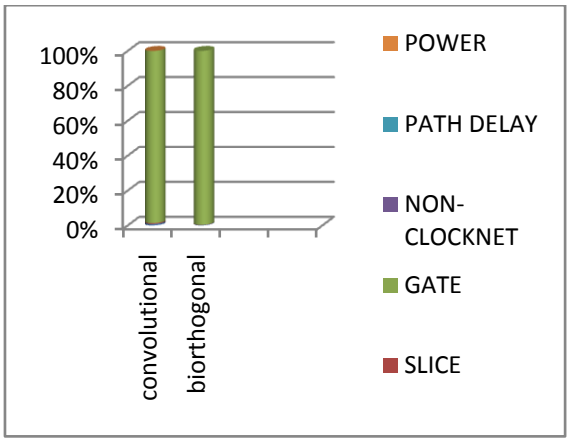


Figure.10 Estimated resource usage

Table 2:Comparison between biorthogonal encoder and convolutional encoder

| specification | Eb/No | BER |
|---|---|---|
| Convolutional coding | 0.18 | $1.61e^{-60}$ |
| Biorthogonal encoding | 0.18 | $5.57e^{-138}$ |

## V. Conclusion

In this paper, we introduced 8-way parallel architecture which operates at 66 MHz system clock. In order to alleviate the resource problem in parallel architectures, we proposed novel optimization techniques .The proposed MB-OFDM architecture made use of biorthogonal encoder instead of convolutional encoder. From the resource efficient design, it was estimated that the gate count could be reduced by 32.47% on average, while none of techniques degraded the overall system performance. With 0.18- μm CMOS process, the gate count of the entire baseband modem were about 7900 gates for biorthogonal encoder and 11700 gates for convolutional encoder at 66 MHz clock rate, respectively.

## ACKNOWLEDGMENT

First author would like to thank the support and guidance offered by Mr.S Janardhana Prabhu, Faculty of ECE, Anna University, Regional Centre, Madurai.

## References

[1] SeokJoong Hwang, Student Member, IEEE, Youngsun Han, SeonWook Kim," Resource efficient implementation of low power Mb-OFDMphy baseband modem with highly Parallel architecture", IEEE Transactions On Very Large Scale Integration (Vlsi) Systems, vol. 20, no. 7, pp.1248-1261,july 2012.
[2] C.-H. Shin, S. Choi, H. Lee, and J.-K. Pack, "A design and performance of 4-Parallel MB-OFDM UWB receiver," IEICE Trans. Commun., vol.E90-B, no. 3, pp. 672–675, Mar. 2007.
[3] W. H. Wu, Y. W. Wu, and H. P. Ma, "A 480 Mbps MB-OFDM-basedUWB baseband inner transceiver," in Proc. IEEE Asia Pacific Conf.Circuits Syst. (APCCAS), 2008, pp. 164–167.
[4] A. Chandrakasan and R. Brodersen, "Minimizing power consumptionin digital CMOS circuits," Proc. IEEE, vol. 83, no. 4, pp. 498–523,Apr. 1995.
[5] A. Safarian, A. Yazdi, and P. Heydari, "Design and analysis of an ultrawide-band distributed CMOS mixer," IEEE Trans. Very Large ScaleIntegr. (VLSI) Syst., vol. 13, no. 5, pp. 618–629, May 2005.
[6] C. Cheng and K. K. Parhi, "High-throughput VLSI architecture for FFT computation," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 54, no. 10,pp. 863–867, Oct. 2007.
[7] A. Chindapol and J. A. Ritcey, "Design, analysis, and performance evaluation for BICM-ID with square QAM constellations in Rayleigh fading channels," IEEE J. Select. Areas Commun., vol. 19, no. 5, pp.944–957, May 2001.
[8] A. Troya, K. Maharatna, M. Krstic, E. Grass, U. Jagdhold, and R.Kraemer, "Efficient inner receiver design for OFDM-based WLAN systems: Algorithm and architecture," IEEE Trans. Wirel. Commun.,
[9] vol. 6, no. 4, pp. 1374–1385, Apr. 2007.
[10] A. Batra, J. Balakrishnan, G. R. Aiello, J. R. Foerster, and A. Dabak, "Design of a multiband OFDM system for realistic UWB channel environments,"*IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 9, pp.2123–2138, Sep. 2004.
[11] E. Akay and E. Ayanoglu, "Achieving full frequency and space diversityin wireless systems via BICM, OFDM, STBC and Viterbi decoding,"