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Design of Low Power Energy Recovery Full Adder Circuit with Comparative Analysis

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Abstract : *Energy recovery is a technique originally developed for low power digital circuits. Energy recovery circuits achieve low energy dissipation by restricting current to flow across devices with low voltage drop and by recycling the energy stored on their capacitors by using an AC type supply voltage. In this paper there apply energy recovery technique to the logic circuits since the clock is typically the most capacitive signal in the chip. The purposed energy recovery logic circuit scheme recycles the energy from the capacitance in each cycle of the clock. In this paper an 1-bit Full Adder energy recovery logic is purposed with the design of advanced Energy Recovery Logic Inverter circuit. This purposed Full Adder circuit is designed with low power energy recovery techniques and is compared with conventional efficient charge recovery logic circuit and this is done by using 0.25 µm CMOS technology in SPICE.*
Keywords - *Adiabatic, AERL, CMOS, Clock voltage, Delay, ECRL,*

a. INTRODUCTION

Until quite recently, the power consumption of VLSI computation devices had not been the major limiting factor in improvements and advances in microelectronic technology Current processors can consume 140W, drawing over 100A of current in the process [1] however today the demand for portable consumer electronics, ubiquitous computing devices [2] is increasing rapidly means that power efficient computation has become more important in widely deployed technologies rather than being confined to niche and specialist areas. The popularity of complementary MOS technology can be mainly attributed to inherently lower power dissipation and high levels of integration. However as the dimensions of CMOS technologies have shrunk, so that for nanometer technologies the thickness of the gate dielectric is a countable number of atoms [3], traditional power reduction techniques like voltage scaling have ceased to be as effective, and new issues like source-drain leakage and even gate leakage have become significant sources of power dissipation. Recently the current trend toward ultra-low power has made researchers search for techniques to recover/recycle energy from circuits.

This paper studies the energy recovery logic families for power efficient circuit design. For this purpose efficient charge recovery logic inverter circuit and Full Adder circuit are taken for present study. Also an advance energy recovery circuit is proposed with reduction in circuit complexity which further reduces power consumption. A comparison of power consumption is also shown between proposed energy recovery logic circuit and existing energy recovery logic families.

II. BASIC PRINCIPLE

Energy dissipation can be divided in two types of losses: one is adiabatic loss and other is non adiabatic loss. Adiabatic loss is generated due to switching resistance of the transistor when current flows through it. This type of loss is less because the switching resistance offered by the charging path is low as the functional block is in parallel with the charging MOS transistor.

The non adiabatic losses occur due to the threshold voltage of the transistor used in charging path. During the recovery phase, the energy is only partially recovered from the output load C_L. When the output voltage goes below the threshold voltage then the PMOS transistor goes in off condition and logic blocks further recovers the energy. During the evaluation phase this uncovered charge gets dissipated as loss when the new input gets applicable.

The energy recovery logic circuits offer considerable improvement in power consumption over static CMOS at low frequencies [4]. Energy recovering logic reuses charge and therefore consumes less power than non-energy recovery logics. An energy recovering logic charges the load capacitance during logic high to drive the gates rather than draining charge to ground [5]-[7]. In non energy recovering logic the charge applied to the load capacitance during logic level high is drained to ground during logic level low.

III. EFFICIENT CHARGE RECOVERY LOGIC (ECRL)

2.1 Inverter Circuit

The schematic of the ECRL inverter is shown in Fig 1. An AC power supply Φ [8] is used to recover and reuse the supplied energy. In ECRL logic precharge and evaluation are performed simultaneously. Full output swing is obtained because of cross coupled PMOS transistors both in the precharged and recovery phase. This circuit suffers from non adiabatic loss. This logic has the similar circuit arrangement as cascade voltage switch logic (CVSL) with differential signaling. It is assumed that signal 'In' is at high and signal 'Inbar' is at low level. At the beginning of a cycle, when the supply clock Φ rises from zero to V_{dd}, signal 'Out' remains at a ground level, because 'In' signal turns ON the transistor MN2 and 'Outbar' follows Φ through MP1. When Φ reaches V_{dd} the outputs hold valid logic levels. These values are maintained during the hold phase and are used as inputs for evaluation of the next stage. After the hold phase, Φ falls down to a ground level and 'Outbar' node returns its energy to Φ so that the delivered charge is recovered. Thus, the clock Φ acts as both a clock and power supply [9].

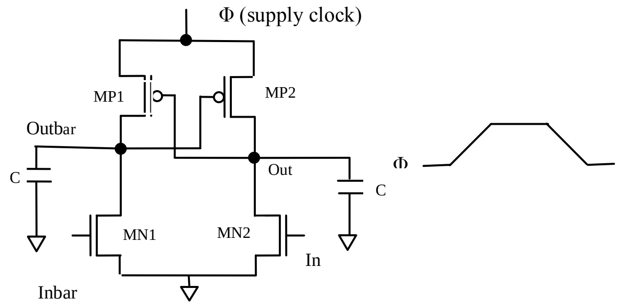

Fig 1: ECRL inverter & Supply clock

3.2 ECRL Adder

The schematic of ECRL adder is shown in Fig 2

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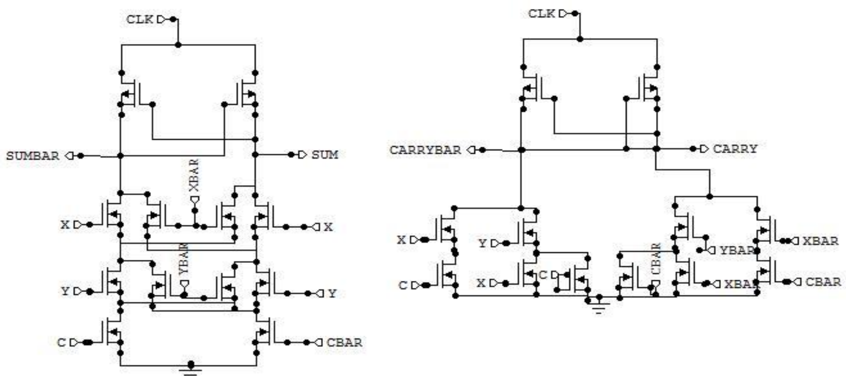

Fig 2: ECRL adder

IV. PROPOSED ADVANCE ENERGY RECOVERY LOGIC CIRCUIT (AERL)

Various ERC's present today have two conducting paths for charging and discharging of load capacitor. There only path is conducting at any instant of time. So design of circuit is more complex. So energy consumption of circuit is more. The delay of circuit also increases. In purposed energy recovery logic circuit, there exist same path for charging and discharging of load capacitor. So circuit complexity is reduced. In this section working of purposed energy circuit has been explained.

4.1 Inverter circuit

The schematic of the proposed energy recovery logic inverter is shown in Fig 3. The clock used for this design is shown in Fig 4

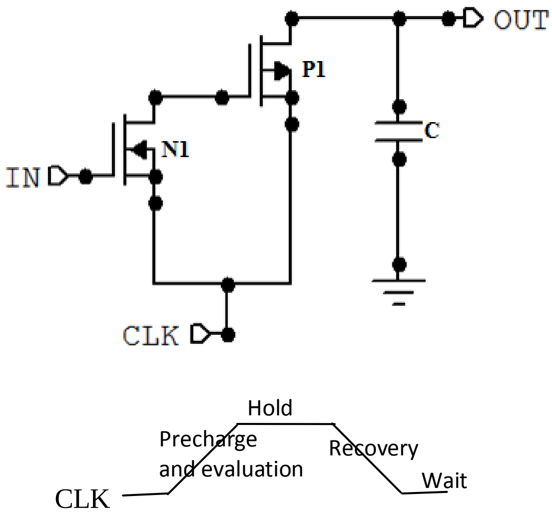

Fig 3: Proposed Advance ERL Inverter

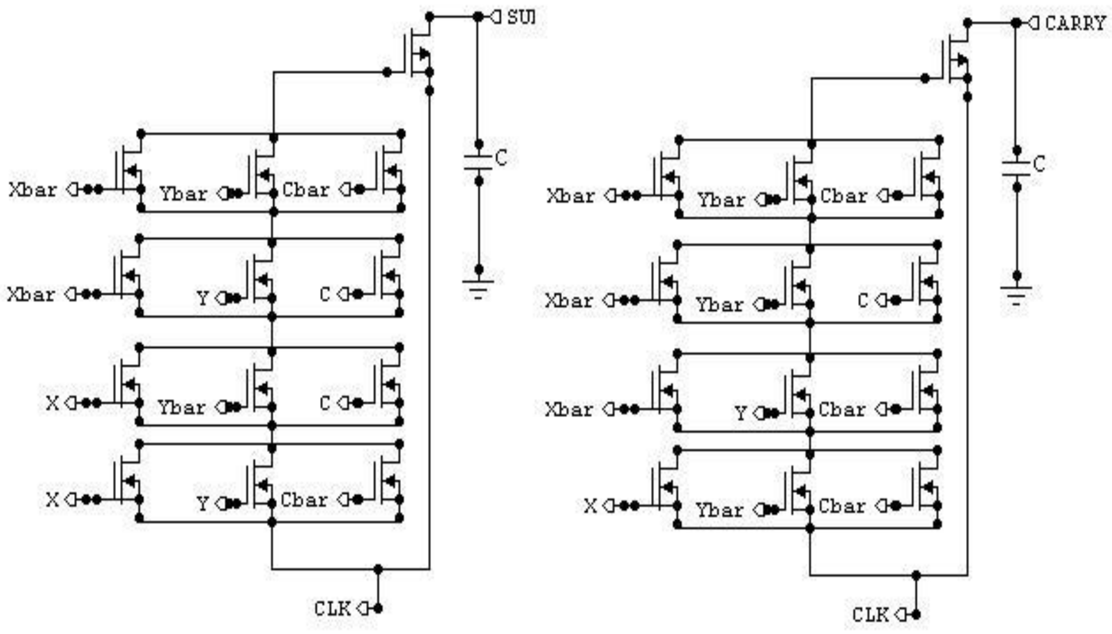

Fig 4: Supply Clock

Let us assume IN is at high i.e. logic “1” and capacitor is initially uncharged. When IN is high N1 transistor is *on* and gate terminal of transistor P1 is connected to source as shown in Fig 5. So M1 transistor is equivalent to *diode*. Any change in CLK value does not impact the OUT node which is still at low voltage because diode is in reverse mode and any charge does not accumulate at capacitor C. Hence it behaves like open circuit. So OUT is low i.e. logic “0”.

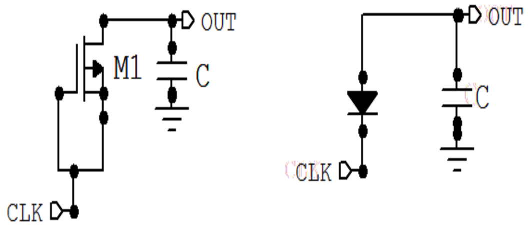

Figure 5: when IN is high

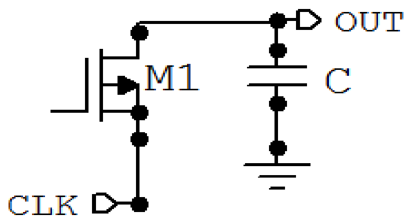

Figure 6: when IN is low

Equivalent Circuit of Purposed ERL Inverter

Now let us assume IN is at low i.e. logic “0”. When IN is at low then N1 transistor is *off* and P1 transistor is on as shown in Fig 6. OUT node follows the CLK. Thus, the CLK acts as both a clock and power supply.

4.2 ERL 1-bit Full Adder

The schematic of Purposed ERL adder is shown in Figure 7.

Fig 7: ERL Full Adder

V. SIMULATION RESULTS

This section describes simulation results of implemented circuits. Comparison has been made among the various energy recovery logic families. First simulations of proposed ERL combinational gates have been presented. The energy and delay variations with different clock voltages are analyzed. The proposed ERL circuits have been compared with different energy recovery logic circuits. Simulations have been performed using 0.25µm CMOS technology in SPICE.

Table 1 shows the delay of ECRL inverter and proposed ERL inverter at various load capacitances. The ERL inverter shows the small delay as compared to the ECRL inverter as shown in as shown in Fig 8. The frequency of clock is 5MHz

Table 1: Delay variation of ECRL inverter and proposed ERL inverter at different load

Load Capacitance (fF)	Delay (nS)	
	EACRL	ERL (proposed)
10	24.885	6.711
20	25.190	8.971
30	25.523	10.833
40	25.557	12.108
50	25.558	13.150
60	26.294	14.149
70	26.306	14.968
80	26.312	15.763
90	26.360	16.509
100	26.770	17.431

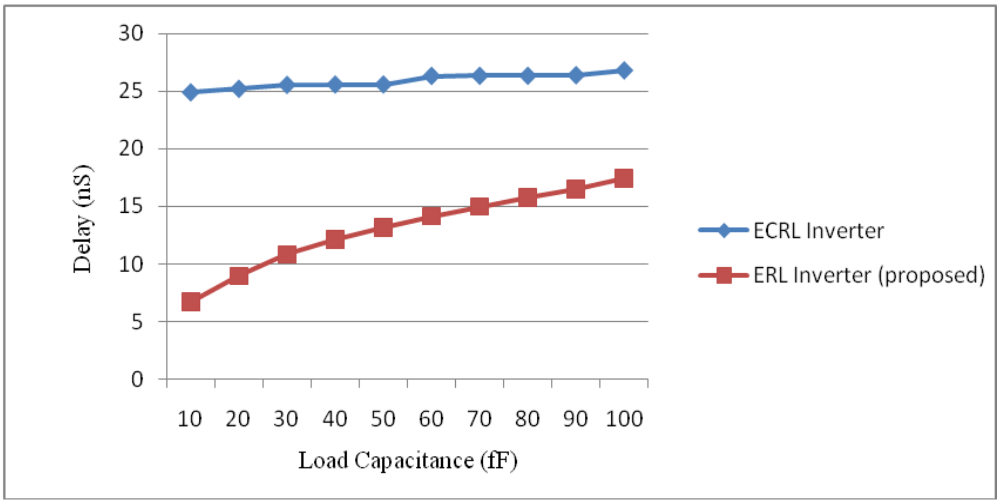

Fig 8: Delay vs. load capacitance of ECRL inverter and ERL (proposed) inverter

Finally the power consumption of ECRL and purposed ERL full adder are compared at different input voltages as shown in Fig 9. The power consumption of all energy recovery full adders is increased with increase in input voltages.

Table 2: Power Consumption of ECRL and proposed ERL full adder at different clock voltage

Input Voltage(V)	Power Dissipation (pW)	
	ECRL	ERL (proposed)
3.0	406.118	355.751
3.2	482.702	418.243
3.4	577.041	499.079
3.6	679.149	596.571
3.8	807.933	713.201
4.0	960.191	844.043
4.2	1427.7	1011.6
4.4	1363.9	1214.5
4.6	1630.2	1462.0
4.8	1960.2	1764.4
5.0	2360.2	2134.0

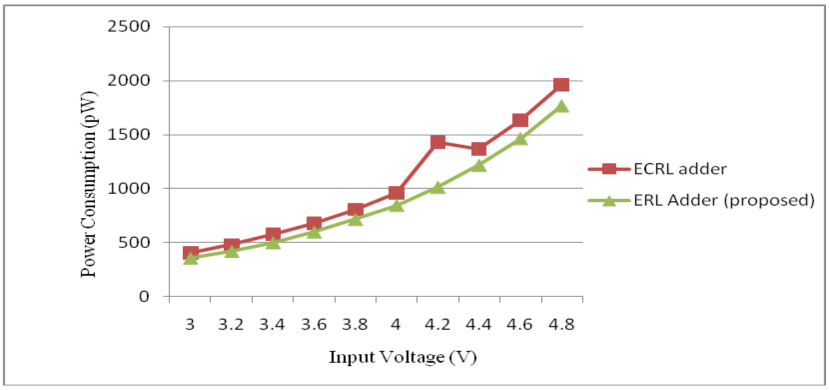

Fig 9: Power consumption vs. input voltage of ECRL adder and proposed ERL adder

The power consumption of proposed ERL full adder shows the less power consumption as compared to ECRL full adder. Proposed circuit also shows superiority in terms of transistor count with earlier reported circuits. So, proposed circuit's shows better performance in terms of power consumption and transistor count.

VI. CONCLUSION

From simulation results it may be observed that purposed ERL circuits offers improved performance in power dissipation with reduction in circuit complexity. Adiabatic logics are highly helpful for implementation of power efficient designs. These logics are alternative technique for circuit design as compared to pipelining and other techniques that requires high circuit complexity. Energy recovery logics has successfully used for fundamental VLSI blocks such as adder, subtractor and other arithmetic circuits. According to simulations results in 0.25 μm technology, delay of proposed ERL inverter is less than other energy recovery circuits. Also the power consumption of proposed ERL adder has been compared with ECRL full-adder and ERL circuit shows improved performance.

Hence it is concluded that the purposed design circuit will provide a platform for designing high performance and low power digital circuits such as digital signal processors, adders and multiplexers. One of the disadvantages of energy logic circuits is that the speed of operation is reduced with reduction in power dissipation.

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