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Integrated on-chip design for parameter monitoring via integration of nodules with soft computing

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Abstract: *Monitoring of environmental parameters like temperature, humidity, pH level, gas presence, and others accurately is a multi-domain signal processing task. This involves data sensing, filtering, processing, and actuating based on the processed values. In order to perform this task, various architectures have been proposed, which range from using Arduino-based controller, DSP controllers, Raspberry-Pi controllers, and FPGA devices. Each of these implementations has their own nuances, some of them have limited processing capabilities, while others have high cost of deployment. In this paper, we propose a novel hybrid methodology which combines the power of FPGA with the flexibility of soft computing algorithms in order to devise a highly efficient environment monitoring system. This uses the NiOS softcore for multi-media processing & FPGA devices for high speed data acquisition from nodules. The combination of these systems enables the system designer to achieve both high throughput with increased speed of operation. Our results showcase that the proposed system has 20% more throughput than its counterparts and is 15% better in terms of operating speed.*

Key Word: *Actuating, filtering, monitoring, nodules, sensing.*

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I. Introduction

In order to effectively sense and process environmental data like temperature, humidity, pressure, gas levels, and other information the following steps have to be followed,

- Sensor selection, wherein an accurate and precise sensor / sensor array must be selected in order to sense the parameter under consideration. The selection of sensors usually decides the performance of the system, better the sensor, higher will be the system performance.
- Pre-processing of sensed data, wherein algorithms like denoising, missing value removal, bound checking, and others are applied to filter the sensed data
- Data processing, where the filtered data is processed using application specific techniques
- Actuation, this is the most important step, wherein actions are taken to turn ON/OFF devices based on the processing of data

In this paper, we have evaluated different algorithms that perform these tasks in an effective manner, and also provide a better and more sophisticated approach towards designing such a system. Our system combines the best techniques from these algorithms in order to create a novel and efficient solution for signal processing.

In this work, we have combined the best signal pre-processing techniques along with the most optimum actuation techniques in order to develop a sophisticated and highly efficient data sensing and actuation system. This system is able to combine the advantages of hard-core processors like FPGAs with soft-core processors like NiOS in order to reduce the delay and improve the system performance.

In the next section we have described different techniques for sensor system design, followed by the proposed approach, and its results. This text concludes by suggesting some interesting recommendations about this system, and the future research that can be conducted to further improve the system's performance.

II. Literature Survey

A Signal processing systems that use combination of hardware and software co-processing are gaining a lot of popularity. For instance, the work in [1], develops a Wireless multimedia sensor network by combining hardware design and software design. They have used spartan 6 FPGA for processing the data. In their work, the camera interfacing is done and full hardware implementation is done using I2C, VGA, and OV7670 controller units. There are no statistical results indicated in their work, but using their work it is clear that any kind of sensor and actuator interfacing can be done solely using FPGAs. Moreover, they also make it clear that high speed sensors (like cameras and VGA displays), must be directly interfaced with FPGA to get optimum performance. A low power interface design using neural networks (NN) for sensor interfaces is defined in [2]. The authors have been able to achieve power consumption as low as 34nW, and a very low delay of 2 micro-

seconds by making use of the inherent low power and low delay capabilities of STM32 architecture.

The work in [3] uses a video powered FPGA network to monitor smart cities in real time, and with high performance. They have used hardware-based FPGA processors to perform this task. There are no statistics mentioned in the paper, but their work uses low power components to reduce the power consumption of the developed system. A similar work is mentioned in [4], wherein authors have used stochastic network calculus to model WSNs. Using their simulations, they have concluded that stochastic processes are very complex, and that the delay is inversely proportional to the complexity of the process under test. An interesting research is done in [5], wherein reconfiguration is used in order to improve the system's performance for WSN design. From their research, we can observe that WSN design can save energy by upto 50% and can reduce the delay by upto 35% when compared to only hardware design. These results are true if there is only sensing of data, and there is limited processing on the given input data. In contrast, the work in [6] uses only Zed board based multi-media controller for designing WSN. Using this controller board, the delay and energy requirements are reduced when compared to MSP 430 controller. They suggest that using an asynchronous circuit design is almost similar to using a synchronous circuit design when developing WSN nodes. As both MSP and Zed board are multi-media controllers, thus this comparison is useful when designing systems that are based on purely multimedia applications, like audio, image and video communication. These node designs are further extended in [7], wherein a node design is presented that can perform CSMA/CA (carrier sense multiple access with collision avoidance). This design is also developed completely on hardware without any co-processor design; therefore, it achieves high throughput and low energy of operation.

A co-processor design that uses NIOS 2 soft-core is defined in [8]. The paper [8] is the motivation for the work proposed in this text. Using their work, it is observed that soft-core processors do not increase performance parameters like delay and energy consumption exponentially as the number of inputs are increased. This forms the basis of this paper, because in the design of this paper multiple hardware components are needed to be interfaced. Multi-sensors are interfaced in [9], wherein environmental sensing capability devices are used. These devices have the capability to sensor multiple environment parameters. They have used radar and ultra-sonic sensors to form a WSN unit. The performance analysis shows that reconfiguration can reduce the delay but increases the energy consumption for multi-component interfacing. A multi-component interface unit is designed in [10], wherein temperature prediction is done using artificial neural networks (ANN), using the values of temperature, humidity and pressure. Results indicate that the performance of system using multi-components for WSN design can be optimized with the help of reconfigurable processing or soft-core processing. An extension to the work in [10] is defined in [11], wherein plant monitoring application is designed using the components used in [10]. It also confirms the fact that soft-core processing is a good option when designing multi-component interfaces. Multi-media applications with FPGA are increasing day-by-day. This can be seen from the works in [12-14], wherein multiple sensors are interfaced along with multi-media nodes for better processing of data. They have used soft core processing to optimize the performance when using multi-media sensors. Using soft-cores have further been confirmed in [15-17], wherein RAM based implementations of soft-core processors are defined. These implementations confirm that usage of RAM-based softcore processors pave the way for better FPGA system designs. A similar approach is given in [18], wherein DSP processors are found to be using soft-cores for a better system performance.

Thus, from this review it is evident that combination of soft-core processors with hardware design can improve the performance of FPGA-based WSN designs. Single component interfacing can be effectively implemented using only hardware design, but as the number of components increase, there is a need to shift from simple hardware design to hardware software co-design. This performance pattern forms the basis of the work in this text, and in the next section the proposed system design is given with its performance evaluation.

III. Proposed System Design

The proposed system is a combination of a FPGA embedded hardware processor and soft-core processors. This combination is done intelligently so that all the high-speed sensing and actuation tasks are done via the hardware processor, while the low priority and slower tasks are performed using the soft-core processors. In this work, the NiOS 2 soft-core processor is used, which is built on top of the hardware layer of the FPGA. The FPGA hardware works at exactly the same clock speed as defined in the spec sheet of the processor, while the soft-core processor has different layers on top of the main processing unit. These layers are majorly application processing layers, that combine different mechanical functions into an API (application programming interface), and present it to the upper layers. This helps the upper layers to perform high-level functions like interfacing with serial ports, USB interfaces, use of high-level programming linguistic functionality (like using Python or C), and other high-level tasks. These high-level tasks if implemented directly on the FPGA will be ineffective in terms of the time needed to develop them, and the number of errors that might arise due to implementing the internal mechanical components of these tasks.

For instance, in order to send serial commands to a RS232 interface, one needs to interface the RS232

hardware with the FPGA, and then send individual signals on the bus. These signals have to be pre-programmed for each RS232 instruction, and the hardware description language (HDL) needs to be changed in case the application demands a different set of RS232 instructions. This re-programming requires the entire FPGA to be erased and then re-programmed, which might not be ideal in case of industry scenarios, where the FPGAs are placed directly on the field.

In such cases, partial reconfiguration can work, but the configuration is limited in terms of functionality and configuration level to the FPGA. Moreover, changing the codes or functionality via reconfiguration tends to insert errors in the already working functionality of the FPGA device. Therefore, it is not recommended to use reconfiguration of industry environments, unless it is utmost required. Thus, researchers have recommended the use of soft-core processors to solve these issues.

Taking into consideration the advantages of soft-core processing, this text uses a combination of both high-speed hardware design and soft-core design in order to design a hybrid and highly efficient sensor nodule design. A nodule is basically a combination of sensor modules and communication equipment, which can be pluggable to any system with the need of minimum interfacing. The following Fig.1 showcases the design of our proposed wireless sensor nodule,

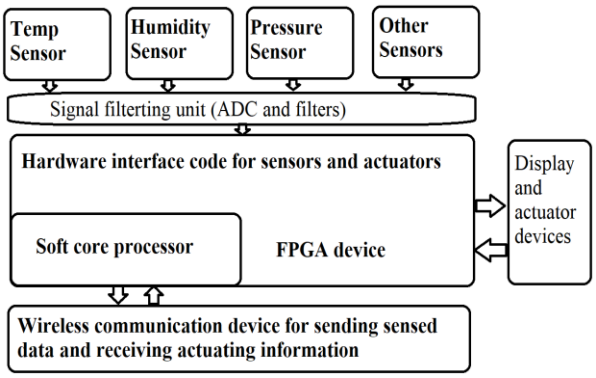

Fig.1: Design of the proposed system

From the design, the working of the proposed system can be described as follows,

- The sensors are interfaced directly with the signal filtering unit
- These sensors have their data in analog format, and might need some pre-processing before actual data recording
- The Signal filtering unit combines an ADC unit along with an ALU to process the sensed data
- This unit also consists of multiplexers that can be used to combine data from different sensors into a single multiplexed channel
- The FPGA device then sends relevant signals to these devices in order to get the final values from the ADC
- These values are then processed on the FPGA device directly, and actuation signals are generated
- These signals are used to modify the display data
- These signals are also used to control the connected actuators (if needed)
- The FPGA hardware uses an internal soft-core processor like NIOS 2 to send these signals to the soft-core unit
- The soft-core unit uses these signals, performs signal processing operations like clustering, thresholding, and others
- These operations are performed in order to find out patterns from the input data which can be used for intelligent processing
- These patterns are sent through a wireless communication channel which can be Zigbee, GSM, WiFi or any other application specific channel
- The data is received at the receiving side, and control signals are generated at the receiver
- The receiver will send these signals back to the transmitter
- Based on these signals, the transmission device can change the actuation signals, and control the devices accordingly

In our proposed system, the sensors used are LM35 for temperature sensing, YL69 for moisture sensing, EC sensor, pH sensor, and SY230 humidity sensor. These sensors are interfaced with and PMOD AD2 ADC for conversion into digital values. The multiplexing is done with the help of 4051 Mux device. All these

devices are connected to a Nexys 2 FPGA board which is powered by the Spartan 3E processor module. The processor is also interfaced with a HD4470 16x2 LCD module for display of data. While the LM293D device is used for actuating the motor based on the data obtained from these sensors.

The soft-core processor is connected to the GSM module, which allows the system to consume lower power, and have high efficiency of wireless data trans-communication. Due to the interface of GSM module with the soft-core processor, there is a possibility of adding multiple application level interfaces to the system. In this work, a simple data communication interface is developed in C language, which takes data from the FPGA and communicates it over the GSM medium. The communicated data is displayed on the operator's mobile device, for on-the-go analysis of sensed data. We analyzed the results of this system in terms of area, power and delay constraints. The results were compared with some of the other state-of-the art implementations, and the comparative analysis was performed. These results are showcased in the next section of this text.

IV. Results and Analysis

In order to analyze the results of the prepared system, we compared the results with some of the standard architectures that are presented by researchers over the years. Table 1, 2 and 3 indicates the results in terms of number of sensors, and the area, power and delay parameters for the designed system. In order to perform this result analysis, the systems were developed manually and tested for the same hardware configuration. Moreover, the number of sensors were increased and reduced in order to evaluate the change in power, area and delay capabilities of the designed system. From the table, researchers can identify the main advantages of each of the configurations, and then decide which kind of configuration is suitable for a particular application.

From table 1, we can observe that the energy consumption of the devices increases exponentially when only hardware implementation is used. This is due to the fact that as the number of sensors increase, the overall static and dynamic power increases rapidly, while in contrast, the proposed model has higher energy requirements for less number of sensors, but the energy requirement curve almost remains constant (or increases infinitesimally) as the number of sensors are increased.

Table- no 1: Energy consumption for the nodule

Number of sensors	Energy Hardware (mJ)	Energy Reconfiguration (mJ)	Energy Proposed (mJ)
1	12.5	15.6	21.9
2	15.9	17.9	22.1
3	19.3	22.7	22.6
4	25.9	29.3	22.9
5	29.6	34.7	23.8

The next table 2 indicates the effect of delay (operating speed) among different sensors.

Table- no 2: Delay needed for the nodule

Number of sensors	Delay Hardware (us)	Delay Reconfiguration (us)	Delay Proposed (us)
1	2.6	2.8	15.3
2	9.8	10.6	18.9
3	16.7	21.6	21.9
4	34.6	39.4	27.6
5	53.4	57.9	31.7

The delay also follows the same nature like the energy curve. It is much lower initially, but as the number of sensors increase, the delay increases exponentially for the proposed system. The next comparison is very interesting; it indicates the change of area requirements as the number of sensors increase. It can be seen from table no 3 as follows,

Table- no 3: Area comparison

Number of sensors	Area Hardware (sq. nm)	Area Reconfiguration (sq. nm)	Area Proposed (sq. nm)
1	15	23	45
2	15	23	45
3	15	23	45
4	15	23	45
5	15	23	45

From the table, we can observe that there is no change in the hardware needed as the numbers of sensors are increased. This is due to the fact that the area is fixated based on the number of gates, number of flip-flops and other RTL components present in the design. Thus, we can observe that the proposed design is very effective in terms of power, and delay, but requires slightly higher hardware due to the presence of soft-core processing. The next section concludes this text, and suggests come interesting research that can be taken up jointly with this research.

V. Conclusion and Future Work

The delay and energy consumption of the proposed work gets better as the number of sensors are increased, but for lower number of sensors it is better to use a direct hardware implementation. The reconfiguration mode implementation is not good and performs moderately in any kind of system implementation for the wireless nodule case. The system's delay performance improves from -500% for 1 sensor, to +40% for 5 sensors. It is evident that this performance will further improve as the numbers of sensors are further increased. The energy performance also improves from -75% for 1 sensor to +20% for 5 sensors, and this performance will also further improve as the numbers of sensors are increased.

The work can be further extended by adding Q-learning algorithms for improving the energy and delay efficiency of the system. Such a mechanism can give rewards to the soft computing unit when it consumes less power and reduces operation delay. This will help the soft-computing system to further perform optimally, and reduce the delay and energy consumption of the system.

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