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High Efficient Complex Parallelism for Cryptography

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Abstract: *Cryptography is an important in security purpose applications. This paper contributes the complex parallelism mechanism to protect the information by using Advanced Encryption Standard (AES) Technique. AES is an encryption algorithm which uses 128 bit as a data and generates a secured data. In Encryption, when cipher key is inserted, the plain text is converted into cipher text by using complex parallelism. Similarly, in decryption, the cipher text is converted into original one by removing a cipher key. The complex parallelism technique involves the process of Substitution Byte, Shift Row, Mix Column and Add Round Key. The above four techniques are used to involve the process of shuffling the message. The complex parallelism is highly secured and the information is not broken by any other intruder.*

Keywords: *Advanced Encryption Standard (AES), Complex Parallelism, Cryptography, Substitution Byte(S-Box).*

I. Introduction

Cryptography, often called encryption, is the practice of creating and using a cryptosystem or cipher to prevent all but the intended recipient(s) from reading or using the information or application encrypted. A cryptosystem is a encryption technique which is used to encode a message and recover the original one. The recipient can view the encrypted message only by decoding it with the correct algorithm and keys. Cryptography is used primarily for communicating sensitive material across computer networks. In crypto-text, the document is unreadable unless the reader possesses the key that can undo the encryption. Encryption is becoming more and more important for day to day life for protecting the data/information. In 1997 U.S Military government found the Data Encryption Standard (DES) Technique. In 2001, the National Institute of standards and Technology (NIST) found the Advanced Encryption Standard (AES) Technique. It can be implemented in hardware. There are a lot of disadvantages in DES Technique. It is insecure and the message is easily broken by the intruder. AES Technique has been widely used in a variety of applications such as secure communication systems and high throughput data servers.

The AES encryption algorithm is a block cipher that uses an encryption key and a several rounds of encryption. A cipher key is an encryption algorithm that works on a single block of data at a time. In the case of standard encryption technique the data is 128 bits, or 16 bytes, in length. The term "rounds" refers to the way in which the encryption algorithm mixes the data re-encrypting it ten to fourteen times depending on the length of the key.

AES encryption uses a single key as a part of the encryption process. The key can be 128 bits (16 bytes), 192 bits (24 bytes), or 256 bits (32 bytes) in length. The term 128-bit encryption refers to the use of a 128-bit encryption key. With AES both the encryption and the decryption are performed using the same key. This is called a symmetric encryption algorithm. Encryption algorithm uses two different keys that is public and a private key. Both are called asymmetric encryption algorithm key technique. An encryption key is simply a binary string of data used in the encryption process. Because the same encryption key is used to encrypt and decrypt data, it is important to keep the encryption key as a secret and to use the keys that are hard to guess. Some keys are generated by software used for this specific task. Another method is to derive a key from a pass phrase. Good encryption systems never use a pass phrase alone as an encryption key.

The previous techniques used in the encryption are parallel mix column and one term one process. The parallel mix column occupies more area and delay. The one term process also occupies more area and delay. So the complex parallelism is introduced.. By using this technique , a higher energy efficiency is achieved and also delay reduction is possible. This technique is applied for so many applications like military purpose, computer password and so on.

The reminder of this paper is organized as follows: section 2 explains the basic types of encryption. The encryption types involve the brief explanation about four techniques which we have given in the abstract. Section 3 presents the complex parallelism. The section also explains the cyclic loop of this mechanism. Section 4 discuss the simulation results of one term one process, parallel mix column and Complex parallelism.

II. Encryption Techniques

AES is a symmetric encryption algorithm, and it takes a 128-bit data as a input and performs several rounds of transformations to generate output cipher text. It is a computer security standard issued by NIST for protecting the electronic data. The basic processing unit used in this AES algorithm is byte. AES is used to encrypt/decrypt data blocks of 128-bits and it can be implemented in both hardware and software. AES acts as a block cipher which operates on fixed length group of bits of data. AES is a stream cipher which means the plain text bits are encrypted one and set of transformations have been applied to the bits. It may vary during encryption process. The plain text input and cipher output are the blocks of 128 bits. The number of rounds depend on key size. Each 128-bit is processed in a permutation and rotation operation. There are different techniques involved in this encryption.

2.1 Substitution Byte*:*

It is a non- linear substitution byte. Each Byte is replaced by another byte. This substitution Byte uses S-BOX for generating the cipher text. This S-box involves two process. First one is used to take the multiplicative inverse of finite field of the matrix (i.e input data). Secondly, the Affine Transformation is applied to the output of multiplicative inverse. Area reduction is possible in this finite field and finite field is used to create a compact field AES implementation. In new technology, the S-Box can be obtained from its truth table by using two level logic such as sum of products and product of sum. If the above mentioned technology is used , the primitive logic cells can be reduced and also cell size can be optimized using synthesis tool. The S- Box is computed from inverse of input to the original input. The example of Affine Transformation is given by

$$\begin{bmatrix} z1 \\ z2 \\ z3 \\ z4 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 & 0 \\ 0 & 1 & 1 & 1 \\ 1 & 0 & 0 & 1 \\ 1 & 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} s1 \\ s2 \\ s3 \\ s4 \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \\ 1 \\ 0 \end{bmatrix}$$

Consider an example, 4X4 matrix is a input text and [s1 s2 s3 s4] is the inverse of the input . the remaining one [0 1 1 0] is a cipher key. The output is a [z1 z2 z3 z4]. The input is multiplied with inverse of input with a cipher key and the output is obtained. The example of Substitution Byte is given below.

a	b	c	d
e	f	g	h
i	j	k	l
m	n	o	p

(a)

a	b	c	d
e	f	s	h
i	j	k	l
m	n	o	p

(b)

Fig 1 (a). Representation of sample matrix and (b). Operation of matrix in substitution byte

2.2 Shift Row:

The technique used in this model is the transformation of the row. Consider a 4x4 matrix, the first row of the matrix remains unchanged. The second row , first bit is shifted to the last one. Then the last one is shifted to the third place. Finally the third row and forth row is finally rotated. The message is shuffled. In otherwords, The row transformation can be expressed as a reconstruction of the matrix using an key expression for each element. The row expressions calculate circular transformation .The example of shift row is given below.

a	b	c	d
e	f	g	h
i	j	k	l
m	n	o	p

(a)

a	b	c	d
f	g	h	e
k	l	i	j
p	m	n	o

(b)

Fig 2 (a) Representation of sample matrix and (b) Operation of matrix in shift row

The figure 2 represents the operation of shift row. The second row "e" is shifted to the last column. Then the shift is repeated upto n times.

2.3 Mix Column:

During this process, the matrix of the input column is shuffled. From that, the message is unbroken. It is similar to Substitution Byte. It uses the polynomial function. It is also based on finite field multiplication. The Mix column is based on the multiplication of two matrices and xor operation of both input and cipher key.

a	b	c	d
e	f	g	h
i	j	k	l
m	n	o	p

(a)

c	b	a	d
g	f	e	h
k	j	i	l
o	n	m	p

(b)

Fig 3 (a) Representation of sample matrix and (b) Operation of matrix in mix column

The figure 3 represents the operation of shift row. The first and third column are exchanged in the matrix. This is the operation of mix column.

2.4 Add Round Key:

The sender sends a message to the receiver using a password (i.e key). The key is known by both sender and receiver. The key is added to the input (which is in the form of cipher text). The message is not hackable by any other intruders and also the information is more shuffled and secure.

2.5 Subsitution Byte with Key:

This operation produce an output word by replacing each byte in the input to another byte according to the Replacement Byte.

2.6 Rotate the input with Key:

This function takes [z3,z2,z1,z0] as a input and performs a rotation and returns the word [z2,z1,z0,z3] as a output.

2.7 Xor Operation with Key:

It performs simply xor operation with input . The message is much more shuffled and more secure.

III. Analysis of System Techniques

3.1 One Term One Process:

The input is fed to the add round key. so the key is mixed with input (i.e cipher text). Then the output of the add round key is shuffled with sub byte, shift row, mix column and add round key. This process is repeated upto nine times. Then the ouput is processed with key elongation process. The output of key

elongation is send to the final stage add round key. Finally the cipher text is generated from the plain text by using this OTOP technique.

3.2 Parallel Mix Columns:

The OTOP model is easily hackable by intruder. So the efficiency of OTOP model is small. This process is similar to the OTOP model. The input is fed to the add round key (i.e cipher text). The output is fed to the sub byte and shift row. The output of the shift row is added to the parallelizing mix column for shuffling the message. Then the output is added to the add round key. The process is repeated for nine times. The key elongation process is applied to the final stage output. The efficiency of parallel mix column is much higher than OTOP model. The area reduction is possible in this parallel mix column.

3.3 Complex Parallelism:

The input is fed to the four main blocks that is replacement bye, row transformation, shuffle the column and xor operation with key. The process is simulated upto nine times. The process is optimized with complex parallelism and the message is secure with cipher keys.

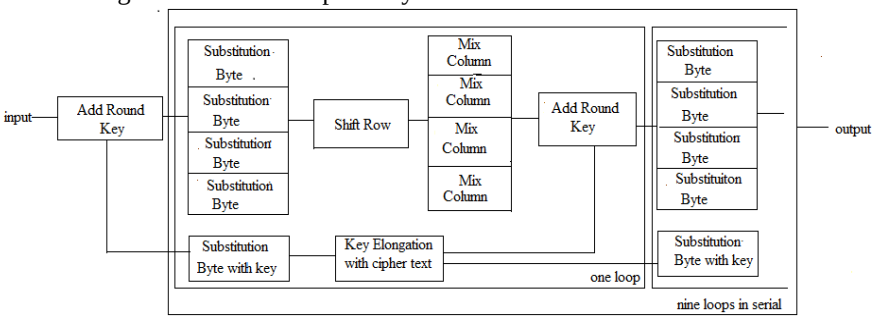

Fig 4 Complex Parallelism

First the input is fed to the xor operation with key. The process involves in this stage is inserting a key to the input data. Then we have to send the data to replacement byte. Parallelizing the replacement byte is used to secure the message. The message is much more shuffled by combining the replacement byte. Then the next one is row transformation. This is used to transfer or shift the data. Then the next step is shuffle the column. It is used to shuffle the input with key. this is done by polynomial function. Then the last one is xor operation with key. The input is xored with key. The process is repeated upto nine times for shuffling the message. Finally the original text is covered by cipher key and the output of the data is cipher text(only with cipher keys). The cipher text information is unbroken by any other intruder. Thus The information is secured by using complex parallelism.

IV. Results and Discussions

The information is encrypted by using complex parallelism. The simulation results of OTOP model and Parallel Mix Column are discussed below. Finally the encrypted output of complex parallelism is also given below.

4.1 One Term One Process:

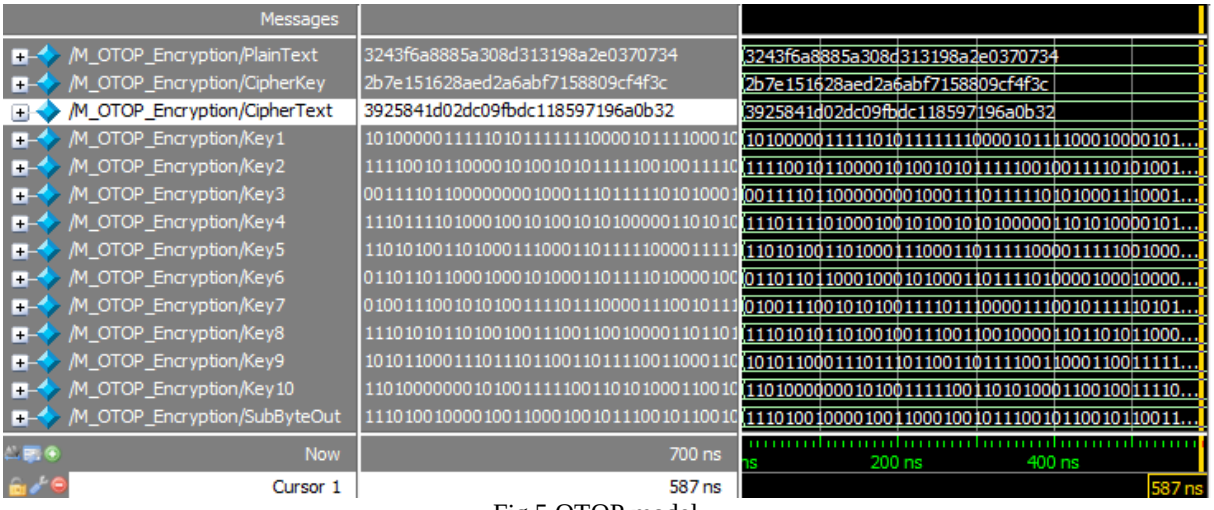

Fig 5 OTOP model

The figure 5 shows the simulation of OTOP model. The input is a 128-bit. The plain text is given to the OTOP encryption key. The cipher text is generated by using cipher keys. The OTOP model involves the process of SubBytes, Shift Row, Mix Column and Add Round key. All the above process is used to perform the message shuffling purpose. The permutation and rotation process are done by using the key elongation process. The message is secure and the information is shuffled for security purposes. The number of LUTs are reduced by 0.8%. Then the number of occupied slices are decreased by 0.9%. The gate count is increased in this OTOP model.

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of 4 input LUTs	21,647	26,624	81%
Logic Distribution			
Number of occupied Slices	11,423	13,312	85%
Number of Slices containing only related logic	11,423	11,423	100%
Number of Slices containing unrelated logic	0	11,423	0%
Total Number of 4 input LUTs	21,658	26,624	81%
Number used as logic	21,647		
Number used as a route-thru	11		
Number of bonded IOBs	384	487	78%
Total equivalent gate count for design	131,919		
Additional JTAG gate count for IOBs	18,432		

Fig 6: Compilation of OTOP model

The Figure 6 show the compilation of OTOP model. The area utilization is 81% in this OTOP model. The delay is calculated in the comparison table for area efficiency.

4.2 Parallel Mix Column:

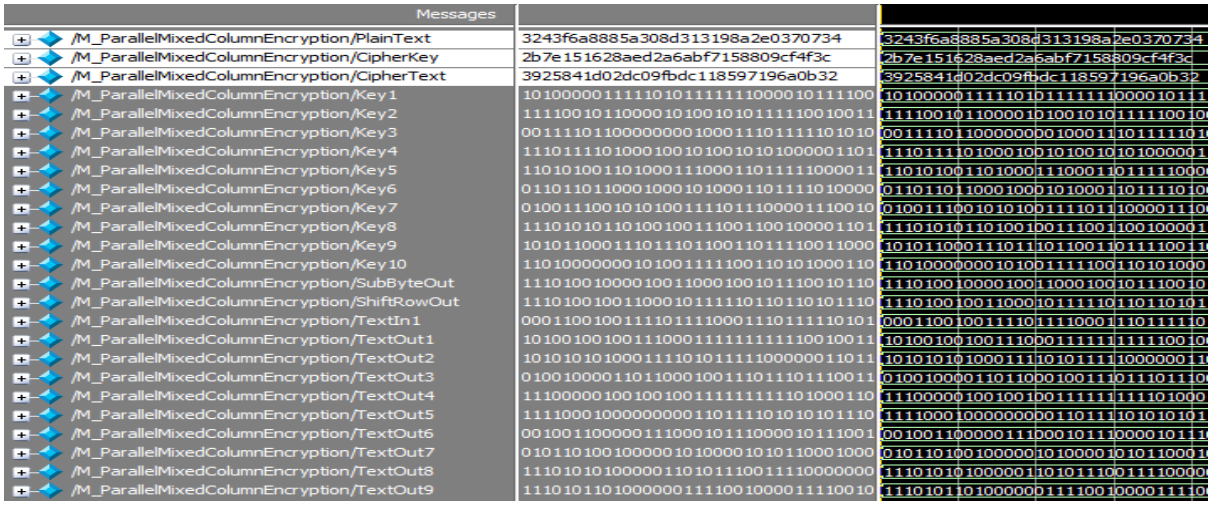

Fig 7 Parallel Mix Column

The figure 7 shows the simulation of Parallel Mix Column model. The input is a 128-bit. The plain text is given to the Parallel Mix Column encryption key. The cipher text is generated by using cipher keys. The Parallel Mix Column model involves the process of SubBytes, Shift Row, Mix Column and Add Round key. All the above process is used to perform the cyclic rotation for rotating the input keys . The key elongation process is done by using key rotation. The message is safe and the information is shuffled for security purposes. The number of LUTs are reduced by 0.9%. Then the number of occupied slices are decreased by 0.9%. The gate count is increased in this Parallel Mix Column model.

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of 4 input LUTs	21,647	22,528	96%
Logic Distribution			
Number of occupied Slices	11,262	11,264	99%
Number of Slices containing only related logic	11,096	11,262	98%
Number of Slices containing unrelated logic	166	11,262	1%
Total Number of 4 input LUTs	21,658	22,528	96%
Number used as logic	21,647		
Number used as a route-thru	11		
Number of bonded IOBs	384	502	76%
Total equivalent gate count for design	131,919		
Additional JTAG gate count for IOBs	18,432		

Fig 8 Compilation of Parallel Mix Column

The figure 8 shows the compilation of Mix Column. The area utilization is 96% in this Parallel Mix Column. The path route delay is calculated

4.3 Complex Parallelism:

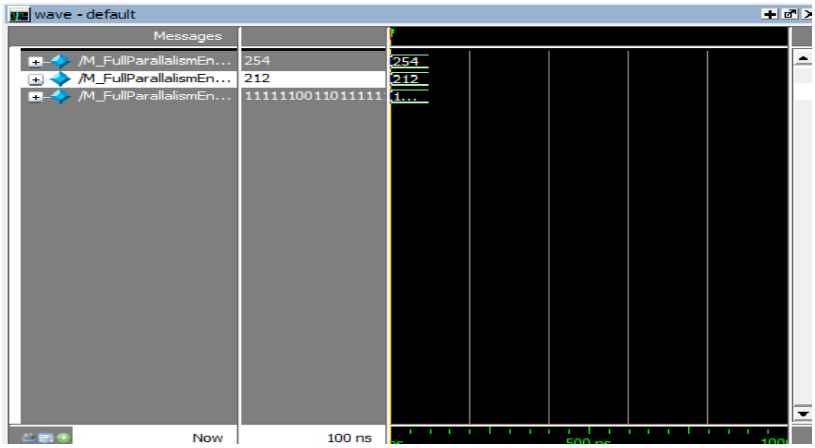

Fig 9: Complex Parallelism

The figure 8 shows the proces of complex parallelism encryption. It will show the complex parallelism process. The process involves the operation of one task one processor, Parallel Mix columns and complex parallelism. It implements in 167 processor using complex parallelism technique. The process is the combination of various techniques like Substitution Byte, Shift Row Mix Column and Add Round Key. The message is secure and the delay is reduced by other methods. The figure 10 shows the compilation of complex parallelism. The delay of complex parallelism is small compared to other techniques.

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of 4 input LUTs	21,629	22,528	96%
Logic Distribution			
Number of occupied Slices	11,262	11,264	99%
Number of Slices containing only related logic	11,140	11,262	98%
Number of Slices containing unrelated logic	122	11,262	1%
Total Number of 4 input LUTs	21,634	22,528	96%
Number used as logic	21,629		
Number used as a route-thru	5		
Number of bonded IOBs	384	502	76%
Total equivalent gate count for design	131,778		
Additional JTAG gate count for IOBs	18,432		

Fig 10 Compilation of Complex Parallelism

The above simulation results discuss the detailed description of three models. The comparison table of area and delay are discussed in the below section. The table 1 discusses the comparison of area with LUTs and Gate count. The table 2 discusses the comparison of delay with path and route delay.

TABLE 1: Comparison of Area

Encryption Name	LUT	Gate Count
OTOP model	21647	131919
Parallel Mix Column	21647	131919
Complex Parallelism	21629	131778

The OTOP model occupies more LUT in the hardware implementation. The number of gates in the OTOP model is very high .The parallel mix column occupies less LUT compare to OTOP model and high compare to complex parallelism. The number of gates occupied in the hardware is same as the OTOP model. The complex parallelism technique occupies less LUTs for hardware implementation. The number of gates in the complex parallelism are less compared to the both previous model. The path delay and route delay is efficient in the complex parallelism compared to the OTOP model and Parallel Mix Column.

TABLE 2: Comparison of Delay

Encryption Name	Delay	Gate Delay	Path Delay
OTOP model	307.909ns	105.862ns	202.047ns
Parallel Mix Column	232.742ns	116.830ns	115.912ns
Complex Parallelism	232.245ns	116.683ns	115.562ns

V. Conclusion

In this brief, cryptography AES technique is presented to protect the information. To increase the efficiency, the complex parallelism technique is used to involve the processing of Substitution Byte, Shift Row, Mix Column and Add Round Key. Using complex parallelism, the original text is converted into cipher text. From that, we have achieved a 96% energy efficiency in Complex Parallelism Encryption technique and recovering the delay 232 ns. The complex parallelism that merge with parallel mix column and the one task one processor techniques are used. In future, Complex Parallelism Decryption technique is used for recovering the original message.

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