IOSR Journal of Computer Engineering (IOSR-JCE)
e-ISSN: 2278-0661, p- ISSN: 2278-8727Volume 16, Issue 1, Ver. VII (Feb. 2014), PP 91-98
www.iosrjournals.org

Charge Pump Phase Locked Loop Synchronization Technique in Grid Connected Solar Photovoltaic Systems

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Abstract : *In this paper, an attempt to design and simulate charge pump phase locked loop method of synchronization in grid connected solar photovoltaic system has been made. Delivery of power with high quality to the grid is of concern in grid connected systems and to ensure the same auto synchronization technique is required. Such a method is proposed and analyzed using MatLab-Simulink and its performance is verified for compliance with IEEE 929 standard prescribed for inverter fed grid systems and IEC 61727 / IEEE 1547 standard for harmonic limitation of grid connected inverters.*

Keywords: *Charge Pump Phase locked loop, IEC 61727, IEEE 929, IEEE 1547, MatLab, Solar photovoltaic array, Synchronization*

I. INTRODUCTION

Increasing demand in power sector has resulted in need for renewable energy sources. Solar power generation has several advantages mentioned in literature [1] and hence synchronization of the solar photovoltaic (SPV) system output to the grid is mandatory. Several issues pertaining to grid connected inverters have been discussed [2] and resolution of these issues is mandatory for proper functioning of grid integrated system.

The challenges in synchronization involves magnitude, frequency and phase angle of the voltage at the point of common coupling (PCC) and these parameters produced from the SPV system has to be matched. In this paper the charge pump phase locked loop (CP-PLL) method has been used to meet the above mentioned requirements.

Design and working principle of CP-PLL technique is discussed in detail in literature [3]. Auto synchronization technique is the process of following the phase angle and frequency of the grid voltage after synchronization [4]. Auto synchronization is often challenged with harmonics, system disturbance and load variations. The limits beyond which the grid interactive inverters would be islanded are mentioned in IEEE 929 standard. Harmonic limits for 10 kW and 30 kW systems are specified in IEC 61727 and IEEE 1547 standard respectively [5], [6].

In this paper, CP-PLL technique has been tested subject to various scenarios that are likely to occur in a grid. The response of this technique is compared with limits mentioned in standard. The compliance of the results with IEEE 929, IEC 61727 and IEEE 1547 standards are also presented.

II. DESCRIPTION OF THE PROPOSED SYSTEM

The proposed CP-PLL synchronization technique for grid connected SPV system is illustrated in Fig. 1. The application of CP-PLL control technique is used here to address the issues discussed in the previous section failing which the power quality and synchronization would be affected. The inverter pulse firing pattern is adjusted based on the grid reference and this modification is implemented using CP-PLL which is described in Fig. 1. The SPV system feeds the grid with a control technique to maintain synchronization. Inverter firing is based on the comparison of modulating signal and carrier signal [7]. The pulse width modulation (PWM) depends on the modulating signal quality. The PCC voltage is taken as reference and the PWM pulses are generated based on modulating signal using CP-PLL technique. The schematic diagram of the proposed CP-PLL is described using Fig. 2. A balanced three phase symmetrical voltage is assumed in CP-PLL design technique [6].

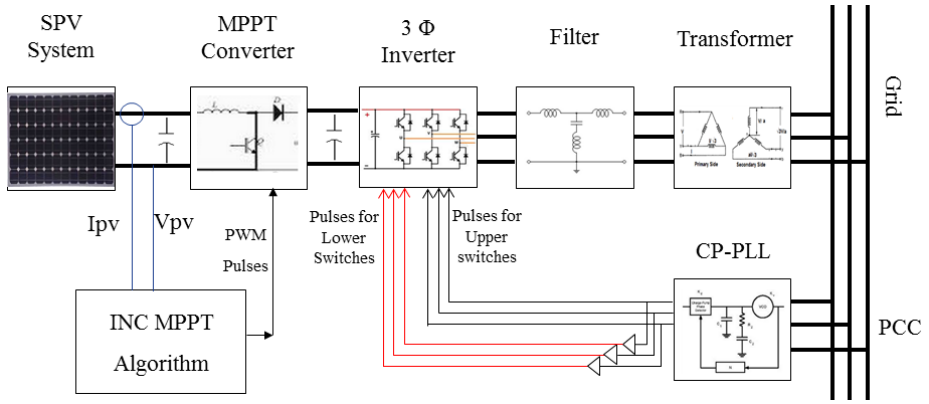

Fig. 1. Schematic representation of the proposed system

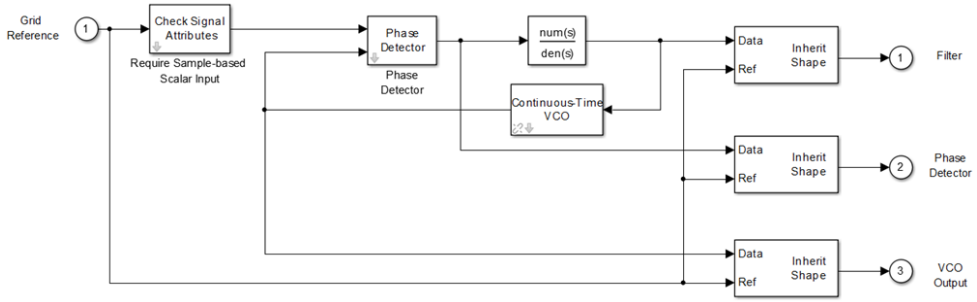

Fig. 2. MatLab implementation of CP-PLL

The simulation parameters of the system design and sizing are listed in Table 1. MatLab Simulink model of CP-PLL method is shown in Fig. 3

Table 1. Simulation Parameters for the proposed system

Parameters	**Values**
Grid voltage	415 V
Single PV panel voltage	16.54 V
Single PV panel current	2.25 A
No. of cells in single PV panel	36 in series
PV Array size	14x2 (14 panels in series and 2 panels in parallel)
PV array voltage	230 V
PV array current	4.5 A

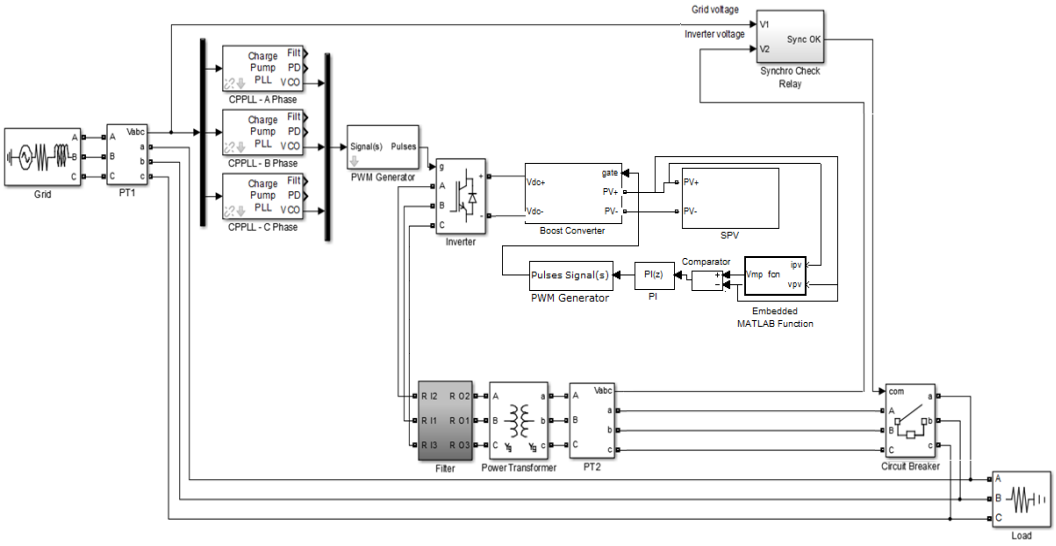

Fig. 3. MatLab-Simulink model of the system shown in Fig 1

Maximum power point (MPP) tracking algorithm is used to track the maximum power point voltage. In this work incremental conductance (INC) MPP algorithm is used by considering its simplicity and ability to

track global maximum power point [8]. The flowchart for INC MPP algorithm is shown in Fig. 4. The algorithm is coded in MatLab Embedded function tool and interfaced with the converter. The simulated results for INC MPP algorithm is shown in Fig. 5. It is observed that the MPP algorithm always tracks the MPP voltage which is around the required 230 V for all insolation levels. Here, boost converter is used as MPP tracker and is designed for continuous conduction mode (CCM) of operation using the equations given in literature [7]. The output from MPP tracker is fed to the inverter via DC link capacitor. The output of the inverter is then connected to a transformer through a proper filter.

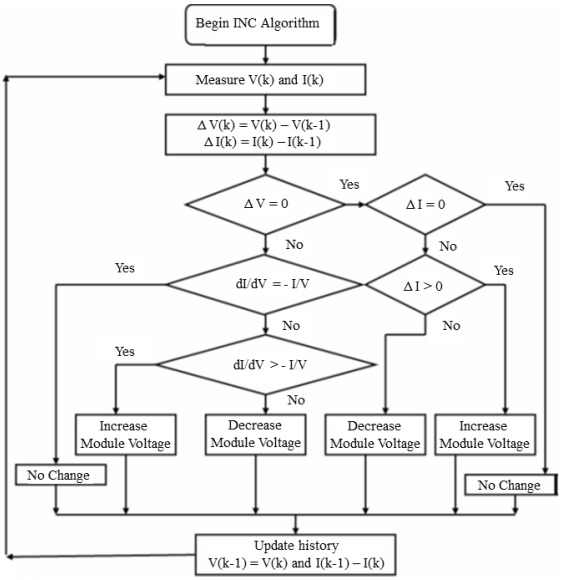

Fig. 4. Flowchart for INC MPPT algorithm

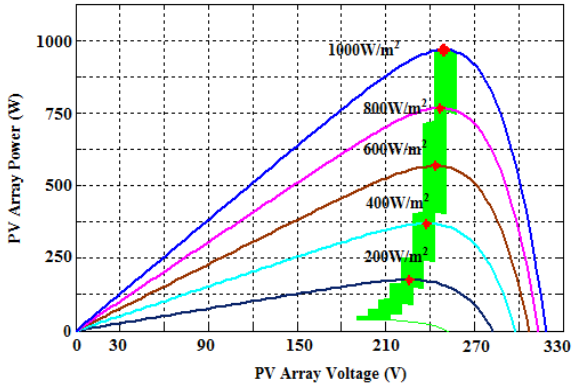

Fig. 5. Tracking characteristics of INC MPPT algorithm

Solar power conditioning unit (PCU) is an integrated system comprising of a SPV system, inverter and filter. The PCU voltage should be greater than the system voltage in order to supply active power according to ANSI C84.1 and hence a transformer with on load tap changer (OLTC) option is accommodated. The standards for grid connected SPV system is summarized in Table 2. To verify the synchronization condition a relay complied with ANSI 25 is used.

Table 2. Synchronization standards for SPV inverter fed grid systems

Parameters	**Standards**
Voltage Magnitude	ANSI C84.1
Frequency	IEEE 929
Phase Angle	IEEE 929
Synchronization	ANSI 25
Current Harmonics	IEC 61727 / IEEE 1547

III. RESPONSE OF THE SYSTEM FOR GRID DISTURBANCE

The most common scenarios in power system during a disturbance have been simulated and the response of CP-PLL is recorded and verified in this section. Response of the system during the presence of harmonics is also tested with FFT tool at every stage. Harmonic distortion of more than 1000% in the voltage

was introduced at the PCC in the system shown in Fig.6. THD was observed to be extremely high and is displayed as infinity. Further to identify the harmonic suppression capability of this technique, the harmonics at the PCC was reduced considerably to 99.33% (with only 2nd, 3rd and 4th order harmonics) (Fig. 7). The harmonics of the output spectrum had a THD of 82.32% (Fig. 9). The results do not comply to IEC 61727 and IEEE 1547 standard (Fig. 6 to Fig. 9) as the tolerance limit as per standard is 5% THD.

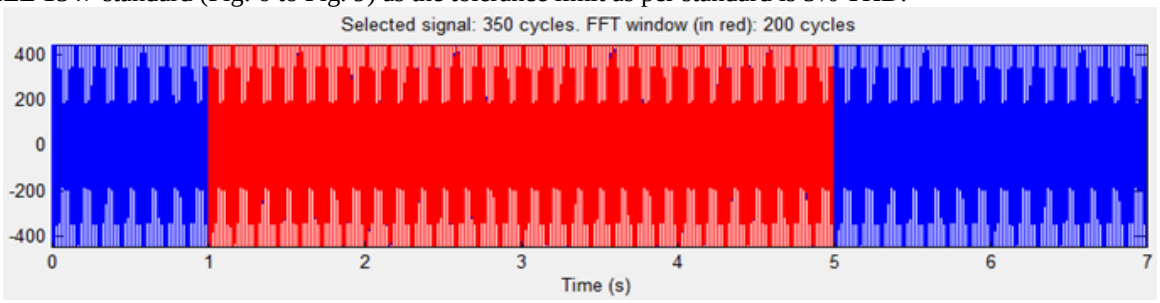

Fig. 6. Voltage spectrum at PCC

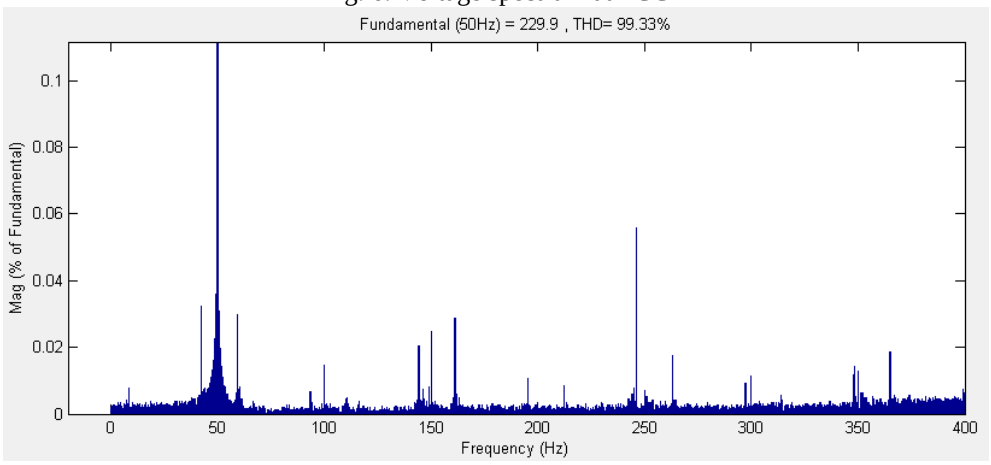

Fig. 7. THD of voltage at PCC

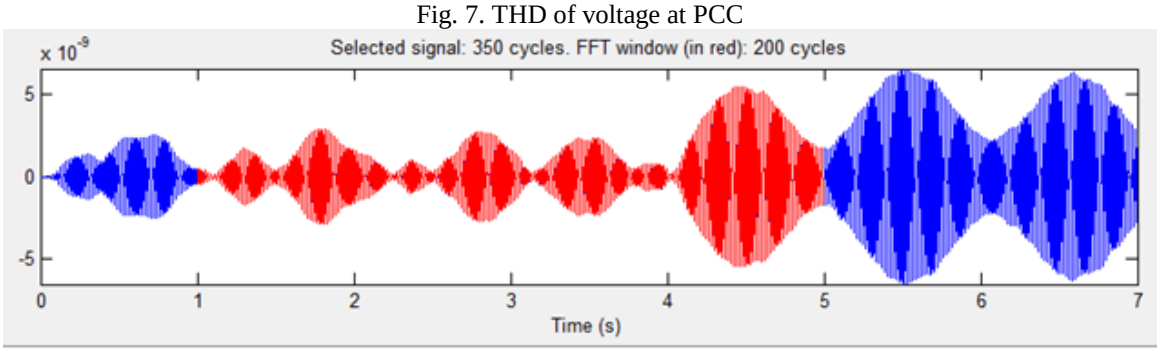

Fig. 8. Current spectrum at PCU in CP-PLL technique

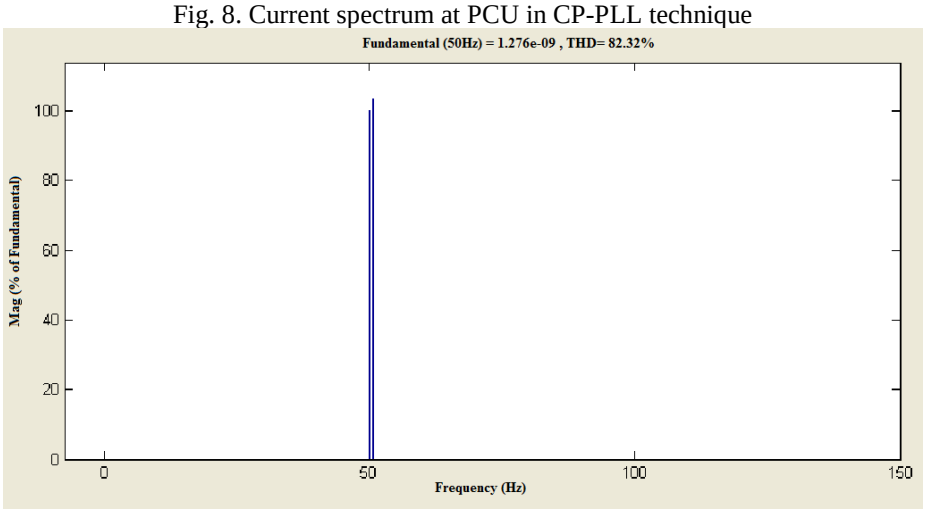

Fig. 9. THD measured at PCU in CP-PLL technique

Table 3. Current harmonics distortion of CP-PLL method for different cases

Different cases under study	**Injected harmonics (%)**	***Permissible limit as per IEC 61727 / IEEE 1547 Standards is < 5%***
		% THD from CP-PLL
Practical	5	81.33
Measurable	99.33	82.32
Worst Case	1065.4	Extremely High

Fig. 10 shows the output voltage spectrum of PCU and PCC. The difference between these two voltages is adjusted by the CP-PLL till the PCU is in phase with the PCC. This can be observed when the PD becomes almost zero after a moment. A sudden variation in frequency is made at PCC to verify the response of CP-PLL and it was found that the PCU is following the PCC after the disturbance. Fig. 11 shows how the PD has increased during the disturbance and then gets settled within a short duration. This is compiled to IEEE 929 standard where the difference in phase is permitted before a grid islanding.

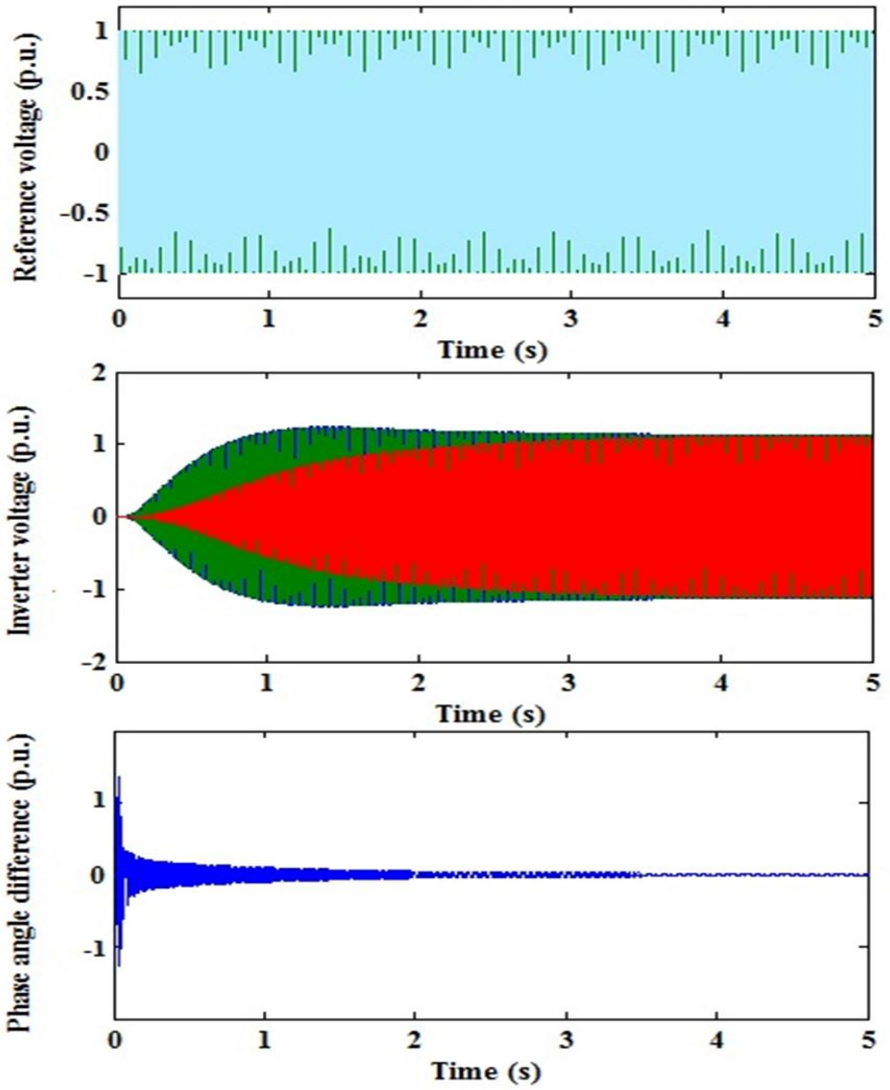

Fig. 10. CP-PLL output displaying the suppression of phase difference between grid and inverter voltage under normal frequency conditions

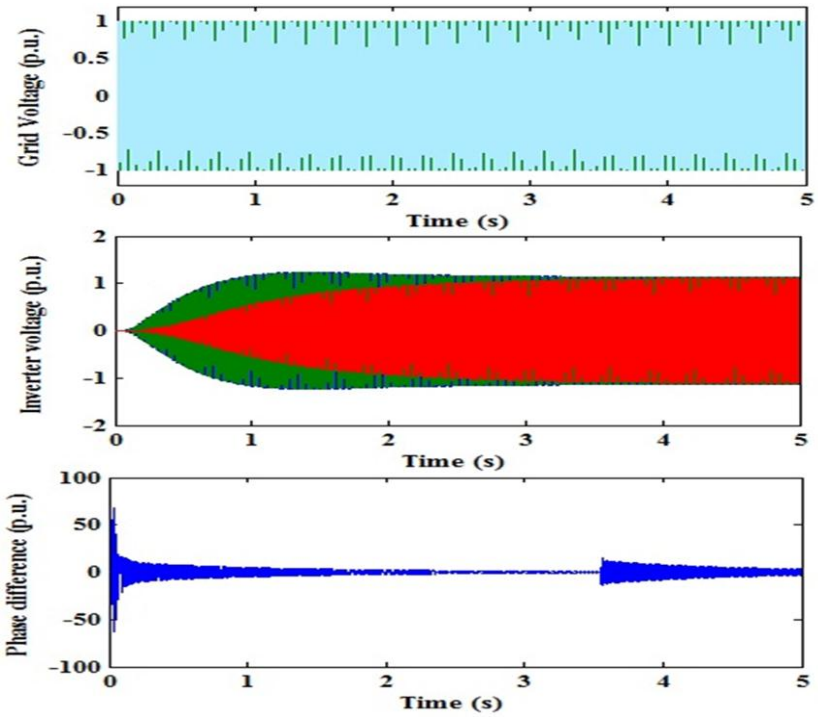

Fig. 11. CP-PLL output displaying the suppression of phase difference between grid and inverter voltage under disturbance conditions

IV. RESULTS AND DISCUSSIONS

Power system disturbances are usually followed by load throw, dc transients and harmonics. CP-PLL method has failed for harmonic conditions as explained in Section 3. Phase angle mismatch between PCC and PCU is addressed in CP-PLL technique. Phase angle difference can be due to load variations or harmonics and CP-PLL cannot distinguish between these two conditions. This overthrows the advantages of CP-PLL since the system goes out of synchronization violating IEEE 929 standard.

V. CONCLUSION

In this paper, a detailed analysis of the harmonic issues in grid synchronization techniques has been discussed. The modulating signal for inverter is taken from the PCC. The presence of harmonics in the grid affects the quality of the inverter output. The ability of CP-PLL technique to address this issue has been tested and the results are not complied with the guidelines given in the standards. CP-PLL method cannot distinguish between phase angle variations due to harmonics and load variation, as load variations are often followed by harmonics. Due to this fact it cannot be used for grid synchronization.

VI. AUTHORS BIOGRAPHY

K N Dinesh Babu received his B.E. in Electrical & Electronics Engineering from SSN College of Engineering, Chennai, Tamilnadu in 2004. He is currently pursuing Ph.D. Degree in University of Petroleum & Energy Studies in the area of grid connected solar photovoltaic system. He has 9 years of industrial experience and is currently working for GE Energy as a Lead Application Engineer for Protection & control in Power system division. He has worked for ALSTOM and ABB as Testing & Commissioning Engineer and was responsible for Testing and Commissioning of Protection Equipment including Substation Automation System.

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