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Silicon Heterostructures as High Performance Field Effect Transistor

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Abstract : *The advances in Silicon technology have driven the MOSFET device fabrication towards submicron regime. Despite all these advances in technology special effects come into play such as velocity overshoot, short channel effects and Drain Induced Barrier Lowering (DIBL). For MOSFET with large geometry, they experience a number of effects ranging from low clock frequencies due to high input capacitance, high threshold voltage hence high power consumption and lower trans-conductance. As the dimensions are scaled down, the drain current increases, evidence that sub-micron devices have better performance as compared to un-scaled devices. It can also be noted that there is a strong correlation between device dimensions and device performance. Also from transfer curves the output drain current decreases with increase in the drain voltage but it was further established from the transfer curves that the trans-conductance of the device increases with scaling at a constant voltage. This shows that sub-micron device has better performance as compared to un-scaled device.*

Keywords: *MOSFET, short channel effects, velocity overshoot, DIBL, silicon.*

I. Introduction

A field – effect transistor is a voltage controlled variable resistor. Unlike bipolar transistor, the field effect (unipolar) transistor operates on electric conduction carried by majority carriers. For the structure of a double diffused Field Effect transistor the middle P region serves as a conductive channel [1]. Two ohmic contacts are made to the channel, one acting as a source to supply carriers and the other as the drain to collect carriers. Voltage V_D is applied between source and drain. For drain made of P- type semiconductor, the drain is negatively biased with respect to the source [2]. MOSFET scalling is fundamental in improving its performance by enhancing its frequency and lowering power consumption [3]**.**

II. Theory and Equations

Considering regions AB as shown in diagram below, the action of resistance modulation takes place and represents the field effect transistor by an idealized structure.

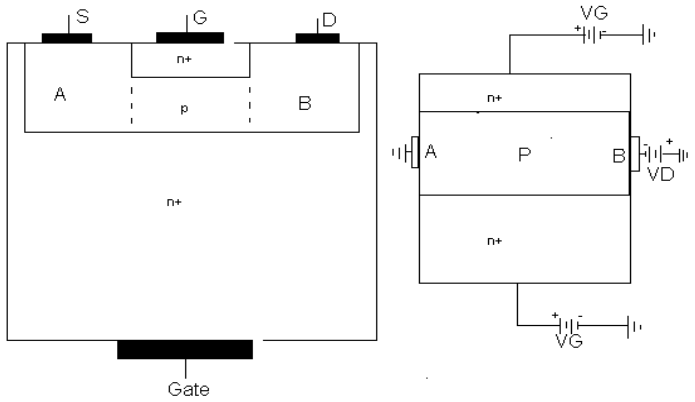

Figure 1. 1 Diagrams showing the representation of field effect transistor by an idealized structure

The middle P region that forms a conductive channel is only moderately doped as compared to the two n regions; therefore, the depletion (space charge) region extends almost entirely into the channel. As V_G or V_D or both are increased, depletion region widens, reducing the channel width. The progressive change in effective width of the channel is as shown below [4].

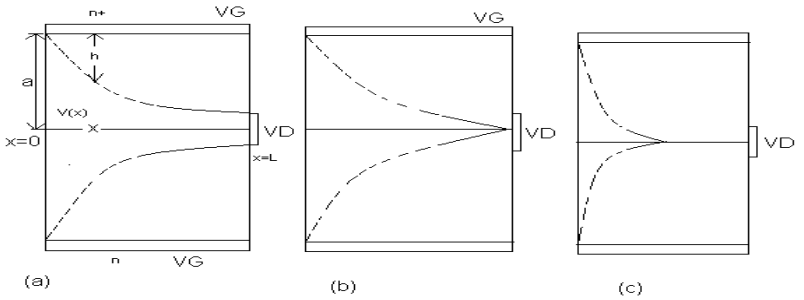

Figure 1. 2 The progressive change in effective width of the channel with V_G.

The diagrams of figure 2.2 show effect of the gate voltage V_G on the width of the conduction channel for V_{G1}, V_{G2} and V_{G3} where $V_{G1}<V_{G2}<V_{G3}$. The conduction channel is bounded by the dashed lines. The channel is pinched off at the drain and the pinch-off point is moved toward the source end as V_G is progressively increased.

Assuming uniform doping concentration N_a in the P region, let – $V(x)$ be voltage at a point X in the channel. The depletion depth h is given by [5]

$$h(x)=\left(\frac{2\in}{eN_a}\right)^{\frac{1}{2}}\left[V_d+V_G+V(x)\right]^{\frac{1}{2}} \qquad 1$$

V_d is the diffusion (or built in) voltage

V_G being positive and V_D being negative with respect to the source.

The width of conductive channel is $2(a-h)$ and the hole concentration in P – region is N_a. Thus current through the channel is $I_D = e\mu_P N_a E_X Z[2a-2h(x)]$ 2

Where Ż is the lateral dimension of the transistor structure. Realizing that $E_x = -\frac{d}{dx}\left[-V(x)\right]$ then,

$$\int_{x=0}^{L} I_D dx = \int_{0}^{VD} 2e\mu_p N_a Z[a-h(x)]dV \qquad 3$$

Substituting (1) into (3) then,

$$\int_{x=0}^{L} I_D dx = \int_{0}^{V_D}\{2e\mu_p N_a Z[a-\left(\frac{2\in}{eN_a}\right)^{\frac{1}{2}}(V_d+V_G+V_D)^{\frac{1}{2}}\}dV$$

$$I_D L = 2e\mu_P N_a Z\int_0^{V_D}\left\{a-\left(\frac{2\in}{eN_a}\right)^{\frac{1}{2}}\left[V_d+V_G+V_D\right]^{\frac{1}{2}}\right\}dV$$

$$I_D = \frac{2e\mu_p N_a Z}{L}\int_0^{V_D}\left\{a-\left(\frac{2\in}{eN_a}\right)^{\frac{1}{2}}\left[V_d+V_G+V_D\right]^{\frac{1}{2}}\right\}dV$$

$$= \frac{2e\mu_p N_a Za}{L}\left\{V_D-\left(\frac{2\in}{eN_a}\right)^{\frac{1}{2}}\cdot\frac{2}{3a}\left[\left(V_d+V_G+V_D\right)^{\frac{3}{2}}-\left(V_d+V_G\right)^{\frac{3}{2}}\right]\right\}$$

$$= G_m \left\{ V_D - \left(\frac{2 \in}{eN_a} \right)^{\frac{1}{2}} \cdot \frac{2}{3a} \left[\left(V_d + V_G + V_D \right)^{\frac{3}{2}} - \left(V_d + V_G \right)^{\frac{3}{2}} \right] \right\} \quad 4$$

where $G_m = 2e\mu_P N_a a \frac{Z}{L}$

Equation (4) holds as long as $h(x) < a$ for $0 < x < L$ Pinch – off voltage $V_p^{'}$ is defined such that when $V_G = V_p^{'}$ at x = 0, the value of h (0) = a in equation (1), thus;

$$h(x) = \left(\frac{2 \in}{eN_a} \right)^{\frac{1}{2}} \left\| V_d + V_G + V_{(x)} \right\|^{\frac{1}{2}}$$

When $V_G = V_p^{'}$ at $x = 0$, the value of $h(0) = a$

$$a = \left(\frac{2 \in}{eN_a} \right)^{\frac{1}{2}} \left[V_d + V_p^{'} + 0 \right]^{\frac{1}{2}} \qquad a^2 = \frac{2 \in}{eN_a} \left[V_d + V_p^{'} \right]$$

$$e \frac{1}{2 \in} N_a a^2 - V_d = V_p^{'} \qquad V_p^{'} = V_p - V_d$$

$$V_p^{'} = \frac{eN_a}{2 \in} a^2 - V_d = V_p - V_d \quad 5$$

Figure 2.2 corresponds to pinch – off at the drain with $V_G + V_D = V_p^{'}$. In terms of $V_p^{'}$, equation (5) becomes $V_p^{'} + V_d = \frac{eN_a}{2 \in} a^2$ and substituting in equation (4)

$$I_D = G_m \left\{ V_D - \frac{2}{3\left(V_p^{'} + V_d \right)^{\frac{1}{2}}} \left[\left(V_d + V_G + V_D \right)^{\frac{3}{2}} - \left(V_d + V_G \right)^{\frac{3}{2}} \right] \right\} \quad 6$$

Figure 1.2 shows $I_D - V_D$ characteristics

The numbers for I_D, V_G and V_D shows their magnitudes in typical field – effect transistor.

For low V_D, expansion of $\left(V_d + V_G + V_D \right)^{\frac{3}{2}}$ term in (6) gives (Fariborz,1993)

$$I_D = G_m \left[1 - \left(\frac{V_d + V_G}{V_d + V_p^{'}} \right)^{\frac{1}{2}} \right] V_D \quad 7$$

In this region I_D increases linearly with V_D. At $V_D = V_P^{'} - V_G$, the current I_D becomes saturated. Values of V_D and I_D at this point are denoted by V_{DS} and I_{DS}. Differentiating I_D with respect to V_D, it's found out that;

$$g_D = \frac{\partial I_D}{\partial V_D} = G_m \left[1 - \left(\frac{V_d + V_G + V_D}{V_d + V^1{}_p} \right)^{\frac{1}{2}} \right] \quad 8$$

But g_D becomes zero when $V_D = V_P^{'} - V_G$ i.e. the current remains constant at V_{DS} for any incremental change in V_D. The quantity g_D is called drain conductance.

The trans-conductance is further defined as

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{-G_m}{\left(V_d + V_P^{'}\right)^{\frac{1}{2}}}\left[\left(V_d + V_G + V_D\right)^{\frac{1}{2}} - \left(V_d + V_G\right)^{\frac{1}{2}}\right] \quad 9$$

In terms of g_D and g_m, the a.c. component of the drain is

$$I_D = g_m V_G + g_D V_D \quad 10$$

Where V_G and V_D is a.c. gate and drain voltages.

III. Modeling And Simulation

This study was conducted through device simulation. It was concerned with investigating the effect of scaling MOSFET gate dimensions on the performance of the device. It is specifically intended to investigate the relationship between saturation drain current against saturation drain voltage at different scaling factors. Such issues are best investigated through simulation method. This method enables the researcher to manipulate the gate dimensions and study/observe the resulting effects. This simulation research design entails, inputting the parameters required, systematic manipulation of some characteristics and examination of the outcome. All simulations were done using MATHCAD software. NMOSFET with gate lengths 100Å, 65Å, 42.25Å, 27.27Å and 17.85 Å, gate widths 100Å and with oxide thickness of 2Å were studied. A gate length of 100 Å was chosen as a very large device and has been scaled by a factor of k, k^2, k^3, k^4 where k=0.65. The results obtained were then used to plot the graphs using ORIGIN lab software at. The transfer curves were then obtained at different drain voltages of 1-5V.

Assuming doping concentration N_a in the P substrate region, the gate voltage (V_G), drain voltage (V_D), built in voltage (V_d), gate length (L), gate width (Z), electron charge (e) and electron mobility (μ_p) then the following equations were used to simulate the results from equation below;

$$I_{DS} = KV_{DS}^2 = K\left(V_G - V_T\right)^2$$ Where

$$K = \frac{\in \mu_n z}{2La}$$

This gives the change in drain current I_{DS},sat (saturation) with the drain voltage $V_{DS,sat}$ at different scaling factors. Also equation below was used to plot graphs of drain current against gate voltage

$$I_D = \frac{\in \mu_n Z}{Ld}\left[\left(V_G - V_T\right)V_D - V_D^2\right]$$

IV. Figures And Discussions

This chapter contains the results of all simulations done for drain current verses drain voltage. Figures 2.1 to 2.3 shows the graphs of drain current against drain voltage at different gate voltage and with different scaling factors.

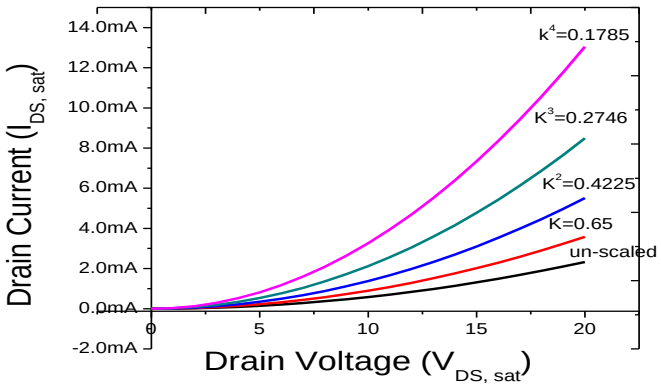

Figure 2.1 Graph of $I_{DS,\ sat}$ –$V_{DS,\ sat}$ at saturation at different scaling factors (un-scaled, K=0.65, K^2=0.4225, K^3=0.2746 and K^4=0.1785)

Figure 2.1 shows a graph of saturation drain current against saturation drain voltage. It is observed that for un-scaled device, the change in drain current against drain voltage is small. As the device is scaled down, the change in drain current against drain voltage increases.

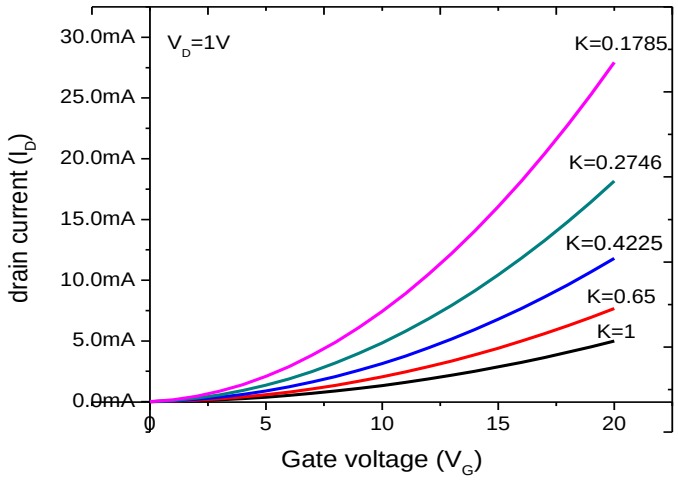

Figure 2.2 Graph of drain current against gate voltage (transfer curves) at V_D=1V and at different scaling factors (un-scaled, K=0.65, K^2=0.4225, K^3=0.2746 and K^4=0.1785)

Figure 2.2 shows a graph of drain current against gate voltage at VD=1V and at different scaling factors. For un-scaled device at L=100 Å, Z=100 Å the rate of change of drain current against gate voltage is small but increases with scaling. This is an increase in the trans-conductance of the device with scaling. It's also observed that there is a shift in the threshold voltage. The threshold voltage decreases with scaling.

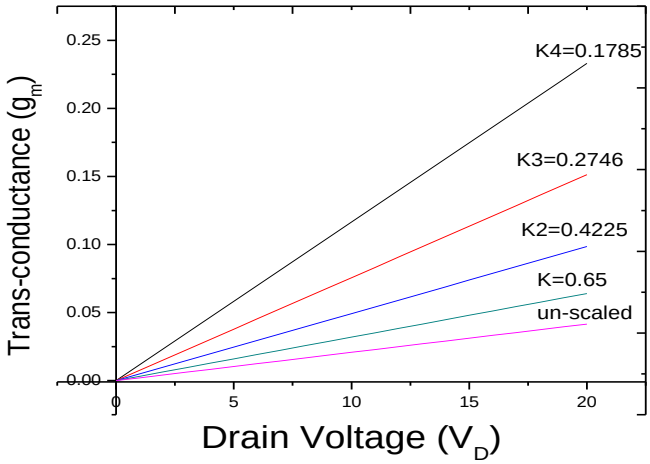

Figure 2.3 Graph of trans-conductance against drain voltage at different scaling factor

Figure 2.3 shows the graph of trans-conductance (g_m) against drain voltage (V_D). It's observed that gm is directly proportional to the drain voltage. It's also worth noting that down-scaling the device increases the trans-conductance of the device. The figure above shows the g_m-V_D graph at various scaling factors as indicated. The smaller the device, the higher the trans-conductance.

V. Conclusion

The MOSFET controls the drain current by controlling the population of charge carriers from the n-channel. When the gate is made more positive, it accumulates the majority carriers to a larger zone around the gate and this increases the current flow for a given value of VDS. Therefore, modulating the gate voltage modulates the current flow through the device [6]. This is evident in the characteristic curves for the device.

The findings indicated that for a miniaturized device there was quite an improvement on its performance. To turn the MOSFET ON the input capacitance C_{iss} must be charged as fast as possible. To turn it OFF it involves the discharge of capacitance C_{iss}. The turn on delay $t_{d\ (on)}$ is the time required to charge the input capacitance to threshold voltage level (V_{TH}). The rise time, t_r is the gate charging time from V_{TH} level to full gate. For small geometry design it's observed that input capacitance is small hence smaller turn on delay and smaller rise time. This owes to the reduction in parasitic capacitances hence a higher speed.
It's also observed that for a MOSFET with large geometry the drain current is significantly small but can be increased by scaling down the device. This shows that there is a strong correlation between device dimensions and device performance. The shorter the length, the greater the driving ability because channel resistance is proportional to channel length. As a consequence performance of the MOSFET can be enhanced by downscaling. In-view of all this it requires the industry to intensify research of CMOS into an increasingly difficult manufacturing domain. However, there are many challenges to be faced as device dimensions become smaller, and therefore a method should be developed that will enable to compensate for this short channel effects.

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