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Progress in Hetero Junction Thin Film Silicon Solar Cell

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Abstract:

Solar photo-voltaic (PV) modules is dominated by crystalline silicon (c-Si) solar cell which captures nearly 80% of the total PV market because of its high conversion efficiency though they are bulky (wafer thickness ~300 micrometer) and have high material cost. Thin film amorphous silicon solar cell for its low cost, deposited on large areas is suitable for large scale terrestrial application. But thin film hydrogenated amorphous silicon (a-Si:H) solar cell technologies occupies only 10% of PV market as its conversion efficiency stuck at 10% in PIN solar module which again degrade by 25% in single junction cells, before stabilization sets in. Researcher are trying to combine both the light weight and low cost a-Si:H material with the high stable efficiencies of crystalline silicon to get most advantageous result of conversion efficiency. Possibly, the Hetero junction a-Si:H/c-Si with Intrinsic Thin layer (HIT) solar cells would be the satisfactory fulfillment of scientists. This article reviews how HIT solar cell opens up the new scope in solar photo voltaic industries and advances with increasing efficiency. Keywords: Amorphous silicon solar cell, Crystalline silicon solar cell, Hetero junction solar cell, Hetero junction solar cell, Hetero junction solar cell, Hetero junction solar cell, Hetero

I. Introduction:

The conversion of solar power in to pollution free green and clean energy requires high efficiency devices that can generate electricity for practical use. It also demands that the device and its fabrication technology must be cheap for industrialization. It attracts attention of researchers working on various photovoltaic materials and technologies. Besides mono-crystalline silicon solar cell technology of various generations of solar cell has been developed. The thin film technology is mostly acceptable due to its low production cost. The low cost thin film amorphous hydrogenated silicon solar cell (a:Si:H) is very light, can be deposited on large area suitable for large scale application. Among the third generation solar cell, dye-sensitized (DSSC) solar cell, organic photovoltaic solar cell, hybrid metal halide perovskites are promising photo voltaic (PV) technologies. This type of new generation solar cell is in infant stage, far apart from commercialization. All this materials have poor stability. Though Hybrid metal halide perovskite solar cell (PSC) has achieved high efficiency (certified 22%) for a small area 0.1 cm² and it is cheapable also, but there are some difficulties for large area production. As the perovskite materials are very fragile, continuous un-ruptured and void-less perovskite with selective carrier extraction layer over a large area is difficult to fabricate. Again this type of perovskite material is decomposed thermally or easily dissolved in water. The rapid increase of efficiency (16.4%) of organic solar cell (OPV) is also notable but the cell area is again too small (0.04 cm²) for making outright record.

Hetero junction intrinsic thin film (HIT) is formed by combining the low cost hydrogenated amorphous silicon with high stable efficiencies crystalline silicon wafer by PECVD technique. Hetero junction intrinsic thin film solar cells HIT, the structure and its current status with the advancement of its structural modification is also described here.

II. HIT Solar Cell:

The key problem of solar photo voltaic is the loss of carrier concentration due to recombination at the boundary of the p-n junction and was successfully reduced by improvement on the mono crystalline cell structure using **Subjects** different material in the p-n junction instead of a crystalline wafer. Many researchers have been working on p/n (a-Si/C-Si) Hetero-junction solar cell. But this hetero junction had a large background current and poor junction property. The modification of hetero junction technology was initiated by the research and development team at Sanyo in 1990 ¹. In 1990 research and development team at sanyo started to develop the hetero junction technology. This is an improvement on the classic mono crystalline cell using different material than a crystalline wafer in the p-n junction. The invention addresses the key point in solar photo-voltaics:



Fig. 1 Hetero junction Solar cell

By using ACJ (artificially constructed junction), they developed 2 a new structure of solar cell in where the a-Si thin i-layer is incorporated into the p/n hetero junction and named it Hetero junction with Intrinsic Thin Layer. The backward current was reduced and seems to reduce the recombination of carrier near the interface. They showed that the value of short circuit current (I_{SC}) was higher than that of the basic hetero-junction p/n (a-Si/C-Si) structure. Due to improvement in the interface properties the collection efficiency as well as short circuit current density (J_{SC}) was increased. In that case V_{OC} was increased by 30 mV and FF was also enhanced by more about 0.8 than p/n hetero junction structure. Conversion efficiency was also increased in HIT structure rather than p/n hetero junction structure. They had been able to fabricate high conversion efficiency stable HIT solar cell (η =18.1%) and prepared by simple low temperature process (< 200°C). The output characteristics of HIT solar cell were unchanged after 10 hours irradiation. Therefore the hetero junction with intrinsic thin layer (HIT) technology sets a new

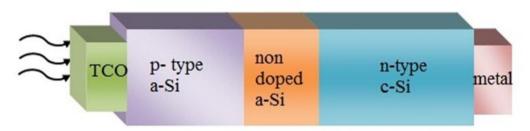


Fig. 2 Hetero junction with intrinsic thin layer Solar cell

height of efficiency and high temperature performance. A record was set for efficiency (23.8%) of solar panel with commercial size by producing a power of 275 W in march 2016 by the Panasonic ³. Recently the hetero junction thin layer (HIT) structure is the most promising technology for the production of high efficiency and good quality solar cells.

Fig. 3 shows the modified structure of an HIT solar cell. A randomly textured n-type Czochralski (CZ) crystalline wafer is sandwiched between a p-layer and intrinsic i-layer on one side and intrinsic i-layer and n-layer on either side. The HIT solar cell is formed by the deposition of an intrinsic (i type) a-Si layer and a p-type a-Si layer on the thin crystalline silicon wafer to form a p/n hetero junction and another i-type and n-type a-Si layers are deposited on other side of the wafer to produce back surface field (BSF) layer of the cell. On both side of the doped a-Si:H layer a transparent conducting oxide (TCO) layer of Indium Tin Oxide (ITO) is deposited and electrodes in the form of metal grid is made by the screen print technology. Here the defects on the surface of the c-Si wafer is effectively passivated by inserting the layer of high quality intrinsic a-Si:H layer which results in a high $V_{\rm oc}$ of the device. To prevent the thermal damage of the cell components due to high temperature emitter diffusion the entire process of deposition should be carried out at low temperature Radio Frequency Plasma Enhanced Chemical Vapor Deposition (RFPECVD) technique. The textured front surface (TCO) plays the most important role to minimize the reflection of the incident photon.

Also the degradation of performance of a solar cell is indicated by its temperature coefficient which is much lower in the case of HIT solar cell. This lower temperature coefficient made the HIT solar cell possible to maintain higher efficiency and to deliver higher power even if at higher temperature. Beside that the low temperature deposition enables to use of thin wafers. To get the high efficiency from HIT solar cell scientists are continuously trying to improve different components of HIT solar cell for its further development either by using good a-Si:H/c-Si hetero junction layer, by developing the good grid quality or by reducing the absorption in the a-Si:H and TCO layers.

To get the higher V_{oc} , a high quality intrinsic thin layer should be required as incorporated intrinsic - layer should reduce the tunneling by localized states in the doped layer. The hetero-junction structure improves V_{oc} considerably by the effects of the large energy band gap of the front amorphous silicon layer and the excellent quality of the interface between the amorphous

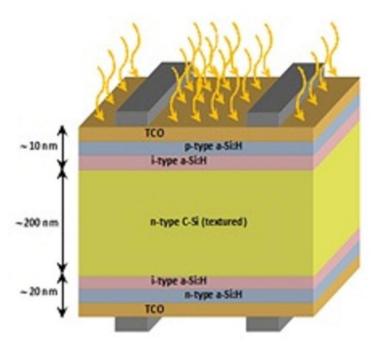


Fig. 3 Structure of the hetero junction with intrinsic thin layer solar cell

layer and the crystalline substrate. So there is a great challenge to get a good quality of intrinsic layer as well as interface. A simulation studies by Maydell et al ⁴ emphasizes that the quality of a-si:H/c-Si is responsible for good performance of the cell. Recombination at the amorphous /crystalline interface reduces the performance of the hetero junction solar cell.

The fill factor (FF) is also affected by both the junction property and the resistive loss. Scientists have tried to increase the FF by improving the surface passivation quality of a-Si layers. They minimized the resistive loses in electrodes using silver paste and TCO. The bulk property of CZ Si wafer is also important for high efficiency solar cells. As the surface recombination velocity of CZ Si wafer is very low it is able to get true potential by using this type of bulk material. Wafer quality, wafer preparation and also good quality a-Si all are the most fundamental requirement to achieve high efficiency solar cell.

In 2009 Taguchi et al $^{5.6}$ had been able to achieve solar cell conversion efficiency 22.3%. This is the world's first practical-size (>100 cm 2) solar cell. They got 0.725 V as V_{oc} , I_{sc} : 3.909 A, FF: 0.791 by changing the a-Si:H/c-Si interface by using new cleaning process and new deposition conditions for a-Si;H layers. With clean c-Si surface, improved textured structure, lower-damage-deposition process, lower-light-absorbing TCO, and finer grid electrode, they obtained the conversion efficiency 22.6%.

In 2014 Taguchi et al 7 achieved the efficiency of HIT solar cell is 24.7% with a 98-micrometer thick wafer for a total cell area 101.8 cm 2 . The value of open circuit voltage was also increased. By optimizing the thickness and by improving the film properties they have been able to reach the value of open circuit voltage to 0.750 V. They also confirmed that the HIT solar cell with thin wafer thickness can achieve high conversion efficiency than thick wafer.

Data for year wise performance of HIT solar cell

Year	V _{oc} [volt]	Jsc [mA/cm²]	FF	Efficiency [%]
1990	0.614	37.9	0.776	18.1
2009	0.725	39.09	0.791	22.3
2012	0.745	39.4	0.809	23.7
2014	0.750	39.5	0.832	24.7

To improve the power conversion efficiency of HIT solar cell Sathya et al ⁸ designed a simulated hetero junction solar cell. This HIT structure is formed by TCO/a-Si:H(P)/A-Si:H(i)/c-Si(n)/a-Si:H(n+)/Ag. The simulated result of HIT solar cell was the open circuit voltage of 0.751V, a short circuit current density of 36.37 mA/cm² and fill factor of 85.37% contributing to the total power conversion efficiency 25.91. They suggested that this increase in conversion efficiency compared to the other HIT solar cell is due to the reduction of resistive losses, recombination losses at the hetero junction interface between intrinsic a-Si and c-Si and optimization the

thickness in a-Si and c-Si layers. It may be expected that by reducing the recombination losses at p/i interface researcher must be able to reach the growing efficiency demanded by PV market.

A high quality TCO film is very much important as it enhances the efficiency of hetero junction solar cell. So efficiency of hetero junction with intrinsic layer solar cell can be enhanced by fabricating different type of high quality TCO materials. In 2016 Maity et al⁹ showed that hexagonal nano piller of ZNO deposited on ptype Si substrate have increased the efficiency of solar cell as it enhances the light absorption. It is suggested that the material of TCO of HIT solar cell can be replaced by nano piller form or nano wire form that can increases the light absorption than conventional TCO and exceed the current conversion efficiency. In 2018 Lee et al lo showed that it is very important to choose TCO layer which is suitable for HIT solar cell performance. Different materials with high transmittance can be used as TCO of solar cell. But low surface resistance and high optical transmittance are mostly desirable for choice of transparent conducting oxide materials. A transparent conducting polymer poly (3,4-ethylene dioxythiophene): polystyrenesulfonic acid (PEDOT:PSS), shows 90% transmittance but due to high sheet resistance [1000 ohm/sq], it can be discarded in HIT solar cell. Though Ag nano-wire presents high transmittance and low sheet resistance, for its corrosion by chemical reactions it can be oxidized and discarded in fabrication of HIT solar cell. They suggested that the ITO and ZNO films are the appropriate transparent conducting layer for HIT solar cell.

Though HIT solar cells is very promising technology, still it cannot be deposited over large area like the amorphous silicon thin film solar cell. Sanyo took HIT cell as a patent and we expect that HIT cell can acquire the place as a building integrated technology in near future.

III. Conclusion:

The production of practical alternative power source will demand highly efficient and inexpensive device to generate electrical power from solar radiation, i.e. a green energy conversion device. Lower temperature coefficient of HIT solar cell points out that it is advantageous to produce more electrical energy at lower temperature over the other photo voltaic modules. Again HIT solar cell is not influenced by light induced degradation like amorphous silicon solar cell. The current article discusses the recent technological advancement of fabrication of HIT solar cells. It also analyzes that how the efficiency of HIT solar cell can gradually be enhanced by incorporating some modifications of different layer of solar cell for practical use in twenty first century. It can be concluded that the HIT solar cell have a great potential for industrial large scale manufacturing. After a thorough and long research on HIT solar cell could be the correct alternative of crystalline silicon solar cell.

References:

- [1] M. Taguchi, M. Tanaka, T. Matsuyama, T. Matsuoka, S. Tsuda, S. Nakano, Y. Kishi, Y. Kuwano, Improvement Of The Conversion Efficiency Of Polycrystalline Silicon Thin Film Solar Cell, In Proc. Int. Photovoltaic Sci Eng. Conf.-5 Tech. Dig (1990) 689–692
- [2] M. Tanaka., M. Taguchi, T. Matsuyama, T. Sawada, S Tsuda, S. Nakano, H. Hanafusa, Y. Kuwano Developments Of New C-Si. Jpn. J. Appl. Phys 31 (1992) 3518-3522
- [3] Sunpower (Usa) November, 2015. Judged From The Solar Cell Efficiency Tables (Version 47), Prog. Photovolt Res. Appl. 24 (2016)
- [4] M. Schmidt, L. Korte, A. Laades, R. Stangl, Ch. Schubert, H. Angerrmann, E, Conrad, K V, Maydell, Physical Aspects Of A-Si:H/C-Si Hetero-Junction Solar Cells Thin Solid Films 19 (2007) 7475-7480
- [5] M. Taguchi, Y. Tsunomura, H. Inoue, S. Taira, T. Nakashima, T. Baba, H. Sakata, E. Maruyama, High-Efficiency Hit Solar Cell On Thin (<100 Mm) Silicon Wafer, In Proc. 24th Eur. Photovoltaic Sol. Energy Conf. (2009) 1690–1693</p>
- [6] Y. Tsunomura, Y. Yoshimine, M. Taguchi, T. Baba, T. Kinoshita, H. Kanno, Twenty-Two Percent Efficiency Hit Solar Cell , Solar Energy Materials & Solar Cells 93 (6-7) (2009) 670-673
- [7] M. Taguchi, A. Yano, S. Tohoda, K. Matsuyama, Y. Nakamura, T. Nishiwaki, K. Fujita, E. Maruyama 24.7% Record Efficiency Hit Solar Cell On Thin Silicon Wafer, Ieee Journal Of Photovoltaics 4 (1) (2014) 96-99
- [8] P. Sathya, R. Natarajan, Design And Optimization Of Amorphous Based On Highly Efficient Hit Solar Cell, Applied Solar Energy 54 (2018) 77-84
- [9] S. Maity, C. T. Bhunia, P. P. Sahu, Improvement In Optical And Structural Properties Of Zn Hexagonal Nanopillar Formation To Improve The Efficiency Of A Si-Zno Hetero Junction Solar Cell, Journal Of Physics D:Applied Physics 49 (20) (2016) 205104
- [10] H. Park, Y. Lee, J. Park, Front And Back Tco Research Review Of A-Si/C-Si Heterojunction With Intrinsic Thin Layer (Hip) Solar Cell, Transactions On Electrical And Electronic Materials, 19(1), (2018) 1-8