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A simple model for the temperature dependence of the Fowler-Nordheim carrier tunnelling current through the oxide in a metal-oxide-semiconductor device in accumulation or inversion

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Abstract: *A simple model for the temperature dependence of the Fowler-Nordheim carrier tunnelling current through the silicon dioxide in a metal-oxide-semiconductor device in accumulation or inversion is proposed. The model is based on the premise that the average energy of the electrons in the oxide change exponentially because the number of electrons in the oxide change exponentially due to ionization at high fields giving a multiplication factor for the carrier tunnelling current. The electron barrier heights or the conduction band offsets in a 4H-SiC MOS device have been computed from the equation for the model at temperatures ranging from 10 K to 698 K. These have been compared with the experimentally observed barrier heights on commercial n-channel 4H-SiC MOSFETs in inversion. The change in barrier height with temperature is found to be -2.9 x 10^{-4} eV/K from the model and -6.86 x 10^{-4} eV/K from the commercial MOSFETs. The difference is attributed to the inaccurate calculation of the oxide field in the commercial MOSFETs. Similar behaviour is observed in a Si MOS device of an earlier study.*

Keywords: *Barrier height, Fowler-Nordheim, Metal-Oxide-Semiconductor, Silicon Carbide, Temperature.*

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I. Introduction

Wide bandgap semiconductors (WBG) form the cornerstone of the field of high temperature and high frequency power electronics. Three relevant reviews out of many are studied by the author [1-3]. The review by Casady and Johnson [1] points to the remarks made by William Shockley at the first conference on SiC in April 1959 on the importance of SiC as a material for high temperature electronics. SiC has the advantage of having thermal SiO_2 as the native oxide for fabricating MOSFET devices along with high thermal conductivity and high saturation velocity of electrons. Infact, commercial WBG semiconductor based MOSFET devices are now available in the market from companies like Wolfspeed, ST Microelectronics, Rohm, Infineon, and others. Neudeck et al. [2] reviewed the parameters of WBG semiconductors relevant for high temperature applications and enlisted the applications at high temperatures. Okumura [3] enlisted the high frequency and high power applications and delineated the role of power switching devices in different power applications. The figures of merit for the semiconductor materials and devices describe their relative importance in power electronics [4, 5].

A high temperature floating gate MOSFET type memory device on SiC or Diamond WBG semiconductor is a possibility in the future for high temperature applications. Charge leakage from the floating gate at high temperatures is a concern that would reduce the retention time of the charge and thus reduce the lifetime of the memory device. Since reading, writing and erasing in a floating gate type FLASH memory of the non-volatile type is performed by the Fowler-Nordheim (FN) carrier tunnelling currents, the study of the temperature dependence of the FN carrier tunnelling phenomenon to develop its understanding is important. Many research groups have done this study. Some of them are mentioned here in this article. Khlifi et al.[6] combines the Schottky conduction with the FN conduction, Waters and Zeghbroeck calculate a temperature-dependent flatband voltage to apply to the FN analysis at high temperatures [7], Le-Huu et al. [8] and Sometani et al. [9] combine FN tunnelling with Poole-Frenkel conduction from a carbon based trap in the oxide at 1.2 eV from the oxide conduction band (CB) to explain currents at high temperature and high fields, and Toumi et al. [10] fitted the experimental I-V-T data by minimizing the vertical quadratic error S on the vertical current axis by evaluating $\partial S / \partial x$ equal to zero. The $d\phi / dT$ where ϕ is the electron barrier height, obtained by the above researches are in few meV/K which are high as compared to the experimental data observed on commercial MOSFET devices by O. Avino-Salvado et al. giving $d\phi / dT$ of -6.86 x 10^{-4} eV/K [11].

This research article attempts to model temperature dependence of FN carrier tunnelling current through a MOS or MOSFET device at high fields based on the premise that the number of electrons in the oxide change exponentially due to ionization causing an exponential change in the average kinetic energy of the

electrons in the oxide also, thereby changing the current. An increase in temperature causes an increase in current and a decrease in temperature causes a decrease in current. The increase in current causes the barrier height to decrease and decrease in current causes the barrier height to increase. The anchor point in the model is the measured current at room temperature of 298 K. The electron barrier height of 2.79 eV at 298 K on the 4H-SiC MOS device has already been confirmed by many research groups [12-15].

II. Theory

Fowler-Nordheim carrier tunnelling current equation through a MOS device in accumulation or inversion is given by [16, 17]:

$$J = AE_{ox}{}^{2} \exp(-B/E_{ox}) \qquad (1).$$

Here, A and B are constants given as follows:

$$A = \frac{e^3 m}{16\pi^2 \hbar m_{ox} \phi_0}$$

$$A = 1.54x10^{-6} \frac{m}{m_{ox}} \frac{1}{\phi_0} \cdots A/V^2 \qquad (2)$$

$$B = \frac{4}{3} \frac{(2m_{ox})^{1/2}}{e\hbar} \phi_0{}^{3/2}$$

$$B = 6.83x10^{7} \left(\frac{m_{ox}}{m} \right)^{1/2} \phi_0{}^{3/2} \cdots V/cm \qquad (3).$$

In the above constants A and B, e is the electronic charge in Coulombs, m is the free electron mass in Kg, m_{ox} is electron mass in the oxide in Kg, ħ is the reduced Planck's constant, ϕ_0 is the electron barrier height in eV, and B is called the FN tunnelling slope constant at a particular temperature in Kelvin. E_{ox} is the oxide field in V/cm. Equation (1) models the current-voltage characteristics across the oxide at high electric fields E_{ox}. For modeling the temperature dependence of this equation a multiplication factor M is devised given by:

$$M = \exp\left(\frac{(3/2)k(T - T_0)}{kT_0} \right) \qquad (4).$$

Here, k is the Boltzmann constant, T is the temperature in Kelvin (K), and T_0 is 298K. The equation (1) thus becomes:

$$J = (A)(M)E_{ox}{}^{2} \exp(-B'/E_{ox}) \qquad (5).$$

$$T = T_0 + (T - T_0)$$

$$\left(\frac{(3/2)kT}{kT_0} \right) = \left(\frac{(3/2)kT_0}{kT_0} \right) + \left(\frac{(3/2)k(T - T_0)}{kT_0} \right) \qquad (6)$$

Taking M inside the exponential, the term in the exponential becomes:

$$\left(\frac{-B}{E} \right) + \left(\frac{(3/2)kT_0}{kT_0} \right) + \left(\frac{(3/2)k(T - T_0)}{kT_0} \right) \qquad (7)$$

The first two terms are clubbed together as -206/6 due to the measurements at room temperature of 298 K given that B is the slope constant for the FN tunnelling current at about 0 K. Therefore, the final equation for the FN tunnelling current density with temperature is given as:

$$J = AE_{ox}{}^{2} \exp\left(\frac{-B'}{E_{ox}} + \frac{(3/2)k(T - T_0)}{kT_0} \right) \qquad (8).$$

For the purpose of calculations, equation (8) can be written as:

$$J = AE_{ox}^{\ 2} \exp\left(\frac{-206}{6} + \frac{1.5(T-298)}{298}\right) \qquad (9).$$

Here, data of n-4H-SiC MOS sample fabricated on (0001) oriented surface of Si-face form the author's collaborative study is taken [17] with E_{ox} = 6MV/cm in the FN region, having a room temperature FN electron tunnelling slope constant B' of equation (8) as -206 MV/cm and A is already presented in the beginning. The model values in the Table I below are created based on the equation (9). The multiplication factor M comes from the physics of ionization based on which there is an exponential increase in the number of electrons due to the minimum energy required for ionization [18]. The average kinetic energy of a conducting electron in a semiconductor, given that SiO_2 can be treated as a semiconductor, having three degrees of freedom is given by (3/2) kT at thermal equilibrium from the theorem for equipartition of energy [19]. This energy is more applicable at high temperatures than at very low temperatures. Since the number of electrons during ionization change exponentially, therefore the average kinetic energy of the electrons will also change exponentially giving a multiplication factor M in the FN tunnelling equation (5). Single ionization of two SiO_4 tetrahedron linked with O atom in SiO_2 is considered. The average kinetic energy of electrons is normalised by dividing by kT_0. Theoretical and experimental studies on impact ionization in thermal SiO_2 have been initiated [20, 21]. DiMaria et al. [21] have shown that there is an exponential increase in the number of electrons due to impact ionization. This type of exponential dependence is also present in the research paper by Indian scientist Megh Nad Saha in 1920, where he has discussed the ionization in the solar chromosphere . His equation takes care of the heat of dissociation U, instead of the minimum ionization energy required in a semiconductor [18, 22]. The exponential dependence of temperature on the chemical reaction rates is also given by Arrhenius relation of the same kind given as exp ($-E_a/kT$). In semiconductors, the intrinsic carrier concentration is related exponentially to negative of the bandgap divided by 2kT as another example of exponential temperature dependence [23]. One last example included here is the high temperature operating life (HTOL) testing performed on MESFET and PHEMT devices where 20% degradation in the drain current due to high temperature stress gives the mean time to failure (MTTF) for the device. Here, time to failure is proportional to $\exp(E_a/kT)$ where E_a is the activation energy for drain current degradation and T is the temperature in Kelvin [24, 25].

III. Results and Discussion

Two sets of results are obtained from equation (9) for the model. The first set of results is presented in Table I and II and the second set is presented in Table III. At a given temperature T, the term enclosed in the exponential of equation (9) is computed, the result of which is multiplied by 6 to give the new slope constant B at that temperature and then using equation (3) for B, ϕ_0 is computed. Thus, the model values of ϕ_0 from 10 K to 698 K are tabulated in Table I and II. The experimental values of barrier heights from commercial MOSFETs [11] are also tabulated for comparison. The experimental values of the electron barrier heights obtained by various research groups are also presented for comparison. The immediate observation is that the electron barrier heights or conduction band offsets (CBO) decrease with increasing temperatures beyond room temperature of 298 K and increase with decreasing temperature up to 10 K. Essentially, the FN electron tunnelling current increases due to exponential increase in the number of conducting electrons at a high temperature and at a sample high oxide field of 6 MV/cm in the FN region which translates into a lower computed barrier height or CBO. The current decreases at a lower temperature resulting in an increased computed CBO.

Table I. Computed and observed electron barrier heights (CBOs) in the temperature range from 173K to 523 K.

Temperature (K)		173	198	223	248	273	298	323	348	373	398	423	448	473	498	523
CBO eV	Average [11]	2.99	2.98	2.96	2.95	2.94	2.92	2.91	2.89	2.87	2.86	2.83	2.82	2.80	2.78	2.75
	Model Values	2.82	2.81	2.81	2.80	2.79	2.79	2.78	2.77	2.77	2.76	2.75	2.75	2.74	2.73	2.73
	Difference	0.17	0.17	0.15	0.15	0.15	0.13	0.13	0.12	0.10	0.10	0.08	0.07	0.06	0.05	0.02
	Lichten[26]											2.83				
	Le-Huu [8]						2.68			2.65		2.59		2.51		2.42
	Yu [27]						2.57							2.36		
	Agarwal[28]						2.43					2.11				

Table II. Computed electron barrier heights based on the model in the temperature range of 10 K to 698 K.

Temperature (K)		173	100	50	10	698
CBO (eV)	Model Values	2.82	2.84	2.855	2.87	2.68

From the Table II, it can be observed that at the temperature of 10 K, the electron barrier height is 2.87 eV. This gives a FN slope constant B = 68.3 x $(0.42)^{0.5}$ $(2.87)^{1.5}$ = 215.2 MV/cm at about 0K temperature. So B' of -206 can be written as -215.2+ 9. Now, (-B'/E) of (-206/6) becomes (-215/6 + 9/6). We know that (3/2) kT_0/kT_0 = 9/6. So equation (9) can be written as:

$$J = AE_{ox}^{\ 2} \exp\left(\frac{-215}{6} + \frac{9}{6} + \frac{1.5(T-298)}{298}\right) \quad (10)$$

$$J = AE_{ox}^{\ 2} \exp\left(\frac{-215}{6} + \frac{1.5kT_0}{kT_0} + \frac{1.5k(T-T_0)}{kT_0}\right) \quad (11)$$

$$J = AE_{ox}^{\ 2} \exp\left(\frac{-215}{6} + \frac{1.5T}{298}\right) \quad (12).$$

It can be observed that the B in equation (7) is -215MV/cm. Equation (12) is same as equation (8) and (9). It now uses the slope constant of -215 MV/cm at about 0K in place of -206MV/cm at 298 K, and calculates the current at any temperature T in Kelvin. For example, the slope constant at173 K is calculated using equation (12) to be -209.775 giving a CBO of 2.82 eV as presented in the Table I above.

The change in the barrier height from 10 K to 698 K is only about 0.2 eV from the model, giving a coefficient of -2.9 x 10^{-4} eV/K. This coefficient is small and from the technology perspective not of critical importance. From the perspective of science, the effect is real and highlights the importance of the temperature dependence of the FN carrier tunnelling current. The coefficient is -6.86 x 10^{-4} eV/K obtained from the experimental data of the commercial MOSFETs in inversion [11] in the temperature range of 173K-523K, and is comparable to the one obtained from the model. To the author's understanding, an important reason for the difference in the coefficients and the CBO values of other research groups lies in the calculation of the oxide field with the MOS or MOSFET device in inversion. The formula used by O. Avino-Salvado et al. [11] is given as:

$$E_{ox} = \frac{V_G - V_{fb} - \psi_s}{t_{ox}} \quad (13).$$

Here, V_G is the applied gate voltage, V_{fb} is the flatband voltage and ψ_s is the inversion potential at the surface of the semiconductor/oxide interface in the MOSFET device in inversion. The formula above contains the theoretical band bending at the semiconductor surface ($V_{fb} + \psi_s$). This should be replaced by the experimental band bending voltage given by ($V_T + Q_d/C_i$), where Q_d is the depletion charge per unit area for the device in inversion, C_i is the insulator capacitance per unit area, and V_T is the experimental threshold voltage [29-31]. The replacement would result in a lower value of the oxide field. This lower value will cause a larger change in $\Delta(1/E_{ox})$ resulting in a lower CBO when $\Delta\ln(J/E_{ox}^{\ 2})$ is divided by $\Delta(1/E_{ox})$ to obtain the slope constant B at a given temperature. As an example, the CBO at room temperature is 2.92 eV [11] as compared to the correct value of 2.79 eV. An incorrect or an approximate value of E_{ox} could be a major source of error in the values of the CBOs determined by other research groups. The thickness of the oxide also has to be quite accurate within ±1nm for say a 40 nm oxide. $E_{ox} = V_G/t_{ox}$ can be used for large oxide thickness such as 100nm, but for thinner oxides, the experimental band bending becomes significant. It can be observed from the specification sheet of the MOSFET used [11], that V_T reduces with increasing temperature. This causes the difference between the theoretical and experimental band bending to reduce with increasing temperature. This observation corroborates to the fitting of the model values of the electron barrier height to those of the experimentally observed average values of Avino et al. [11] in Table I.

Experimental studies of temperature dependence of the FN electron tunnelling current across a MOS device in accumulation or inversion is not new. Lenzlinger and Snow conducted a study in 1969 [32] when it was shown that thermal silicon dioxide based MOS device exhibited electrode-limited conduction rather than bulk-limited conduction as in silicon nitride or tantalum oxide containing more bulk traps. Furthermore, the temperature dependence was thought to be due to the barrier height variation with temperature, given in Appendix II of the reference by the equation [32]:

$$\phi(T) = \phi_0(1 + \alpha(T)) \qquad (14).$$

Here, α is the coefficient for variation in barrier height which for Si bandgap is 7.021 x 10^{-4} eV/K [33, 34]. The electron tunnelling current has a multiplicative term $\pi ckT / \sin(\pi ckT)$ that models the temperature dependence. The model does not satisfy the experimental current-voltage characteristics at different temperatures when using the electron effective masses in the oxide same as the masses for the electrode-limited conduction of say 0.42m for Si. A relative mass of 0.94m or 0.96m had to be used, where m is the free electron mass. Also, the calculated value of barrier heights given in Fig. 9 of the reference and reproduced in Table III below have not been proven experimentally. Column 4 and 5 in Table III presents the calculated values of CBOs at two different oxide fields at temperatures from 100 K to 423 K using the model in the present study and described in the theory section. The slope constant B for the electron tunnelling current through Si/SiO_2/metal MOS device is taken as 254 MV/cm [29] at 298 K replacing 206 MV/cm in equation (9). It shows nearly 0.1 eV change in the CBOs from 100K to 423K giving a coefficient of -3.4 x 10^{-4} eV/K. in this temperature range. A change in the high oxide field in the FN region of 8 MV/cm from 6.9 MV/cm does not affect the CBO values. Column 6 in Table III below also presents the current calculated at different temperatures across the MOS device using the equation for the model in the present study. These are comparable to the experimentally observed current given in Fig.8 of the reference [32]. It can be observed that the currents at 100K and 300K calculated with the equation (9) for the model in the present study matches to the experimentally observed values in Fig.8 of the reference [32]. The current at 373 K does not match and is a little less than the observed value.

Table III. The CBOs computed using the model, compared with values of L and S [32] at several temperatures.

Sample	Calculated values of electron barrier heights and currents at various temperatures using the model.				
Si/SiO_2 MOS device having 100nm thick thermal oxide	Temperature (K)	CBO calculated by Lenzlinger and Snow	CBO at 6.9 MV/cm, (eV)	CBO at 8.0 MV/cm, (eV)	Current (pA) for 30 mil diameter dots, Area=4.56 x 10^{-3} cm^2, at 6.1 MV/cm
	100	3.23	3.26	3.27	0.06
	200	3.13	3.23	3.24	
	300	3.20	3.20	3.20	0.16
	350	3.08	3.19	3.19	
	373	3.07	3.18	3.18	0.23
	423	3.02	3.17	3.16	

IV. Conclusions

A model for temperature dependence of the FN carrier tunnelling current is proposed. It is based on the physics of ionization when there is an exponential increase in the number of electrons due to ionization in the oxide. The average energy of the electrons is given by (3/2)kT which also changes exponentially, thus changing the current. This multiplicative factor is added to the exponential term of the FN tunnelling equation. The model appears to be a good fit to the experimentally observed changes in the electron barrier height due to change in temperature in the commercial 4H-SiC power MOSFETs in inversion. The $d\phi / dT$ observed in the commercial MOSFETs is -6.86 x 10^{-4} eV/K and that from the model is -2.9 x 10^{-4} eV/K. These are comparable and the difference is due to the inaccurate calculation of the oxide field in the commercial MOSFETs where, for example the barrier heights at room temperature of 298K can be compared. The Si MOS device behaves similarly and has a smaller change in the electron barrier height than that calculated by Lenzlinger and Snow. From the perspective of the technology, the change in barrier height due to the change in temperature is very small and may not affect the reliability of the device. The temperature effect on the barrier height is significant from the perspective of science. The technology can thus be more tolerant of deviations in parameter values than science.

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